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Distributed Modeling and Characterization of On-Chip/System Level PDN and Jitter Impact

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Abstract

The constant pursuit of higher operating speeds combined with the effort to reduce power consumption creates increasingly stringent requirements for modern I/O interfaces. As the voltage margins shrink and the operating frequencies increase, the quality of the power delivery network becomes the critical factor that determines the I/O performance. A successful I/O design depends on having a robust and reliable power supply at all levels of the system.

This paper describes a methodology flow that enables characterization of a system-level power delivery network. The methodology takes into consideration the combined effects of chip, package, and board-level components of a power supply. The system approach results in a very accurate prediction of the power supply noise and of its impact on the system timing. The characterization flow brings together different commercial computer-aided engineering tools as well as some in-house techniques to create a complete model of a power delivery network. The correlation and verification steps use several types of Xilinx FPGA products as test vehicles, and leverage the flexibility offered by FPGAs to measure the parameters of the system. Modeling and measurements are done both in frequency and time domains. Such characteristics of the system as frequency-dependent power delivery network impedance, transient voltage noise, I/O phase noise, and jitter are all considered.

Author Biographies

Dmitry Klokotov is Senior Signal and Power Integrity Engineer at Xilinx Inc. He specializes in modeling and validation of system level power delivery networks, and characterization of crosstalk and power supply noise induced jitter in high-speed I/O interfaces. He received his MS and PhD degrees in Electrical and Computer Engineering from the University of Illinois at Urbana-Champaign, and BS degree in Physics from Saratov State University, Saratov, Russia.

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Yong Wang is Engineering Director of Device Power and Signal Integrity Team at Xilinx since 2011. He worked at NVIDIA, MetaRAM, and Intel/HP before Xilinx. He is extensively involved in power/signal integrity in silicon, package and board design/validation/production. He received his M.S. Degree in Electrical Engineering from Colorado State University and B.S. Degree in Electrical Engineering from Peking University, China.

Introduction

With each new generation of chips, the I/O circuitry is expected to perform at higher frequencies while the supply voltage is being reduced to meet the new aggressive power efficiency targets. As the result, circuits become increasingly sensitive to on-chip power supply noise. Since voltage margins are tight to begin with, even minor variations in the on-chip supply voltage have large detrimental impact on timing. Therefore, the ability to characterize the properties and optimize the performance of the power delivery network (PDN) is crucial for a successful design. As the noise sensitivity of the I/O circuitry has become very high, it is important to consider the PDN noise on a system level, including contributions from the chip, package, and the printed circuit board (PCB) [1], [2].

In this paper we first discuss our general approach to PDN characterization and the metrics we use to capture PDN performance. Then, we provide an overview of our modeling methodology for PDN components and of the PDN system as a whole. Further, we present the results of the simulations performed using our methodology together with the results of laboratory measurements for several FPGA test vehicles. Finally, we demonstrate the correlation of the measurements with our simulation-based predictions. A separate section is dedicated to the topic of PDN impact on system timing.

General Approach to PDN Characterization

A typical system-level PDN representation has four main components (as shown in Figure 1): voltage regulator module (VRM), PCB, package, and silicon (chip).

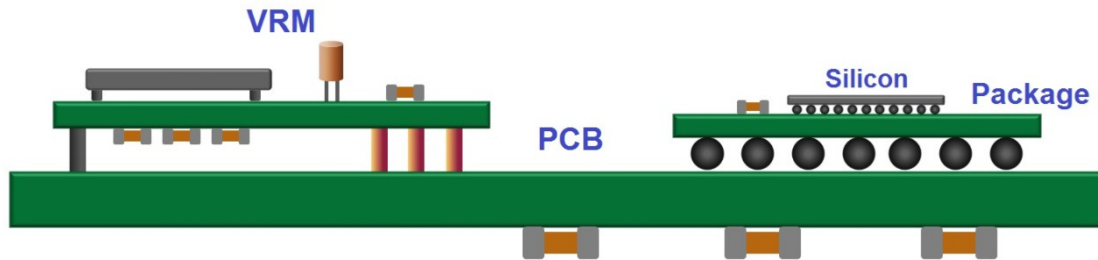


Figure 1. Components of a PDN system

Every time the core chip logic circuitry switches, it creates a transient current that has to come from the external power supply through all the PDN components in Figure 1. Each component of a PDN has certain non-zero impedance associated with it. That impedance causes voltage variations (voltage noise) as the transient current passes through the elements of the power supply. Therefore, we can represent a PDN as a chain of equivalent lumped RLC circuits that correspond to impedances of the PDN components (as shown in Figure 2). The scale of RLC values is very different for different components in Figure 2. If we consider the system behavior in the frequency domain, each component of the PDN contributes to the on-chip voltage noise in different

frequency bands. Equivalently, the on-chip circuits "see" a particular impedance profile that results from the interaction of PDN components. Figure 3 shows the measured impedance profile of one of our test systems.

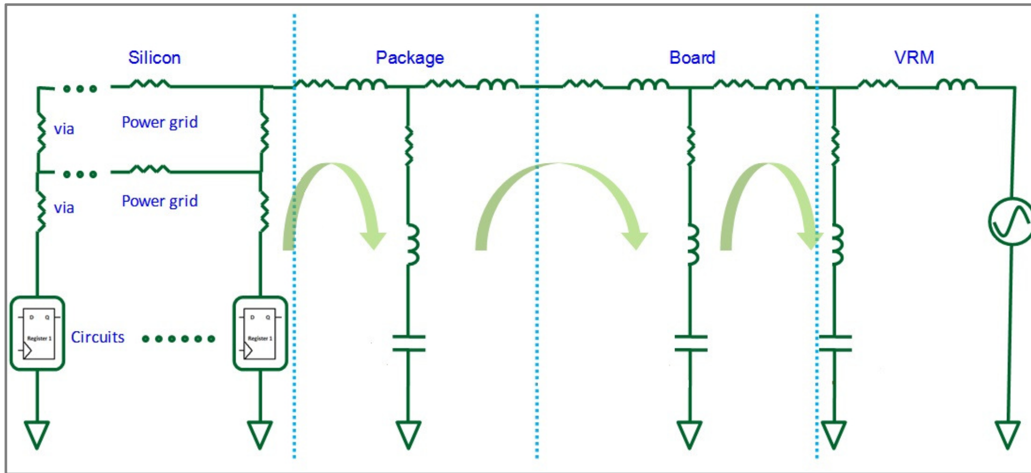


Figure 2. Equivalent circuit representation of a PDN

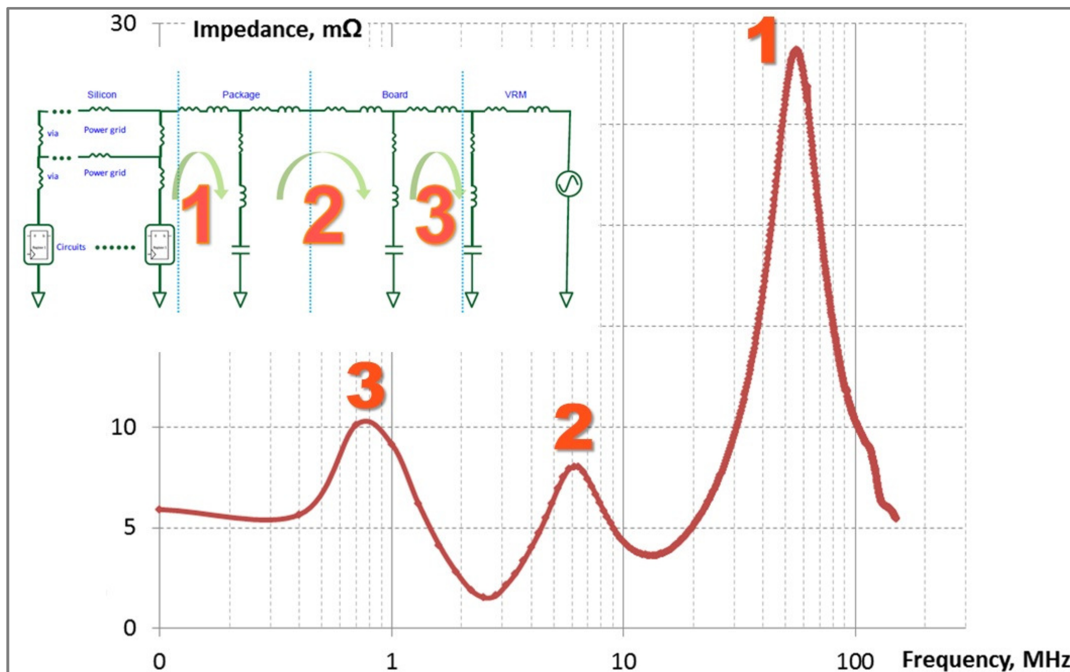


Figure 3. Example of a PDN impedance profile

The profile in Figure 3 has three distinct peaks. The most prominent one (# 1) is around 50 MHz and is caused by the resonance between the on-die capacitance and the inductance of the package. Another peak (# 2) is below 10 MHz and is due to the resonance between on-package decoupling capacitors and the PCB inductance. There is another resonance in the sub-megahertz range that is most likely the result of interaction

of the smaller on-board decoupling capacitors and the combined parasitic inductance of the board PDN components and the VRM.

Impedance profile is a suitable system-level metric of the quality of a PDN. Ideally, such profile should be flat and stay below the target impedance set for the system PDN. If, during a system's operation, there are signals present that generate excitations at the frequencies close to the PDN resonances, the corresponding voltage noise components can be greatly amplified. Impedance profile helps identify potentially problematic frequency ranges. An appropriate choice of the decoupling capacitors can help mitigate PDN resonances. In the worst case, the end user can at least be instructed to avoid certain ranges of operating frequencies.

Another approach to studying the properties of the PDN is the time-domain or transient analysis. When on-chip circuitry goes from idle state to switching, current draw increases and causes a dynamic voltage drop (undershoot) due to the parasitic inductance of the PDN. Figure 4 shows a typical voltage waveform induced by a transient current event on a core logic supply. The magnitude of undershoots and overshoots and the time scale of the waveform in Figure 4 reflect the characteristic properties of a PDN. The first undershoot corresponds to the response of the RLC circuit formed by the on-die capacitance and the package inductance. The magnitude of the first undershoot is commonly used as a design spec for the on-chip and package-level PDN.

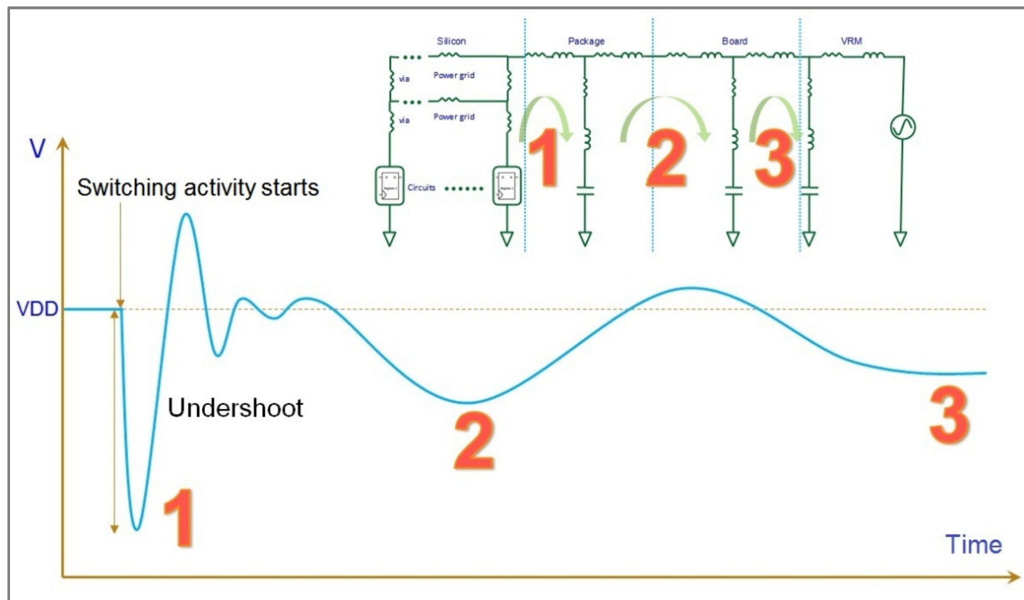


Figure 4. Transient response of a PDN

The amplitude of the waveform in Figure 4 also depends on the amount of circuitry involved in switching, and on the switching frequency. In order to create a spec, one has to determine a reasonable approximation of the worst case utilization and activity without causing overdesign. It has to be noted that there is more than one way to induce the voltage noise and more than one way of probing it. In general, the magnitude and the type

of stimuli, as well as the choice of a probing solution, can all affect the characteristics of the response in Figure 4 and will be discussed in more detail further.

Power supply noise results in variations of signal propagation delay and thus impacts system timing. A common timing uncertainty metric is jitter. The topic of jitter characterization, decomposition, quantification, and correlation is fairly complex. One way to capture the power supply noise impact on timing is to observe phase noise in the system's clock network while the PDN is subjected to various stresses. Phase noise is a frequency-domain value, but it can be transformed into time-domain jitter through integration. Phase noise plot (Figure 5) in itself is a convenient debugging tool that helps identifying PDN-induced jitter and correlating it to other frequency domain and transient PDN characteristics.

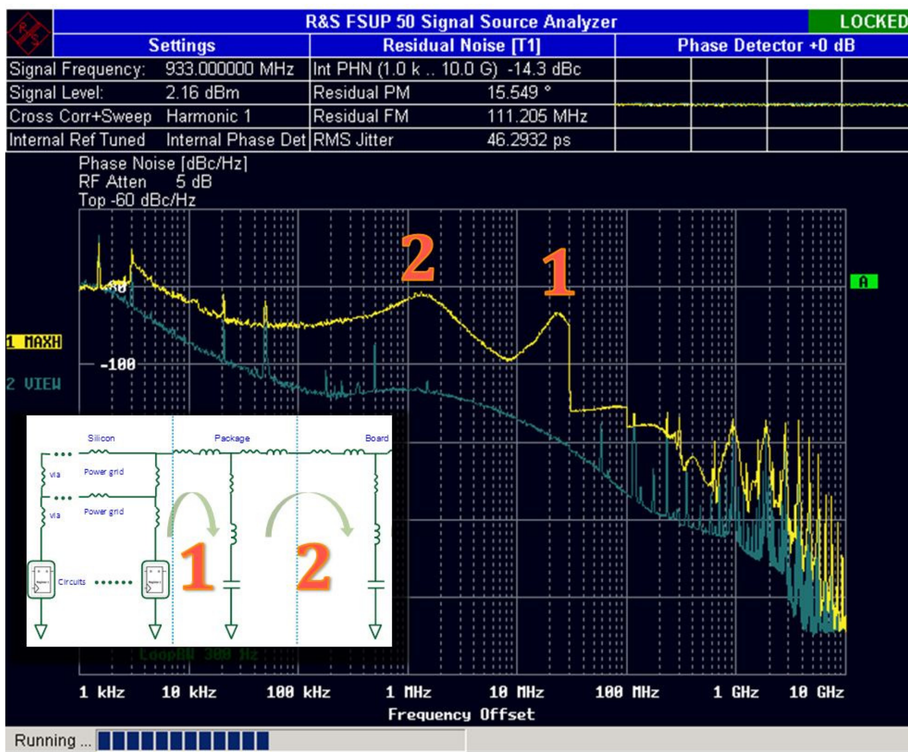


Figure 5. Example of a measured phase noise plot

Figure 5 shows a phase noise plot for a clock signal in one of our test chips. Two traces in the plot correspond, respectively, to the quiet case, when no switching activity is happening; and to the case when the core power supply is stressed by switching of a portion of the logic circuitry. The two peaks denoted on the curve by 1 and 2 correspond to the resonances between the chip and the package; and the package and the board, respectively. The peaks on the phase noise plot correspond to the frequency ranges where the PDN is most sensitive to excitation and the voltage noise values are highest. As the voltage noise increases, so does its impact on timing and hence the clock jitter.

System-Level PDN Modeling Methodology

There are three main parts in our system-level power supply model: board, package, and die. We leave the modeling of a VRM outside of the scope of this paper. Each part of the model contributes to different components of the power supply noise and requires somewhat different treatment. However, the overall approach is based on representing every component with a behavioral (s-parameter) model or a lumped circuit (where appropriate); and on combining the elements into a system-level model that can be used either for small-signal or transient analysis. Figure 6 shows a general setup of a system-level PDN model.

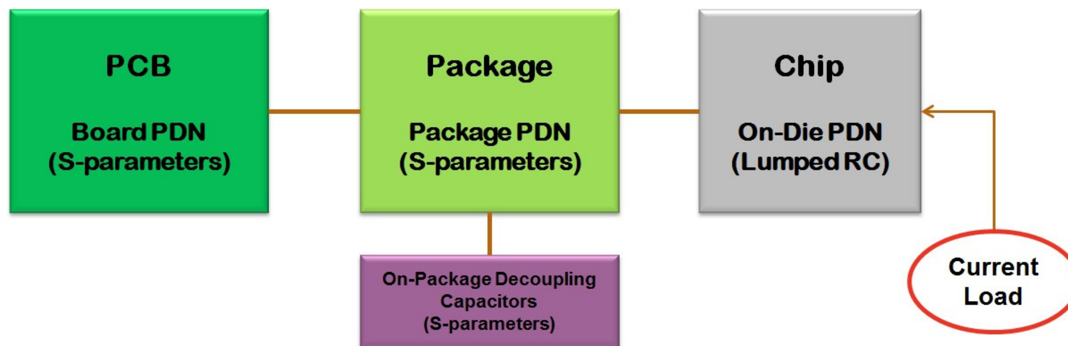


Figure 6. General setup of a system-level PDN model

Small signal analysis produces the frequency-dependent impedance profile of a PDN system as seen by the on-die circuits. Once all elements of the PDN model are in place, the small signal analysis does not require any special setup.

The transient analysis, on the other hand, requires an appropriate transient current load to induce voltage noise in a PDN system. In the subsections below we discuss the current load setup and the details associated with the modeling of system-level PDN components.

A. Current Load Model

Voltage noise in a PDN is induced by a time-variant current created by the switching of the on-chip circuits. In order to model such time-variant current, we can introduce a switching current source. If we want to achieve an accurate representation of the circuit switching activity, we can use a dataset-based current source modulated by the switching profile of the specific circuits. Figure 7 shows the switching profile of a single core logic block. The gain of the source is scaled based on the amount of logic involved in switching.

We can generate a single switching event and obtain the characteristic voltage noise waveform that is essentially the impulse response of the system. Alternatively, we can

create a continuous switching event, a current step. A current step represents a case where a system goes from an idle state to switching.

If we do not need to know the exact noise waveform, or if the switching current profile is not available, a step current load created by a switching profile-based source can be approximated with a simple ideal step source. The magnitude of the step represents the time-average or equivalent DC value of the current load. The comparison of the ideal and the high-frequency switching current steps is shown in Figure 8. Figure 8 demonstrates that the frequency content of an ideal step is very close to that of a switching profile-modulated step at the lower frequencies in the valid frequency range of package and board PDN design. And this ideal step could dramatically simplify the simulation time with reasonable trade-off.

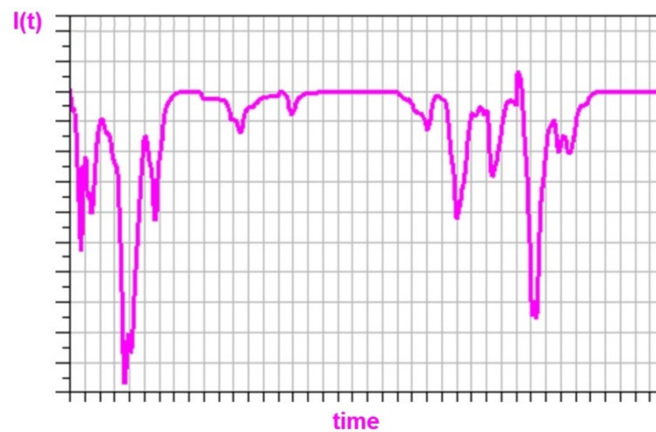


Figure 7. Switching current profile of a sample digital block

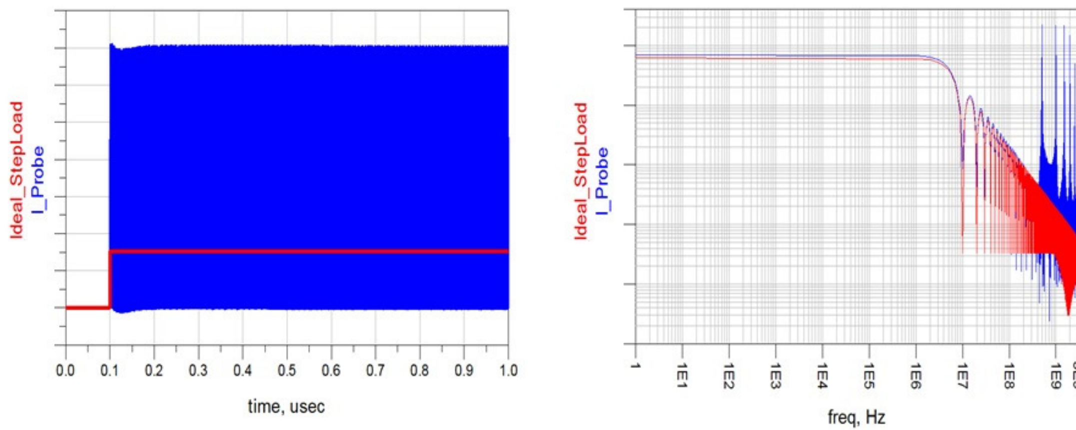


Figure 8. Comparison of an ideal current step load and the realistic one shows that an ideal step closely approximates the energy of the realistic load in the low-frequency range of the spectrum

B. Board Model

Board-level PDN affects the low-frequency power supply noise components. Generally, a PCB model is not required to be extremely accurate. As long as a model reflects the stackup and the dimensions of a board with reasonable accuracy, the exact details of the power routing have little impact on simulation results. It is somewhat more important to add the correct on-board decoupling capacitor solution to the model. In Figure 6, a board model is shown as a single block with the entire decoupling solution embedded, while in some cases we were able to achieve better correlation results by using external equivalent RLC models for larger capacitors.

Typically, we used a 2.5D EDA tool to extract a PCB model from a complete board layout. However, since PCB technology does not change much between generations of silicon devices, such a layout-based model can be used as a starting point for pre-layout "what if" type simulations.

C. Package Model

Package-level PDN is responsible for the mid-frequency components of the voltage noise. Essentially, a package can be treated similarly to a PCB by starting with a layout database and running a simulation in a 2.5D tool to generate an s-parameter behavioral model. However, care should be taken to accurately extract the inductance of a package PDN, since that inductance, together with the on-die capacitance, determines the shape of the most prominent PDN resonant peak. For better accuracy, on-package decoupling capacitors should also be modeled separately (as shown in Figure 6), rather than being embedded inside the package model.

An interesting effect that can be demonstrated with a package PDN model is the distributed nature of the voltage noise. The package model in Figure 6 has only one input and one output port. The die-side port lumps together all power bumps on the top layer of the package. The board-side port represents all BGA balls dedicated to the power supply. Such treatment can result in inaccuracies when chips with large footprints are modeled.

Figure 9 shows an example of a package level core logic PDN layout (top layer) and the corresponding contour map of the simulated power supply voltage undershoot levels. Instead of using a single port for the entire C4 bump field, we divided the die into 25 individual partitions. The results in Figure 9 show that on-package decoupling capacitors help mitigate the voltage noise, but as the distance from the capacitors increases, they become less effective and the noise levels increase. Predictably, the worst noise is observed in the center of the die area. In the simulation we assumed a uniform distribution of the switching circuitry across the die area. In reality it is not the case. The distribution of the switching current becomes close to uniform only at high levels of device utilization. If only a relatively small percentage of logic is utilized in the design, distributed nature of the supply noise can become even more pronounced.

D. Die Model

Equivalent simple RC circuit model is used for the on-die PDN simulation(Figure 6). Distributed RC model could be used too but the complexity grows exponentially. Design trade-off between simulation time and accuracy needs to be made for such modeling, depending on the simulation objectives. While the single equivalent RC model is simple, determining the values of R and C still requires numerous simulations. It is important to establish a reliable methodology flow to extract the correct values of on-die resistance and capacitance. The on-die PDN RC values determine the position and the magnitude of the largest peak in the PDN impedance profile (Figure 3). The system-level PDN model is highly sensitive to the parameters of the on-die power supply model.

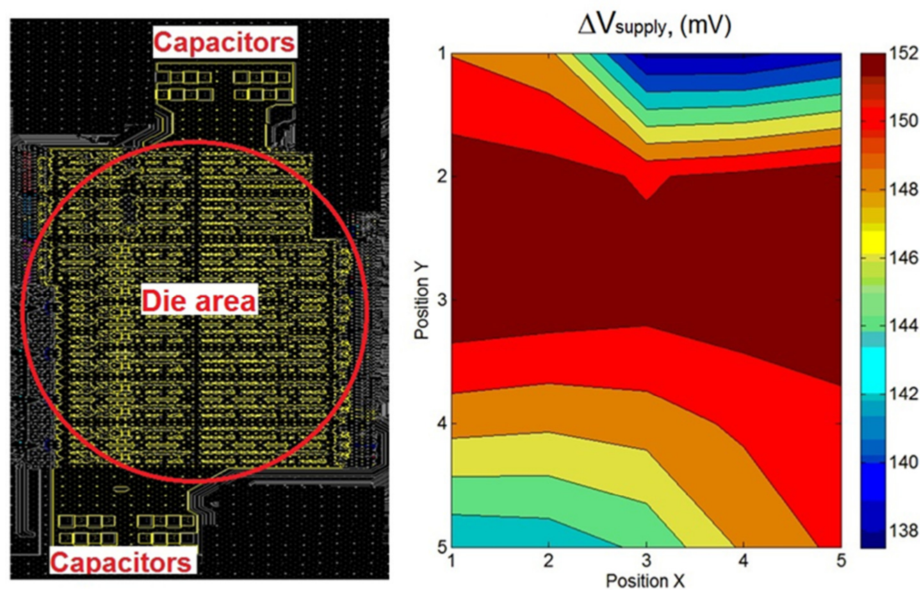


Figure 9. Distribution of PDN noise in a package

Different extraction methodologies are used for different types of circuit blocks, considering the design flow and circuit characteristics. Mixed-signal circuitry could be simulated through HSPICE to extract RC parasitics while digital blocks could be simulated through EDA tools like Redhawk or HSPICE if possible.

Simulation Results

The setup in Figure 6 can be used for both transient and small-signal analysis. In a transient simulation we can observe the time-main voltage noise waveform. The magnitude of the first voltage undershoot is used to determine whether the PDN of the chip/package combination meets the design specifications. The result of the small-signal analysis is the frequency-dependent impedance of the power supply, the impedance profile of the PDN as seen by on-chip circuits. The impedance profile is used to determine if the decoupling solution used in the system is adequate.

A. Transient Analysis

Figure 10 shows different probing locations used in our transient simulation. The largest values of PDN noise are observed at the die level. Power supply noise waveform gets filtered and attenuated in the package. As we discussed earlier, noise levels are location-dependent, and the waveform observed at the package decoupling capacitor location demonstrates that effect.

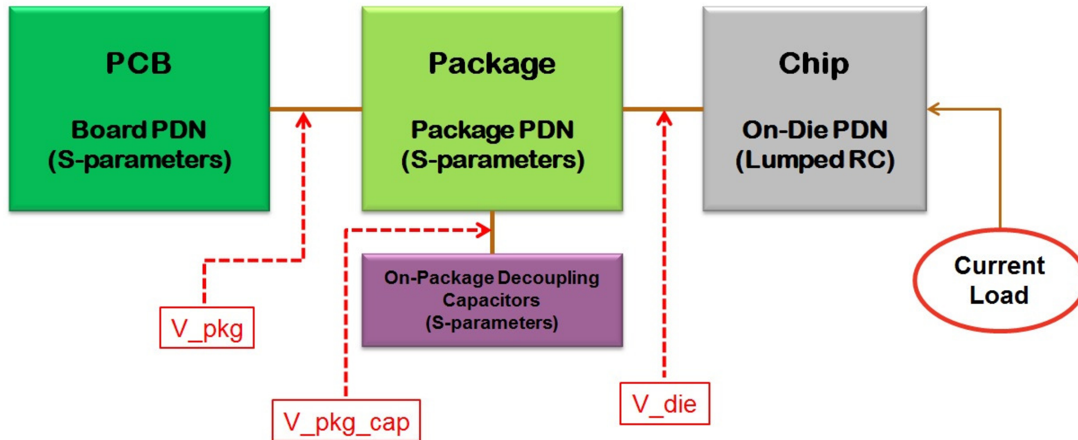


Figure 10. Probing locations in a transient simulation

Figure 11(a) shows the first voltage undershoot waveforms at both the die and package probing points and at the package decoupling capacitor. The model of one of our test systems, System A, is used in the simulation. The simulation is driven by a switching current source based on the core logic switching profile. Probing at a decoupling capacitor terminal produces a significantly attenuated and smoothed waveform.

Figure 11(b) shows results for the same model excited with an equivalent ideal current step. We can see from Figure 11 (b) that an ideal current step provides a good approximation of the switching current load. If we measure the distance between the first and second minima in the Vdie waveform, we obtain the value of 23.5 ns. We can then estimate the die/package resonant frequency that causes the first undershoot as 1/23.5 ns, which is 42.6 MHz. So we would expect to see a resonant peak in the impedance profile of System A somewhere around 43 MHz.

B. Small Signal Analysis

In Figure 12, impedance profiles of two different test systems are shown. System A and B have unique combinations of chip, package, and PCB. The biggest difference is in the sizes of the chips: the chip in system B has a significantly larger die. Boards and packages in both systems are manufactured using the same technology (both packages are flip chip) and have similar material composition and architecture.

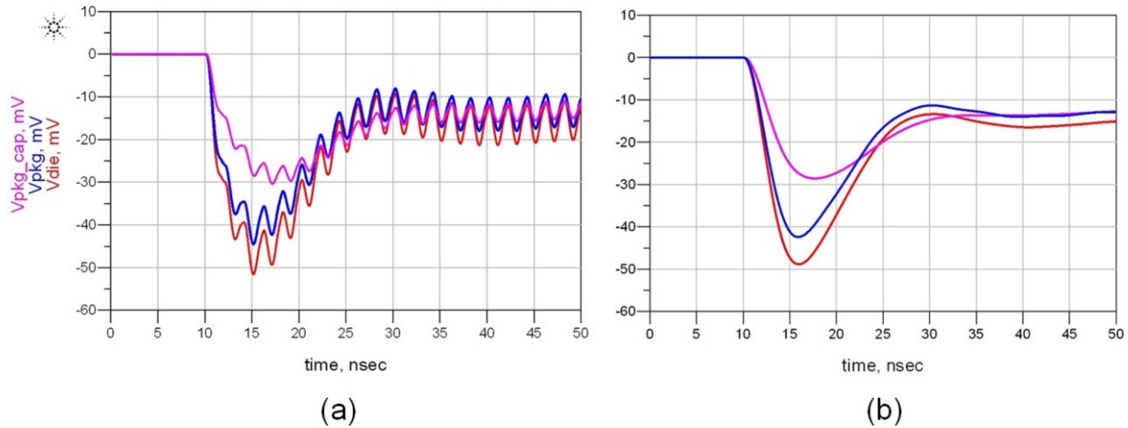


Figure 11. Simulated PDN step response of System A with a switching current source (a) and with an equivalent ideal current step (b)

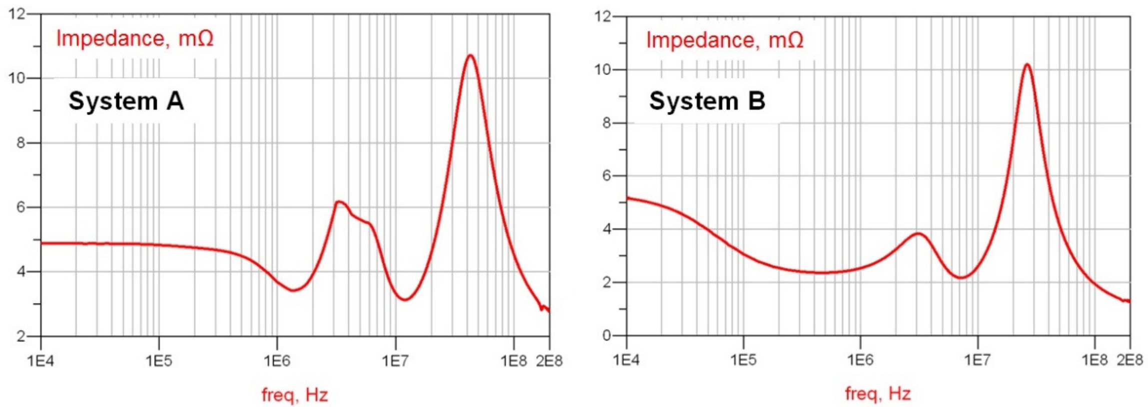


Figure 12. Simulated impedance profiles of two test chips

From Figure 12 it appears that System A has a less than ideal PCB-level decoupling solution. Both systems exhibit fairly large die/package PDN resonances between 10 MHz and 100 MHz. System A has a PDN resonance at 43 MHz. System B has a larger die size and hence a higher value of on-die capacitance. Therefore, PDN in System B resonates at the lower frequency of 26 MHz.

Measurements and Correlation

Similar to the modeling methodologies, measurements fall into two categories: time-domain characterization, and frequency-domain measurements. Additionally, the approaches to measurement and the treatment of the results both depend on the choice of the probing solution.

A. Probing Solutions

Since ultimately we are concerned with the performance of on-chip circuits, ideally we would want to measure PDN characteristics directly at the die level. That, however, is not easy to achieve. Figure 13 demonstrates that it is possible to set up an on-die probing solution for a device in a wire bond package (System C). In the case of a wire bond package, on-die probing is also the only good way of characterizing the on-chip PDN. Bond wires act as low-pass filters for power supply noise; therefore, a probing solution needs to bypass these wires in order to obtain a useful, undistorted sample of the noise waveform. The setup involves a chip with an exposed die and a micro probe station (Figure 13).

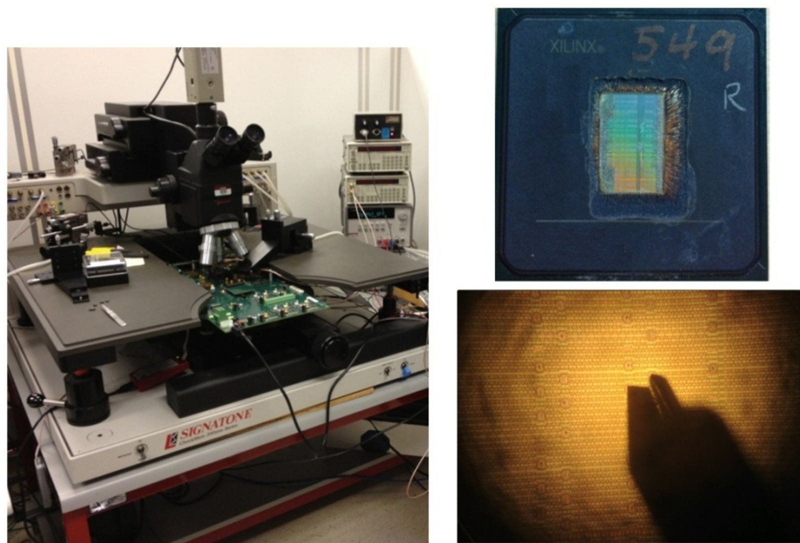


Figure 13. On-die probing solution for a wire bond device (System C)

The on-die probing solution that we use for our wire bond test cannot be applied to the majority of the devices as they are manufactured using the flip chip packaging technology. Figure 14 demonstrates the other two probing options that we use in our measurements: the package probe and the "spy hole". Package-level probing is the best we can do in terms of proximity to on-die circuitry. Dedicated probing points have to be implemented in a package design to provide access to the power supply of interest. Microcoaxial cables can then be used to connect on-package probing points to landing pads on a PCB. Package-level probing allows observing the high-frequency components of the voltage noise waveform. However, the magnitude of the noise measured at the package probe location only reflects the noise level at the edge of the power plane.

A more robust solution, one that does not require complex rework and additional probing features, is the so-called "spy hole." For a "spy hole," one dedicated pair of power and ground BGA balls is routed out to connectors on a PCB. A "spy hole" does not require additional rework and allows measurement of the voltage noise close to the center of the

die area. The downside of a “spy hole” solution is that a transient noise waveform is filtered by a package and its high-frequency content is lost.

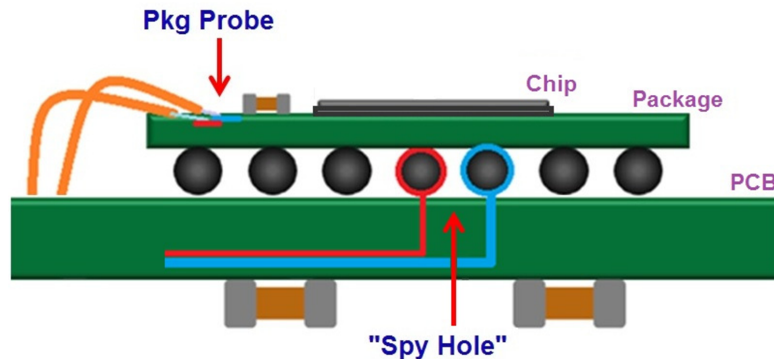


Figure 14. Different probing solutions

B. Time-Domain Characterization

As we discussed previously, PDN voltage noise can be induced by creating a transient current event. Throughout this paper we use a core logic supply as an example of a PDN system. In order to observe the characteristic PDN voltage noise waveform in a core logic supply, we need to create a transient current in the core logic circuitry (fabric). It is fairly easy to do in an FPGA device. We can program the desired percentage of the fabric to switch, and trigger the switching with an external signal source. In this way, we can start or stop the switching activity at will, as well as control the magnitude and the frequency of the transient current.

Figure 15 shows a screen capture from a real-time oscilloscope. Channel 3 displays the switching activity of the logic circuitry, while Channel 4 displays the corresponding transient voltage waveform induced in the core PDN. Effectively, we create a current step by triggering high-frequency switching of the core logic and observe a voltage undershoot induced by that current step.

The waveform in Figure 15 is measured in System C (the one with a wire bond chip). The signal in Channel C4 comes from the micro probe placed directly on the die (Figure 13). The switching is driven by a clock signal. Only twelve percent of the fabric is switching.

Figure 16 shows the correlation between the measured and the simulated waveforms. In the simulation, the noise waveform is sampled at the on-die probing point (Figure 10). The waveforms in Figure 16 align reasonably well. Based on the time-scale of the first voltage undershoot, we can tell that the die/package resonance happens around 14 MHz.

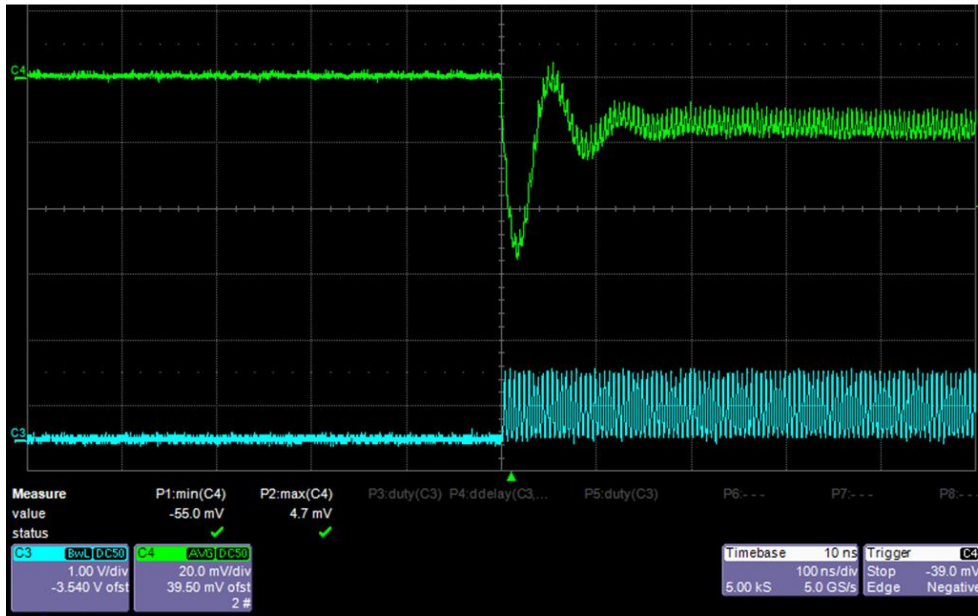


Figure 15. Measured PDN transient step response of System C

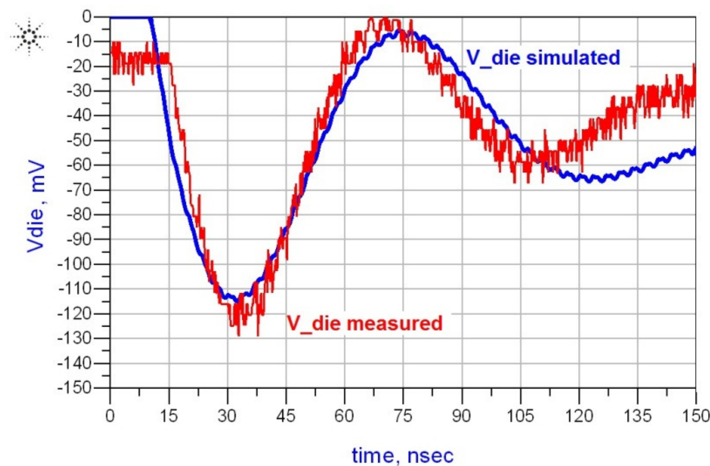


Figure 16. Measured and simulated PDN noise waveforms in System C

In Systems A and B (flip chip packaging), we do not have the option of direct on-die noise probing. Instead we rely on package-level probing points and on the "spy hole" probing solution (Figure 14). We can use System A to demonstrate the differences between the two probing options. In Figure 17, the transient step response of System A, measured with a package probe, is overlaid with the same waveform measured at a "spy hole" location.

Figure 17 shows that the magnitude of the first voltage undershoot measured at the "spy hole" is significantly higher than the one measured with a package probe. This result is in line with our earlier discussion of the distributed nature of the voltage noise.

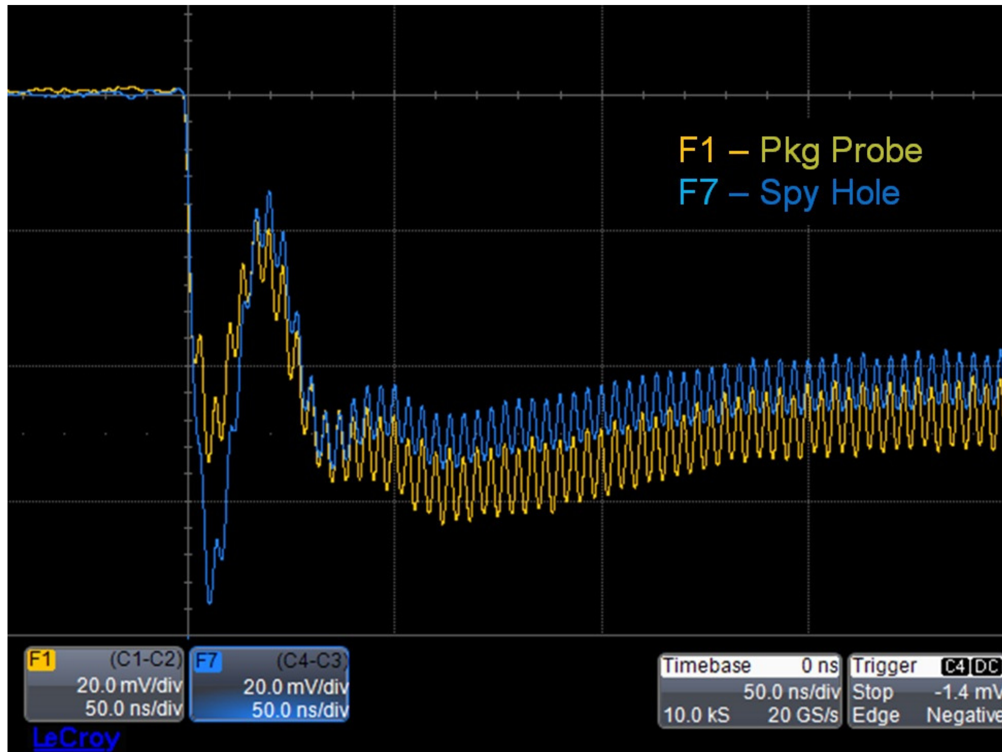


Figure 17. PDN transient step response of System A measured at the package probing point and at the "spy hole"

We also expect to see a difference in the frequency content of the noise waveform between the two probing locations. In order to observe the high-frequency noise components, we can look at the impulse response of the PDN system (the way the PDN responds when the logic circuits are switched only once). Figure 18 shows impulse response waveforms of System A measured at two different probing points.

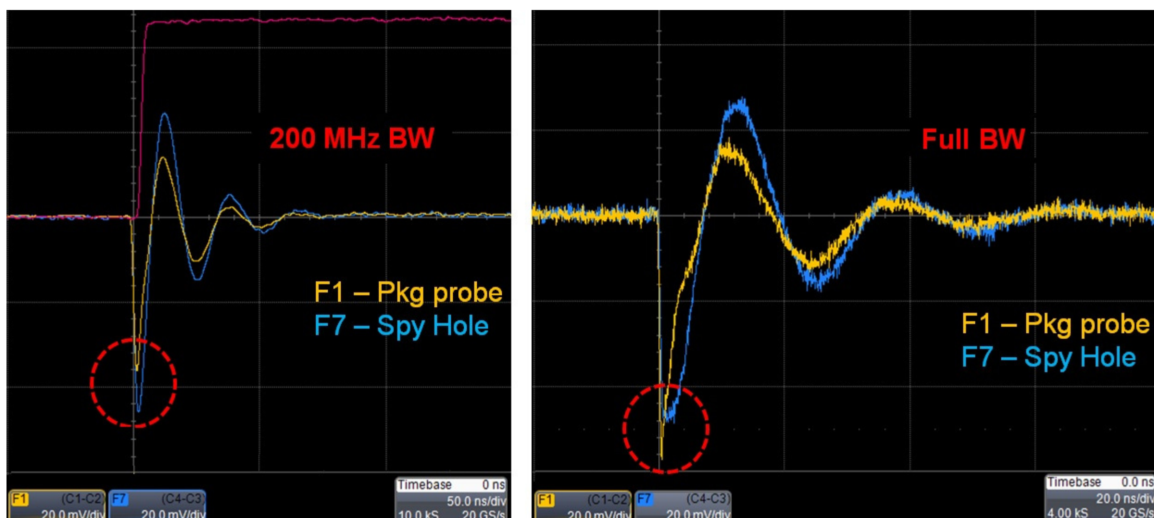


Figure 18. PDN impulse response of System A measured at a package probing point and at the "spy hole"

On the left panel of Figure 18, the impulse response waveforms are filtered by limiting the scope channel bandwidth to 200 MHz. When the 200 MHz filter is applied, we see that the magnitude of the waveform measured at the "spy hole" location is larger at all times. However, when the bandwidth is not limited (screen capture on the right panel of Figure 18), we are able to see the high-frequency spike in the first undershoot of the package probe waveform that is not present in the "spy hole" trace. The high-frequency component measured with the package probe actually exceeds the undershoot captured at the BGA level.

Figure 19 shows the correlation between the measured PDN step response and the simulated one. We use the data from the "spy hole" measurement and capture the simulated waveform at the package probing point in Figure 10. Both waveforms are filtered with a 200 MHz low-pass filter. Figure 18 shows that the simulated step response is reasonably close to the measured one.

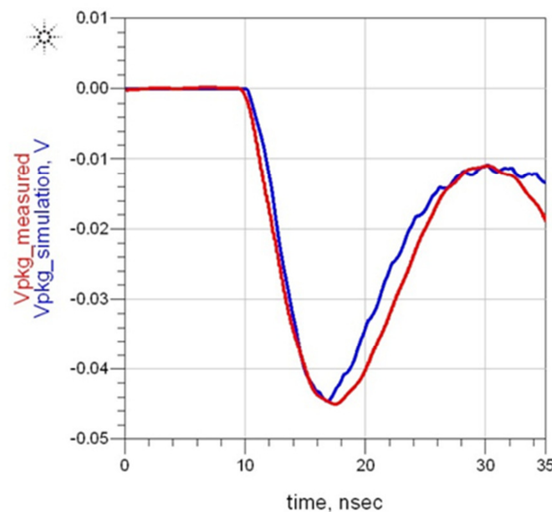


Figure 19. Measured and simulated PDN noise waveforms in System A

So far we only considered power supply voltage undershoots caused by rapid increases in current consumption due to the switching activity of on-chip circuits. Another power supply voltage transient event happens when the switching activity stops abruptly and the current draw decreases. At the end of the switching activity burst the inductive properties of a PDN cause a voltage overshoot. Figure 20 shows the complete sequence of events: the switching activity starts and the voltage undershoots, the switching continues and the voltage level stabilizes, finally, the switching stops and the voltage overshoots. Figure 20 also demonstrates that the board-level bulk decoupling solution and the VRM in System A are poorly balanced The peak values of the waveform in Figure 20 are not caused by the first voltage undershoot associated with the chip/package resonance (the first undershoot can hardly be seen in the figure because of the large time scale). The large voltage undershoots in Figure 20 are the result of the board-level PDN and the VRM resonances. These undershoots correspond to the 3rd voltage droop in Figure 4 and occur in the frequency range of several hundreds of KHz.

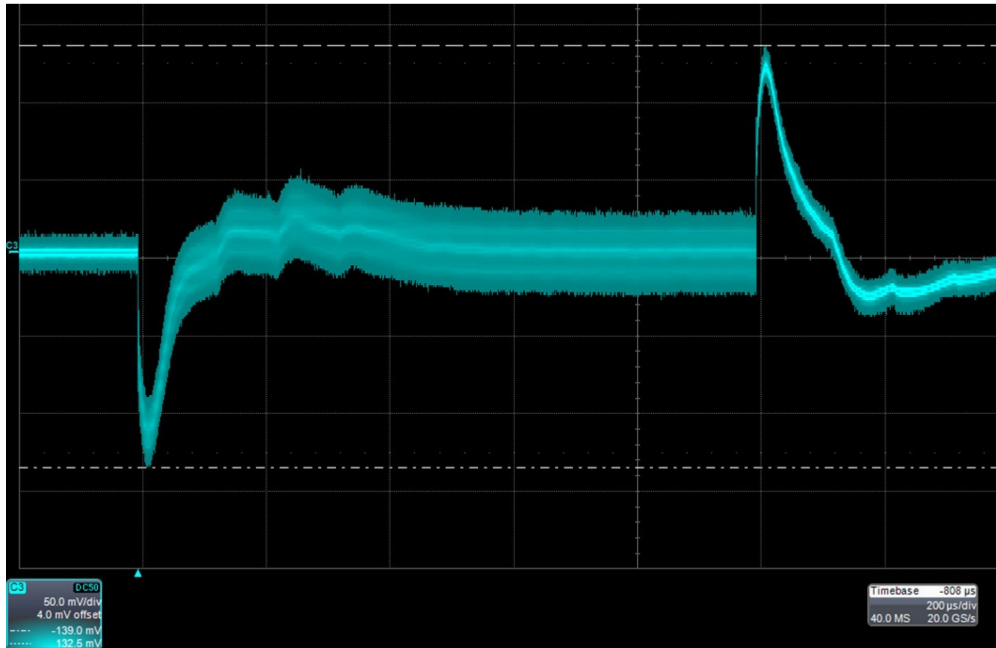


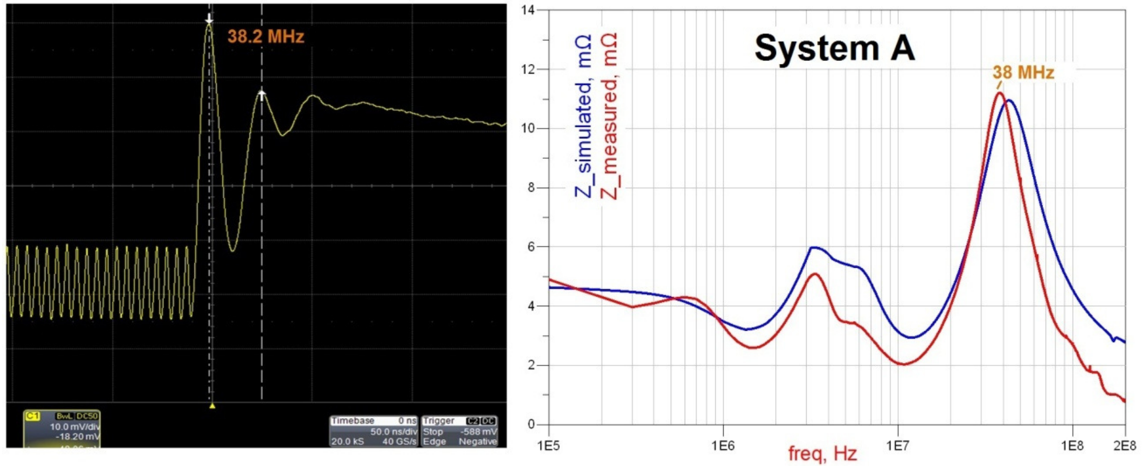
Figure 20. PDN voltage undershoot and overshoot in System A

C. Frequency-Domain Measurements

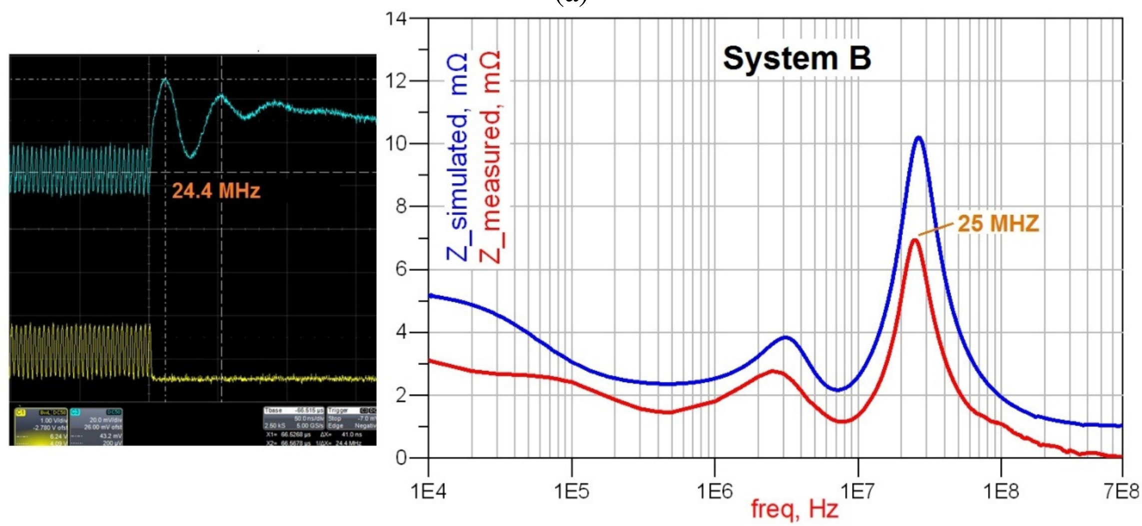
We use the frequency-dependent impedance of a PDN as the frequency-domain characteristic of a power supply system behavior. The impedance profile of a PDN as seen by on-chip circuits is a design metric: impedance must stay below a specified target. The impedance profile is used to guide the design of a decoupling capacitor solution.

It is relatively easy to model the impedance of a PDN. However, it is simply impossible to measure the impedance of an active system directly. We have to derive impedance values from other measurements using our in-house technique. The indirect nature of the technique makes it somewhat more sensitive to measurement errors. To remedy this, we combine two correlation approaches to validate our results. First, we obviously want to see a reasonable match between the simulation results and the measurement. Additionally, we know that the impedance profile of a PDN system shapes the transient response of that system. Thus, we expect to see a correlation between the measured transient voltage noise waveform and the impedance profile.

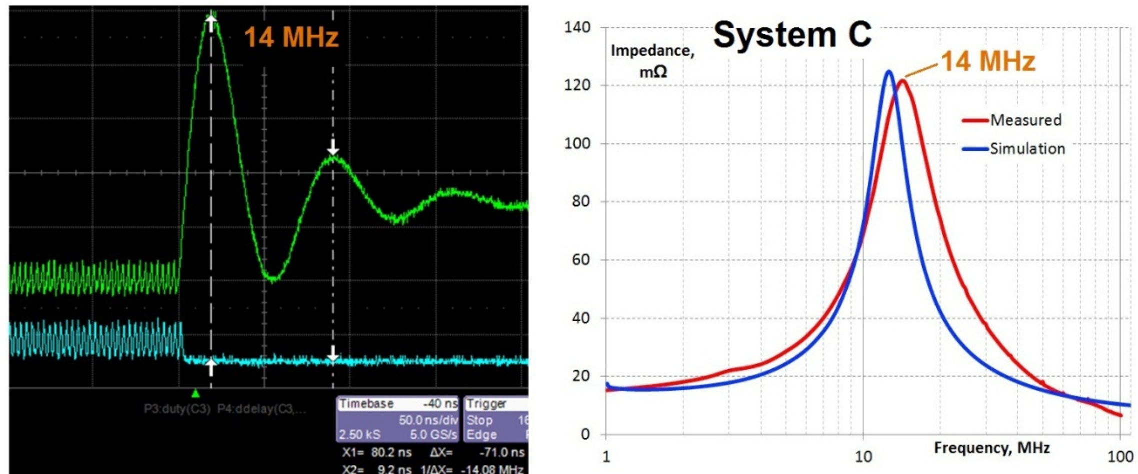
Figure 21 shows measured and simulated impedance profiles of the three test systems together with the corresponding transient voltage noise waveforms. We used voltage overshoot waveforms to measure the time scale of the chip/package resonance. It is convenient to use an overshoot waveform for correlation (rather than an undershoot), as it does not have the high-frequency switching noise riding on it.



(a)



(b)



(c)

Figure 21. Measured impedance profiles of the three test systems and their correlation with the time-domain measurements and simulation results

From Figure 21 it is evident that the estimate for the chip/package resonance frequency obtained from the time-domain measurement matches very well with the impedance profile in all cases. We observe reasonable correlation between the measured and the simulated PDN impedance profiles. The PDN impedance profile of System C has only one peak; this is expected since there are no on-package decoupling capacitors in System C.

PDN Impact on Jitter

The topic of PDN-induced jitter measurement, analysis, and decomposition is fairly complex. There are a number of papers entirely dedicated to the subject [3], [4]. To limit the scope of our discussion for the purposes of this paper, we only consider frequency domain techniques for jitter characterization. Although jitter is a measure of timing uncertainty, it can be characterized in the frequency domain. Timing jitter of the clock in the time domain generates phase noise in the frequency domain [5]. We utilize phase noise measurements to demonstrate the way in which PDN noise can affect clock signals in a system, and how PDN contribution to jitter can be correlated with system properties.

Our measurement setup consists of a clock path and a block of core logic circuitry. The clock input comes from an external clock source. The core logic is triggered by a separate external signal source. On-chip clock management circuitry is supplied by the same core PDN as the logic. Thus, the supply voltage noise induced by the switching logic affects the propagation delay of the clock signal. Timing variations in the clock signal at the output of the system translate into the phase noise in frequency domain. The phase noise is measured with a signal source analyzer.

Up to this point we only used clock signals to drive the switching activity of the core logic in our measurements. Clock-driven switching of the fabric circuitry produces a targeted narrow-band excitation of the core PDN. In real customer applications, the logic switching is driven by data traffic. Data patterns produce a wide-band random excitation of a PDN. To mimic realistic data traffic and to obtain a PDN response across a wide range of frequencies, we use PRBS patterns to drive the switching activity. Figure 22 shows the comparison between the spectra of a clock and PRBS signals.

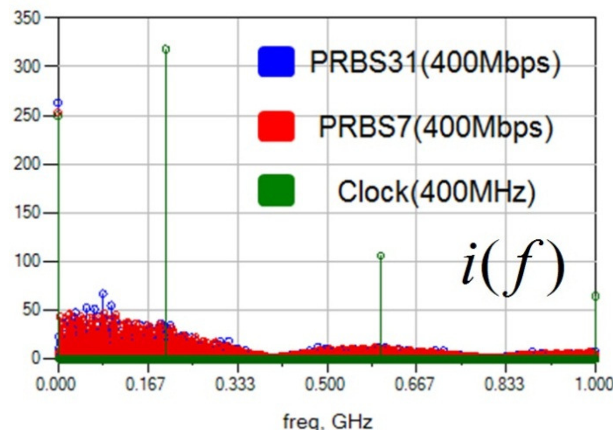


Figure 22. Spectral content of a clock signal and two PRBS patterns

Figure 23 shows phase noise plots of a 933 MHz clock signal at the output of System A. In Figure 23, trace 2 corresponds to the case of fabric switching being driven with a clock pattern. In trace 2, phase noise mainly appears in peaks around separate frequency offsets that correspond to the source frequency and the harmonics of that frequency.

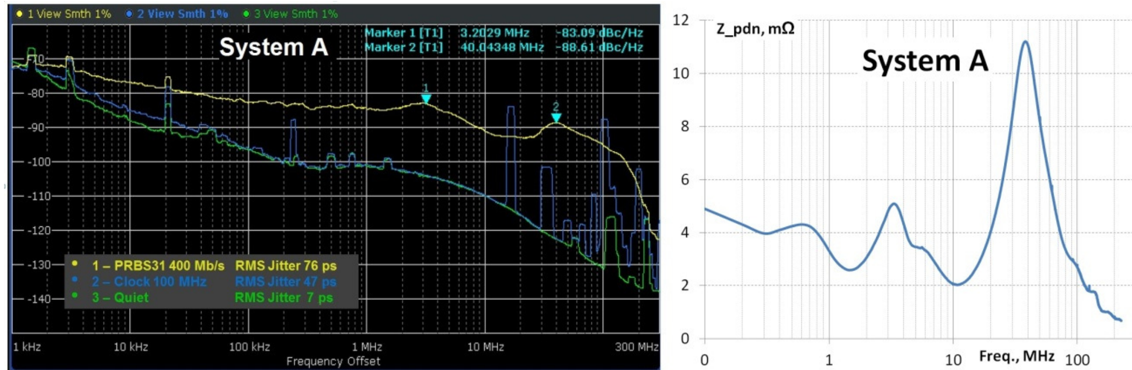


Figure 23. Phase noise plot of a 933 MHz clock signal in system A and a corresponding measured core PDN impedance profile

Trace 1 in Figure 23 corresponds to the case when the noise inducing circuitry is switching with PRBS31 pattern. Such broad-band excitation results in a much higher overall level of phase noise and a high RMS value of jitter.

Jitter can be calculated using the following equation:

$$\left(\int i(f) \bullet z(f)df\right) \times JitterSensitivity \Rightarrow jitter$$

Thus, jitter is the product of the switching current, the PDN impedance, and circuit sensitivity to jitter. When a PRBS pattern is used, the switching current has a wide-spread spectrum with many components at the lower frequencies. Circuit jitter sensitivity function has a low-path shape. Finally, PDN impedance is low in the frequency range above 100 MHz. It is expected, then, that PDN noise contribution to jitter is largest at the frequencies below 100 MHz. We can also note that the two peaks in Trace 1 in Figure 23 occur at the frequency offsets that correspond to PDN resonance frequencies in the impedance profile of the system. The same pattern can be observed in the phase noise plot for the clock signal in System B (Figure 24).

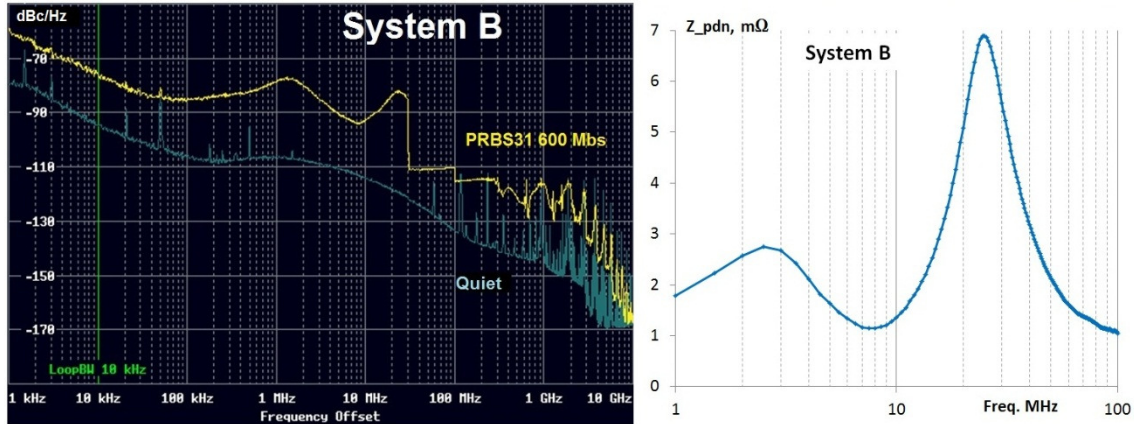


Figure 24. Phase noise plot of a 933 MHz clock signal in system B and a corresponding measured core PDN impedance profile

Summary and Conclusions

The comprehensive methodology of system-level PDN characterization outlined above allows considering all levels of power supply simultaneously, which makes it a robust tool to guide PDN design. This methodology brings together time- and frequency-domain techniques in order to create a complete, accurate representation of the power supply network. Our results show good correlation between time- and frequency-domain measurements; moreover, those results match well with our simulation-based predictions. These factors make this system-level PDN characterization methodology an efficient instrument of chip, package, and board co-design.

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