

Extended Spartan-3A Family Optimized for Lowest Total Cost

		Part Number	XC3S50A	XC3S200A	XC3S400A	XC3S700A	XC3S1400A	XC3SD1800A	XC3SD3400A
Logic Resources	System Gates ⁽¹⁾	50K	200K	400K	700K	1400K	1800K	3400K	
	Slices ⁽²⁾	704	1,792	3,584	5,888	11,264	16,640	23,872	
	Logic Cells	1,584	4,032	8,064	13,248	25,344	37,440	53,712	
	CLB Flip-Flops	1,408	3,584	7,168	11,776	22,528	33,280	47,744	
Memory Resources	Maximum Distributed RAM (Kbits)	11	28	56	92	176	260	373	
	Block RAM Blocks	3	16	20	20	32	84	126	
	Total Block RAM (Kbits)	54	288	360	360	576	1,512	2,268	
Non-Volatile Capability	Single Chip Option	Yes	Yes	Yes	Yes	Yes	No	No	
	User Flash (Kbits) ^(3,6)	627	3,054	2,380	5,779	12,251	—	—	
Clock Resources	Digital Clock Managers (DCMs)	2	4	4	8	8	8	8	
I/O Resources	Maximum Single Ended I/Os	144/108 ⁽⁶⁾	248/195 ⁽⁶⁾	311	372	502	519	469	
	Maximum Differential I/O Pairs	64/50 ⁽⁶⁾	112/90 ⁽⁶⁾	142	165	227	227	213	
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, PCI 3.3V 64bit/66MHz, PCI-X 3.3V, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25 & 33, LVPECL25 & 33, Mini-LVDS25 & 33, RSDS25 & 33, TMDS33, PPDS25 & 33							
Embedded Hard IP Resources	Multipliers/DSP48A Blocks	3/0	16/0	20/0	20/0	32/0	0/84 ⁽⁴⁾	0/126 ⁽⁴⁾	
	Device DNA Security	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Speed Grades	Commercial	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	
	Industrial	-4	-4	-4	-4	-4	-4 ⁽⁵⁾	-4 ⁽⁵⁾	
Configuration	Configuration Memory Bits (Kbits)	0.4	1.2	1.9	2.7	4.8	8.2	11.7	
Package ⁽⁷⁾		Size	Maximum User I/Os						
VQFP Packages (VQ): very thin QFP (0.5 mm lead spacing)									
VQ100	16 x 16 mm	68	68						
TQFP Packages (TQ): thin QFP (0.5 mm lead spacing)									
TQ144	22 x 22 mm	108 ⁽⁸⁾							
FGA Packages (FT): wire-bond fine-pitch thin BGA (1.0 mm ball spacing)									
FT256	17 x 17 mm	144	195 ⁽⁸⁾	195	161	161			
Chip Scale Packages (CS): wire-bond chip-scale BGA (0.8 mm ball spacing)									
CS484	19 x 19 mm						309 ⁽⁵⁾	309 ⁽⁵⁾	
FGA Packages (FG): wire-bond fine-pitch BGA (1.0 mm ball spacing)									
FG320	19 x 19 mm		248	251					
FG400	21 x 21 mm			311 ⁽⁸⁾	311				
FG484	23 x 23 mm				372 ⁽⁸⁾	375			
FG676	27 x 27 mm					502 ⁽⁸⁾	519	469	

Notes: 1. System Gates include 20%-30% of CLBs used as RAMs 2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic 3. User Flash is the space left in the on-chip Flash after a portion is used to store configuration bitstream 4. Integrated in the DSP48A slices (Advanced Multiply Accumulate element) 5. The L low-power option is exclusively available in CS(G)484 package and Industrial temperature range 6. Spartan-3AN only 7. All products available Pb-free and RoHS-Compliant, check datasheet for Pb package availability 8. Single chip non-volatile option available for this package