Jump Start Your Design with the Artix® UltraScale+™ Development Platform – Webinar Q&A

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1. What is the availability across the device portfolio?

   As of February 2022, the AU25P and AU20P devices are in production, and the smaller AU10P and AU15P are entering production with pre-production parts now shipping. Contact your local sales representative for device pricing and availability.

2. Does FrontPanel SDK support Linux?

   FrontPanel SDK does support Linux. You can read more about the SDK at https://docs.opalkelly.com/fpsdk

3. Can you provide resources on how to build MicroBlaze with Artix-7 and Artix UltraScale+ FPGAs?

   You can view this webinar where we discuss MicroBlaze™ IP and demonstrate how to implement it on an evaluation platform. Though the target device is a Spartan®-7 FPGA, the flow is effectively the same for Artix®-7 and Artix UltraScale+™ FPGAs. Also view the stand-alone “Hello World” Demonstration of MicroBlaze, based on the MicroBlaze Quick Start Guide. More information can be found on the MicroBlaze web page.

4. Can you support more than two transceiver connectors on a board like this?

   Each TXR4 SYZYGY port on the XEM8320 fully populates a transceiver bank. There are three banks on the AU25P. The two TXR4 ports on the XEM8320 populates two of them, the third is populated by SFP and SMA.

5. Do you have a reference design with a MIPI CPHY interface?

   The Opal Kelly Camera Reference Design uses the MIPI CSI-2 Rx Subsystem IP. This port will become available in the coming weeks. Keep watch at the following for when this port is released: https://docs.opalkelly.com/camera/release-notes/

6. When will the SZG-PCIEX4 PCI Express x4 host adapter card (Opal Kelly) be available to purchase?

   Please reach out to support@opalkelly.com for more information.

7. How do I access the Xilinx Power Estimator (XPE) for Artix UltraScale+ FPGAs?

   XPE is available via lounge access only. If you don’t have access to the Early Access lounge, contact your local sales representative. A new tool is planned for the Vivado® 2022.1 release.

8. What IP cores support HDMI 2.1 and DisplayPort? Do they require additional licenses?

   Video DisplayPort 1.4 RX/TX Subsystem and Video DisplayPort 1.4 RX/TX Subsystem IPs. AT the time of the webinar (Feb ’22), HDMI 2.1 are in BETA status for Artix UltraScale+ devices. You can view these IPs from the IP Catalog.

9. Is the MIPI core using the gigabit transceivers or normal fabric (soft core)?

   Standard MIPI interface based on SLVS uses high-performance I/O (HPIO) up to 2500Mb/s in Artix UltraScale+ devices. SLVS-EC MIPI interfaces use the gigabit transceivers. Visit the MIPI Connectivity page for more information on MIPI support for our FPGAs and adaptive SoCs.

10. If 8 pins are at 16GHz per SYZYGY transceiver, does that mean it’s 8 ports?

    Each TXR4 SYZYGY port on the XEM8320 fully populates a transceiver bank—that being the four lanes of the bank. There are three transceiver banks on the AU25P. The two TXR4 ports on the XEM8320 populates two of them, the third is populated by SFP and SMA.

11. Is there a license for Vivado 2021.2 included in the kit?

    You can download Vivado ML Standard Edition free from: https://www.xilinx.com/support/download.html

12. Will there be a version of the Opal Kelly FrontPanel running over PCIe?

    Opal Kelly will be evaluating this. If we release a PCIe® compatible FrontPanel, it will be listed under the following in time: https://docs.opalkelly.com/fpsdk/release-notes-5-x/. For the time being FrontPanel is USB.

13. The camera reference design seems to support one camera, but you mention four cameras?

    A 3 MIPI camera design utilizing the SZG-MIPI-8320 will become available in the coming weeks. This port will use 3 Digilent MIPI PCAMs at one time. At this time, only a one SZG-Camera port is available for the XEM8320. A multiple SZG-Camera port will also become available for the XEM8320 in the coming weeks.

14. Are SerDes on Artix UltraScale+ FPGAs the same as on Kintex UltraScale+?

    The Artix UltraScale+ FPGA uses the same gigabit transceiver IP blocks found in the other UltraScale+ families.

15. Can KCU116 be used for prototyping?

    Yes, the KCU116 Evaluation Kit is a good approach to prototyping for Artix UltraScale+ devices, given the same fundamental architecture with Kintex® UltraScale+ FPGAs. Another advantage is KCU116 has FMC connectors if those are desired.

16. What is the difference between Zynq UltraScale+ and Artix UltraScale+ devices?

    Zynq UltraScale+ devices offer dual/quad Core Arm® Cortex®-A53 and Cortex-R5F processors. You can refer to the UltraScale+ FPGA product selection guide for more details: https://www.xilinx.com/support/documentation/selection-guides/ultrascale-plus-fpga-product-selection-guide.pdf

17. On the XEM8320, are the maximum number of bits available for partial reconfiguration?

    We use the SelectMAP in the FrontPanel firmware, so that cannot be used. You can use external JTAG for partial configuration. And of course you can inspect the XEM8320 redacted schematics for more information: https://docs.opalkelly.com/xem8320/specifications/

18. Is there new JESD204B or 10G Ethernet IP that is free?

    The JESD204B core is not free. 10GBASE-R is free on all devices. 10GEMAC, FEC, AN/LT are free components.

19. Does Xilinx plan to make a SOM like K26 for the Artix UltraScale+ FPGA?

    As of this writing, Opal Kelley is currently developing the XEM8310-AU25P SOM based on the Artix UltraScale+ AU25P device. Stay tuned.

20. Is the Vitis™ Unified Software Environment supported?

    Yes. You can download both Vivado and Vitis tools at https://www.xilinx.com/support/download.html

21. Are there any adapter boards for SYZYGY-to-FMC?

    Opal Kelly doesn't currently produce a SYZYGY-to-FMC adaptor. This adaptor wouldn't fully populate FMC as the pin count on SYZYGY is less. But there could be value is a partially populated FMC adaptor. We will bring it up to the team at Opal Kelly.

22. Can we purchase the XEM8320 now?

    Yes. You can purchase the XEM8320 now: https://opalkelly.com/products/xem8320/

23. Why only PCIe Gen4x2? Aren't there plenty of transceivers capable of x4, x8, etc.?

    Artix UltraScale+ devices can go up to Gen4 x8.

24. Do transceivers Artix UltraScale+ FPGAs support USB 3 signaling?

    No. Zynq UltraScale+ MPSoC offers USB 3.0 support.

25. What is the max bandwidth of LVDS using regular I/O pins (not transceivers)?

    Up to 2G as referenced in the DC and AC Switching characteristic data sheet:
    https://www.xilinx.com/support/documentation/data_sheets/ds931-artix-ultrascale-plus.pdf

26. CoaxPress 2.0 cores need transceivers in the PL not only in the PS. Are these available?

    Yes. Note that Artix UltraScale+ FPGAs do not have a processing subsystem (PS)—these subsystems are only in our adaptive SoCs (e.g., Zynq SoCs, Versal® ACAPs).

27. Is JTAG still used for internal logic analyzers (ILAs)?

    Yes. JTAG is used for ILA and debug and is supported on the Artix UltraScale+ FPGA.

28. Why am I not seeing the questions that the presenter is addressing here in the question box (during the webinar)?

    The questions are only sent to the presenters, we will be sending an FAQ document to all attendees shortly.

29. If I need more USB ports, do I need to use another SYZYGY port?

    The USB port on the XEM8320 is exclusively for the FrontPanel interface. It cannot be used elsewhere. You could create a USB SYZYGY peripheral if you require.

30. For the camera design, is there a distance from the SYZGY connector the cameras should be mounted?

    We have not tested distances from the carrier with the Camera Reference Design. This is a valid point. We will investigate this. This would end up failing by signal integrity issues, obviously, but we are unsure what those distances are.

31. For the ADC/DAC Data Acquisition reference design (125 MSPS) what is the bit width of the samples?

    ADC has 12- and 14-bit variants. DAC is 12 bit.

32. Are there high-speed, low-latency DACs with the SYZYGY interface available?

    The only DAC and ADC available through Opal Kelly are located at:
    https://docs.opalkelly.com/syzygy-peripherals/szg-adc-ltc226x/
    https://docs.opalkelly.com/syzygy-peripherals/szg-dac-ad911x/

33. Do you know the signal switching latency for the AD9116 version?

    You can inspect the data sheet for the DAC. You can also view more information at: https://docs.opalkelly.com/syzygy-peripherals/szg-dac-ad911x/

34. Is the interface exclusively command line?

    The FrontPanel SDK supplies an API for various languages for you to create command line applications. You may also use the FrontPanel GUI to create applications with a graphical user interface. More information can be found at: https://opalkelly.com/products/frontpanel/

35. Does solution support Kubernetes / containers?

    This is not supported. We will consider adding this to some later version of the SDK. You can read about what the SDK supports at: https://docs.opalkelly.com/fpsdk/introduction/

36. What level of support is provided for Vitis vision libraries?

    ISP and Vision Library IP are supported in Vivado and Vitis tools.

37. Is HPIO SGMII compatible? (over LVDS, Non-Transceiver)

    Yes, HPIO was supported for SGMII over LVDS on KU+ so it should be supported on AU+ as well.

38. Does the AU10P device come with 16Gb/s transceivers?

    Yes, The Artix UltraScale+ FPGAs have both GTH and GTY with 16.3Gb/s transceivers. You can refer to the product selection guide for more details.

39. How do smaller density AU10 and AU15 support PCIe Gen4 with 12G transceivers?

    The AU15/AU10P devices have transceivers that are capable of 16Gb/s in the A676 package.

40. Can customer buy the XEM8320-AU25P from Xilinx distributor?

    Boards are available exclusively through Opal Kelly.

41. Will this family support soft RISC-V IP?

    This is something we are currently investigating. Bluespec, SiFive, and a few other IP vendors are already doing this.

42. Does using the Vivado Store require Vivado to be connected to the internet?

    It does. You must retrieve the latest board files from the Board Store GitHub repository, Vivado will fetch this though the GUI. You can obtain a local copy though, and point Vivado to that repository.

43. Why is there no UltraRAM in Artix UltraScale+ FPGAs?

    To ensure a cost-optimized device portfolio, UltraRAM is not available in these FPGAs. The available block RAM can support the aggregate bandwidth and most applications we've targeted for this portfolio.

44. How is communication to the FPGA on the evaluation kit managed?

    Communication to the FPGA is done through a USB3 microcontroller. We have a Java API available. See the following: https://docs.opalkelly.com/fpsdk/frontpanel-api/programming-languages/