Versal PDN Model User Guide

Contents

Introduction

Versal PDN modes are provided by AMD to facilitate PCB board-level simulations of the various power rails to ensure the voltage ranges adhere to datasheet limits.

PDN Model Downloads

Versal PDN models can be found at:

https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/device-models/pdn-models/versal-acaps.html

Power Design Manager (PDM)

The AMD Power Design Manager (PDM) tool is referenced in this document. PDM provides accurate power estimates for the specific user design as well as providing decoupling capacitor recommendations for the board. PDM can be downloaded at Power Design Manager

Components of a PDN Simulation

An ACAP PDN simulation will typically contain models for the ACAP itself, a PCB extracted model, PCB decoupling capacitors, and optionally a model for the voltage regulator module (VRM). Figure 1 shows these components in graphical form, with Figure 2 showing a schematic view.

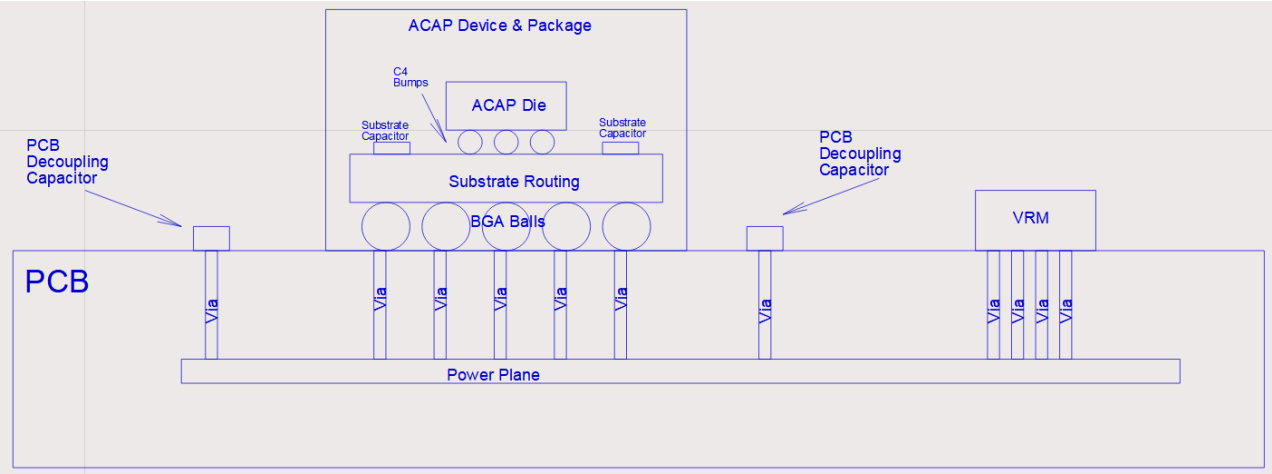


Figure 1: PDN Simulation Model

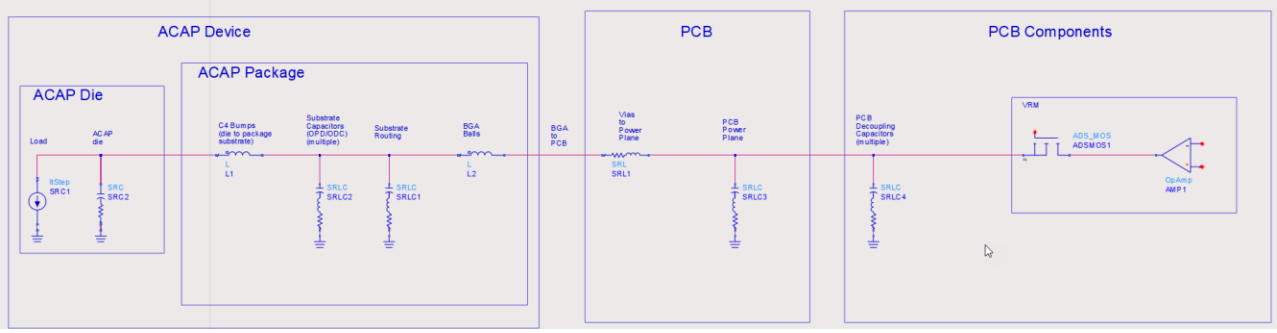


Figure 2: Schematic Model of PDN Simulation

ACAP Die & Package Model (AMD PDN Model)

ACAP Die & Package models include die R/C, substrate routing, and on-package-capacitors (substrate capacitors). AMD provides an all-encompassing model for each rail on each Versal device. The models provided by AMD are in s-parameter form, with die ports (for transient simulations) as well as a single port for a combined BGA connection. By providing an S-parameter model with die R/C, substrate routing, and on-package-capacitors included, the user does not need to be concerned with these aspects of the design, which are often proprietary in nature and that would require high complexity to compile and obtain individually from AMD.

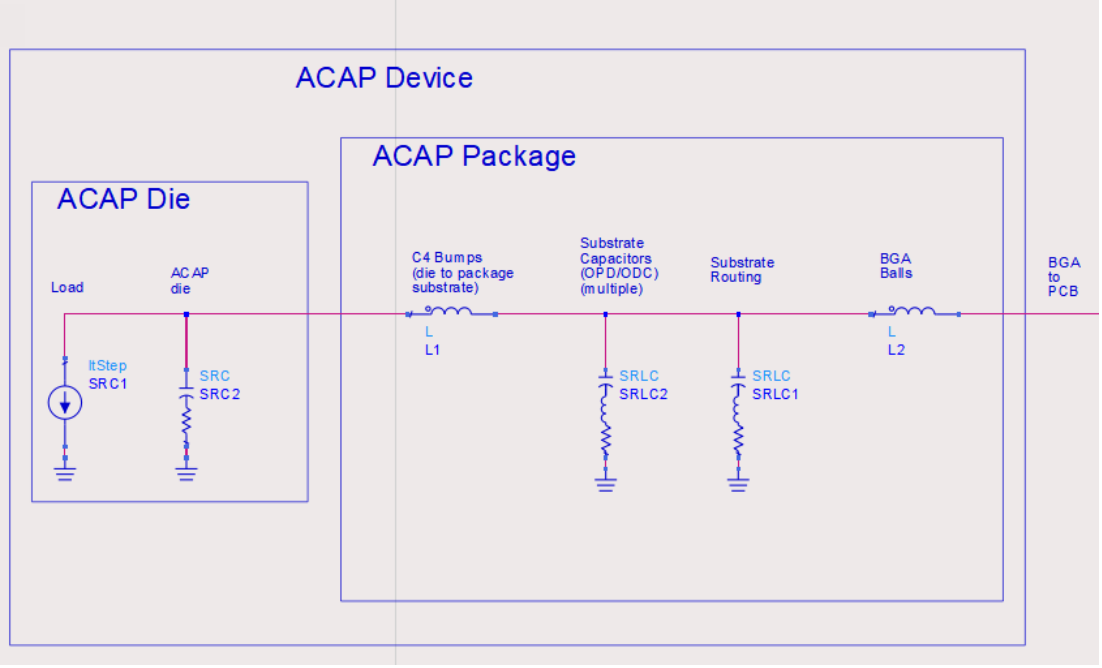


Figure 3: Schematic view of ACAP Die & Package Model

PCB Model

This is the model of the user's printed circuit board without any components. The model includes PCB and component footprints, vias, traces found on all layers of the PCB. It is possible to include PCB capacitor models in this model if the extraction tool allows for it. There will generally be at least one port for the ACAP BGA (all BGA pins merged to one point) and ports for each component on the board.

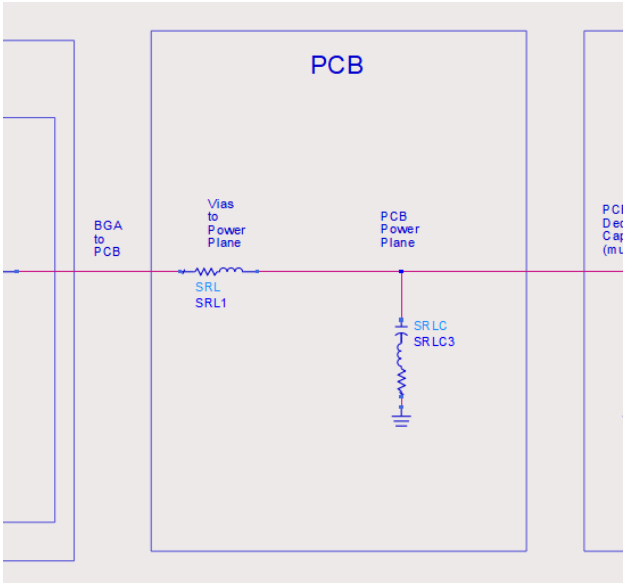


Figure 4: Schematic view of PCB Model

The PCB decoupling capacitor quantities can be determined via simulation and via the AMD PDM tool. ADM recommends utilizing the PDM tool in order to estimate power in the design and to determine the quantities and types of decoupling capacitors to use either as presented or as part of a first pass PDN simulation. Figure 5 shows an example of PDM output listing recommended PCB decoupling capacitor quantities and types:

Power Supply Design

Power Rail Group	Schematic Name	Power Domain/	Voltage	AC Ripple*	DC*	Dynamic	Step Current	Total	Power Delivery	Power Delivery	330uF-1210	100uF-0805	47uF-0603	22uF-0603	10uF-0402	1.0uF-0201
1V8_PMC_IO (Digital)		PMC/1	1.800 V	4%	1%	0.004 A	0.004 A	0.300 A					1		1	
0V80_PMC (Digital)		PMC/2	0.800 V	+-17mV	1%	0.145 A	0.048 A	1.233 A					1		1	
1V5 (Digital)		PMC/3	1.500 V	2%	1%	0.064 A	0.064 A	1.211 A					1		1	
0V80_SOC_IO (Digital)		SYSTEM/2	0.800 V	+-17mV	1%	0.002 A	0.001 A	8.657 A			1	1	1		1	
1V5_VCCAUX (Digital)		SYSTEM/3	1.500 V	2%	1%	0.060 A	0.020 A	11.577 A					1		1	
1V8_PS_IO (Digital)		LPD/1	1.800 V	4%	1%	0.000 A	0.000 A	0.300 A					1		1	
0V80_PSLP (Digital)		LPD/2	0.800 V	+-17mV	1%	0.000 A	0.000 A	1.355 A				1	1		1	1
0V80_PSFP (Digital)		FPD/1	0.800 V	+-17mV	1%	0.000 A	0.000 A	6.025 A					1		1	
3V3_VCCO (Digital)		PL/1	3.300 V	+2%/-4%	1%	0.000 A	0.000 A	0.000 A								
2V5_VCCO (Digital)		PL/1	2.500 V	4%	1%	0.000 A	0.000 A	0.000 A								
1V8_VCCO (Digital)		PL/1	1.800 V	4%	1%	0.000 A	0.000 A	0.000 A								
1V5_VCCO (Digital)		PL/1	1.500 V	4%	1%	0.003 A	0.003 A	0.409 A					1		1	
1V35_VCCO (Digital)		PL/1	1.350 V	4%	1%	0.000 A	0.000 A	0.000 A								
1V2_VCCO (Digital)		PL/1	1.200 V	4%	1%	0.000 A	0.000 A	0.000 A								
1V1_VCCO (Digital)		PL/1	1.100 V	4%	1%	0.000 A	0.000 A	0.000 A								
1V0_VCCO (Digital)		PL/1	1.000 V	4%	1%	0.000 A	0.000 A	0.000 A								
0V80_VCCINT_RAM (Digital)		PL/2	0.800 V	+-17mV	1%	372.382 A	119.035 A	378.882 A			13	19	45		83	159
0V92 (Analog)		PL/3	0.920 V	+-17mV	1%	30.526 A	24.198 A	31.951 A			8	16	8	8	8	8
1V5 (Analog)		PL/4	1.500 V	10mV pk-pk	2%	0.799 A	0.593 A	1.279 A						4		4
1V2 (Analog)		PL/5	1.200 V	10mV pk-pk	2%	45.001 A	35.186 A	45.477 A			8	16	8	8	8	8

Figure 5: Example PDM output showing recommended PCB decoupling capacitors

PCB Decoupling Capacitor Models & Voltage Regulator Models

These models can be found directly from various capacitor manufacturers. Models are typically provided in s-parameter form and/or SPICE form.

If a suitable voltage regulator model is available from the manufacturer, it can be included in the simulation, though it is not always necessary.

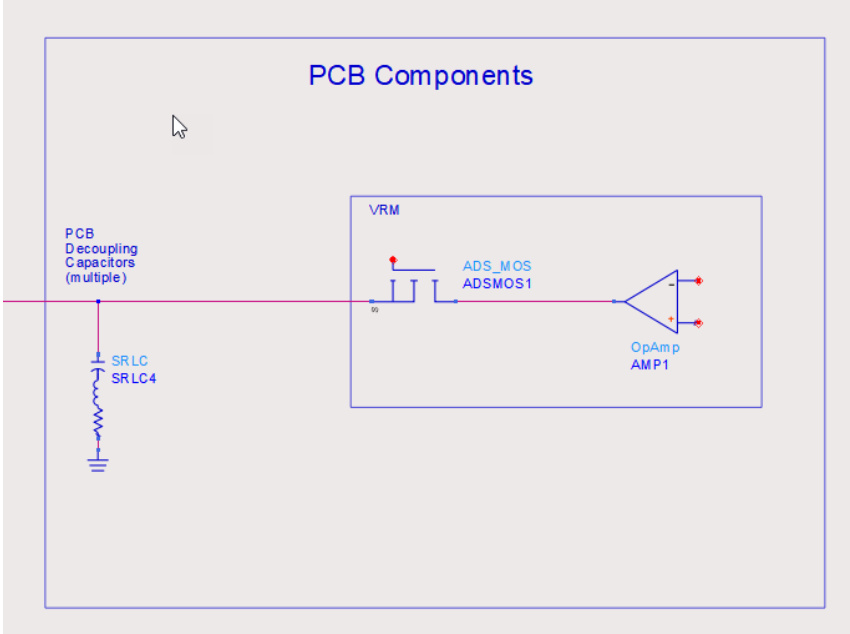


Figure 6: Schematic view of PCB Capacitor and VRM Models

Explanation of AMD PDN Model Ports

Each AMD package model includes one or more die ports, along with one or more BGA ports, depending on the particular rail. Only Gigabit Transceiver (GT) models contain more than one BGA port as the GT blocks are generally separated on both sides of the device with the respective power rails intended to be connected together at the PCB level.

XCVP2802_VSVA5601_VCC_PSFP.s2p

```
! Created Thu May 26 11:27:32 2022
! Port 1:  die
! Port 2:  BGA
# hz S ma R 0.1
! 2 Port Network Data from SP1.SP block
! freq  magS11  angS11  magS21  angS21  m
!
                0      0.0182733428
              100      0.0182745715
              200      0.0182782572
```

Figure 7: Example of model with one die port

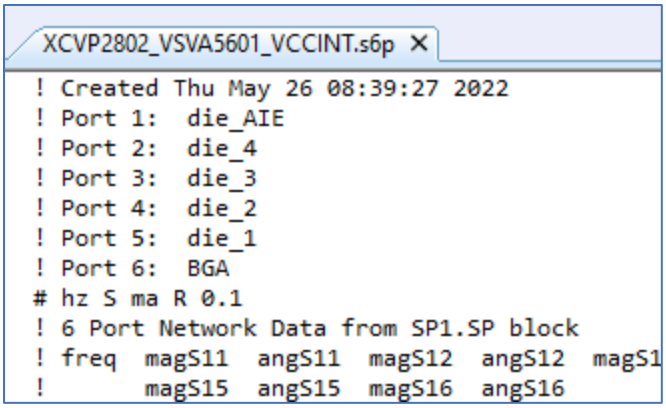


Figure 8: Example of ACAP model with multiple die ports

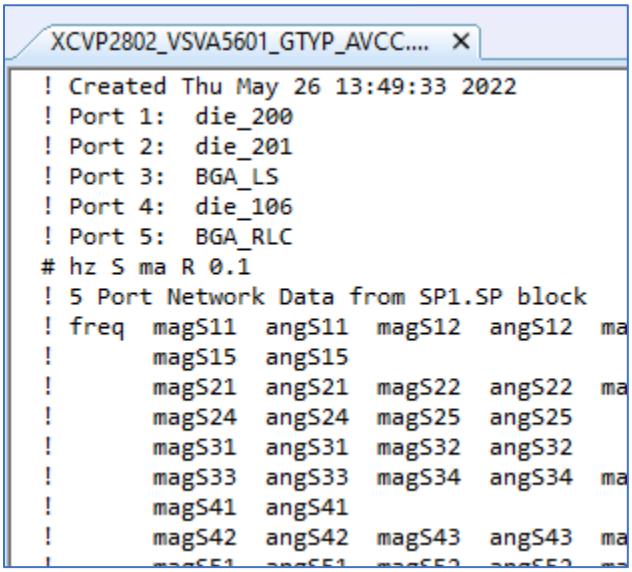


Figure 9: Example of ACAP model with multiple die and BGA ports

For Frequency vs Impedance (F-Z) simulations, the user would only be concerned with the impedance at the BGA port(s), as AMD guarantees device performance as long as the voltage limits from the datasheet are adhered to. In other words, the die ports for F-Z simulations can be left unconnected.

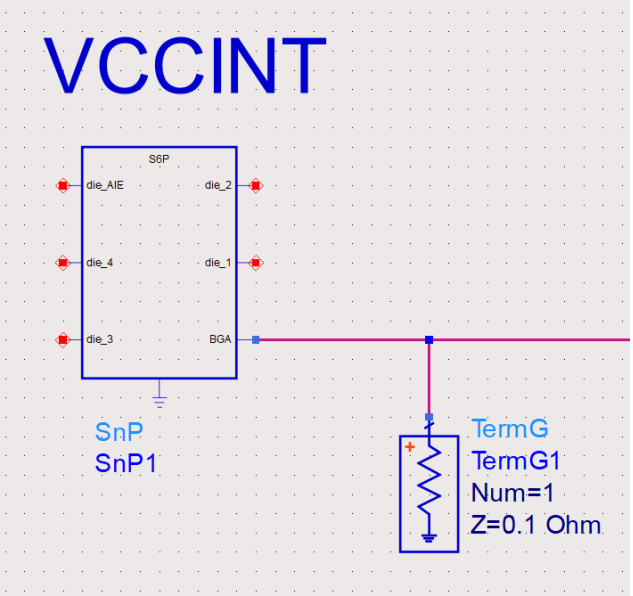


Figure 10: Example of F-Z Simulation with die ports unconnected

For Transient simulations, die ports are included so the current source(s) of the transient load can be placed on them. The user is still only concerned with the voltage(s) at the BGA port(s), but putting the transient current sources at the die ports provides the most realistic path of the current step. It is recommended that all die ports be connected together for transient simulations with one current source that reflects the entire anticipated transient load on the rail. For advanced simulations, the user can apply individual current transients to each die port, but that would require knowledge of individual transient activity at each point in the die, which is generally not available.

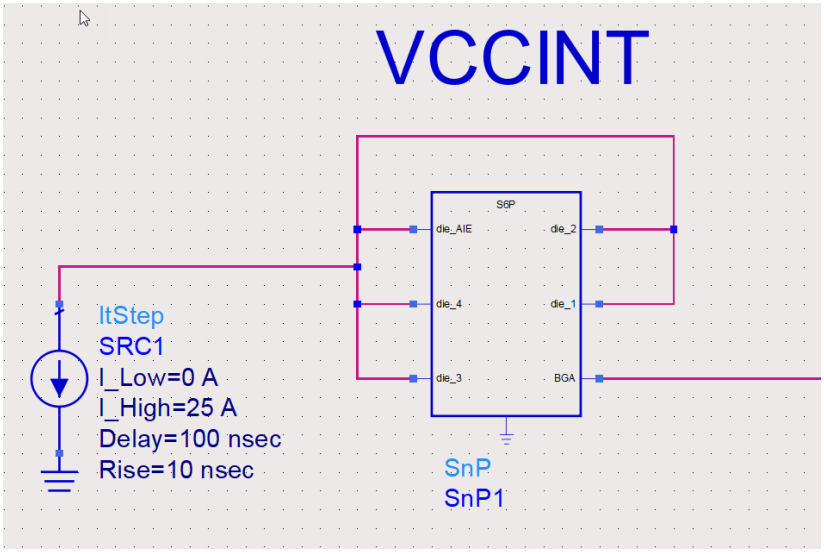


Figure 11: Example of Transient Simulation with all die ports connected together

Example of PDN Simulation Schematic

Figure 12 shows an example schematic for simulating a combined 0.8V PCB rail that connects VCCINT, VCC_RAM, and VCCINT_GT from the ACAP to the board. ACAP die/package models are shown (provided by AMD). The PCB model shown consists of a generic parallel-plate capacitor model along with BGA vias connecting the ACAP rails to the "0.8V" plane in the PCB. PCB decoupling models are also shown (vias to the 0.8V plane are within the capacitor symbols).

NOTE: Using a generic PCB model (as shown) is useful in the beginning phases of PCB design, though it is intended that a board extraction be performed and used for final simulations to better predict the actual behavior of the design.

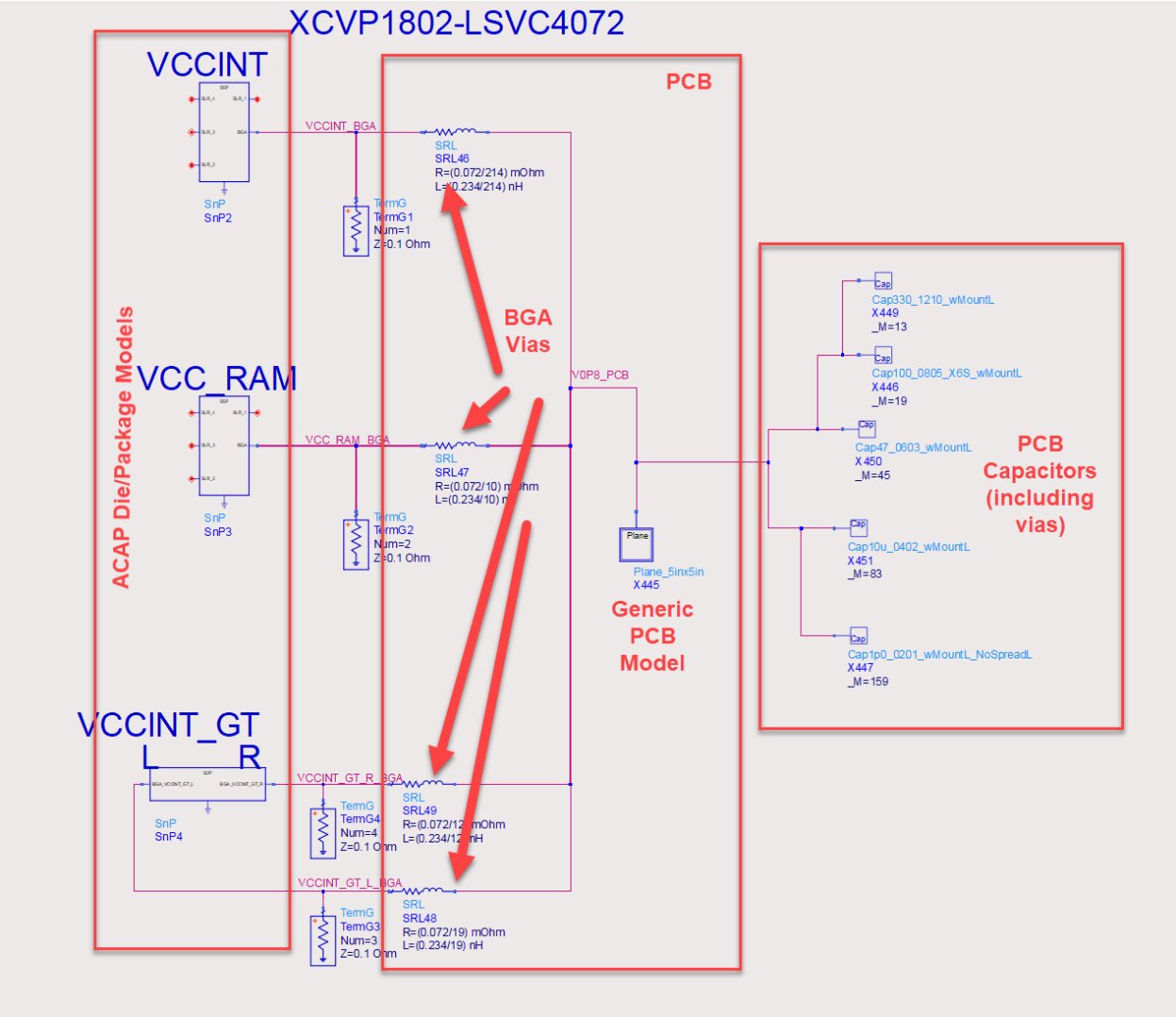


Figure 12: Example PDN Simulation Schematic (with generic PCB model)

Frequency-Impedance (F-Z) Simulations

A common method to determine if the system power delivery network (PDN) is operating in the proper range is to perform a frequency-Impedance simulation in which the system PDN impedance for each rail is compared against a "target" impedance that is derived from the worst-case anticipated current step on the rail. Figure 13 shows the result of an F-Z simulation for the VCCINT rail.

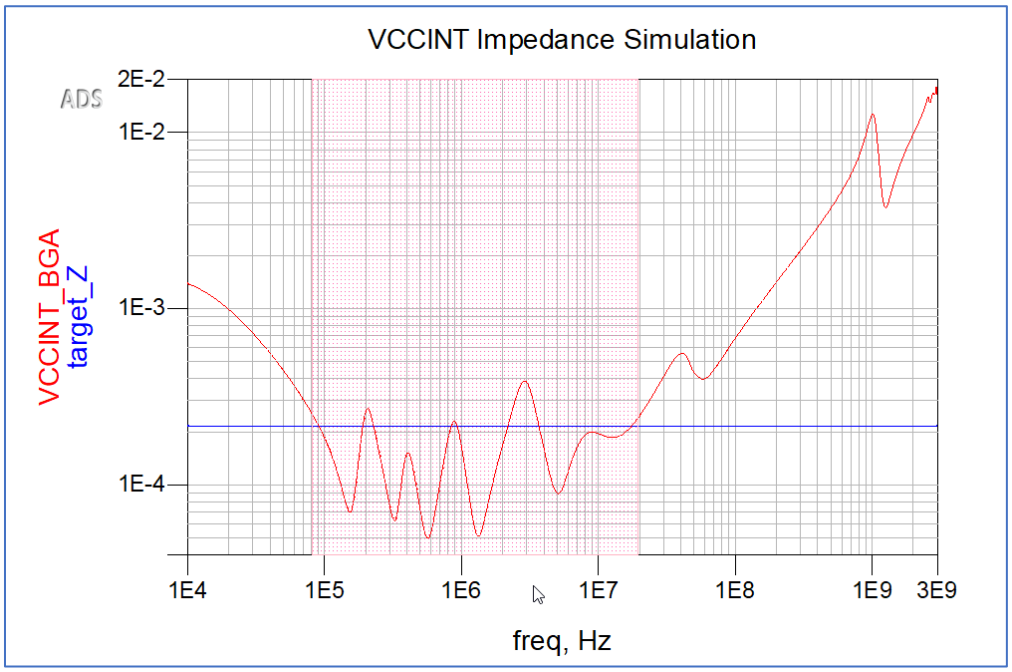


Figure 13: Target Impedance Simulation Output

The simulation shows the impedance of the VCCINT rail at the output of the ACAP BGA (in red) over a wide frequency range, along with a horizontal "target" impedance line for the rail (in blue), which is based on the specific nature of the design. The pink shaded area shows the frequency range in which the on-board PCB decoupling capacitors have their greatest effect on the impedance of the rail. The typical range is for PCB capacitor effectiveness is ~100kHz to ~15-20MHz. Below 100kHz is where the voltage regulator predominates, and above 20MHz is where decoupling capacitors in the Versal package predominate. If the impedance of the rail is too far above the target impedance in the shaded range, then the PCB design can redesign the board, including adding more PCB capacitors as needed.

REMINDERS:

- The impedance should be plotted at the BGA output, which is where the ACAP specifications in the datasheet are based.
- The voltage regulator is presumed to control the impedance of the network below ~100kHz.
- For frequencies above ~15-20MHz, while the above simulation appears to show out of specification, the capacitors on the ACAP package will work to ensure that the voltages at the die level remain in proper operating range.

Target Impedance Calculation

The target impedance for a rail is defined as

$$Ztarget = \frac{VoltageRipple}{CurrentStep}\ \Omega$$

Equation 1: General Voltage Ripple Equation

...where *VoltageRipple* is the allowable voltage dip on the rail, and *CurrentStep* is the maximum expected current step load on the rail.

Voltage Ripple

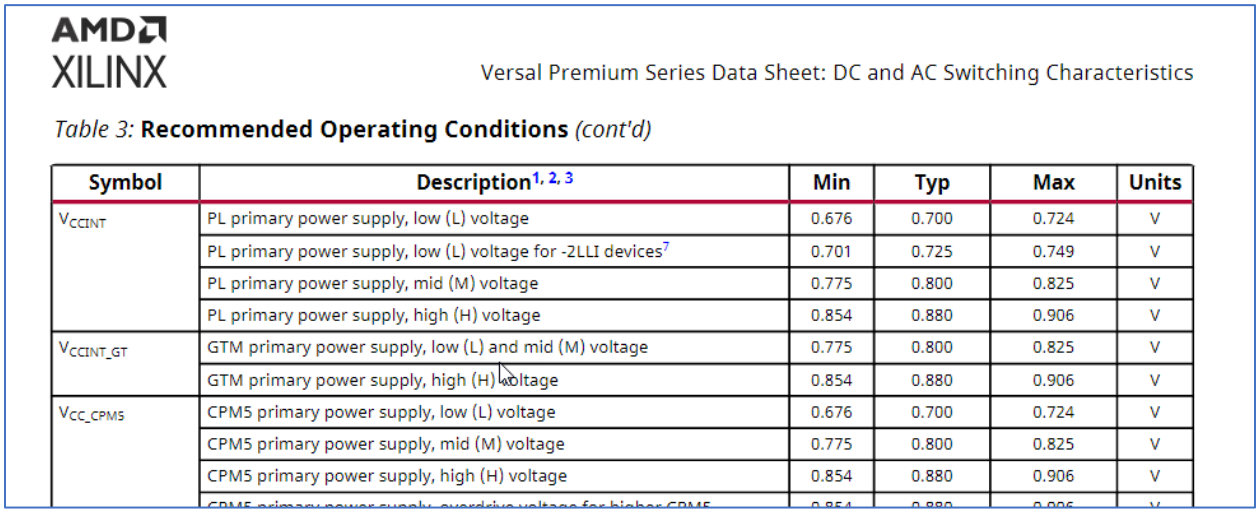
Voltage ripple can be determined from AMD datasheets and with knowledge of the DC tolerance of the voltage regulator being used. Typical voltage regulator tolerances are 1%, though can be higher or lower depending on the specific regulator.

$$VoltageRipple = Vtyp * (\left(\frac{(Vtyp - Vmin)}{Vtyp}\right) - \left(\frac{Tolerance\%}{100}\right))\ \ V$$

Equation 2: Versal Voltage Ripple Equation

Vtyp is the nominal recommended voltage, and *Vmin* is the minimum recommended operating voltage.

Each Versal datasheet lists "Recommended Operating Conditions" for each voltage rail that lists Minimum, Typical, and Maximum voltage levels. The voltage regulator DC tolerance level can be found from the manufacturer of the regulator.



AMD XILINX

Versal Premium Series Data Sheet: DC and AC Switching Characteristics

Table 3: **Recommended Operating Conditions** *(cont'd)*

Symbol	Description[1, 2, 3]	Min	Typ	Max	Units
V_{CCINT}	PL primary power supply, low (L) voltage	0.676	0.700	0.724	V
	PL primary power supply, low (L) voltage for -2LLI devices[7]	0.701	0.725	0.749	V
	PL primary power supply, mid (M) voltage	0.775	0.800	0.825	V
	PL primary power supply, high (H) voltage	0.854	0.880	0.906	V
V_{CCINT_GT}	GTM primary power supply, low (L) and mid (M) voltage	0.775	0.800	0.825	V
	GTM primary power supply, high (H) voltage	0.854	0.880	0.906	V
V_{CC_CPM5}	CPM5 primary power supply, low (L) voltage	0.676	0.700	0.724	V
	CPM5 primary power supply, mid (M) voltage	0.775	0.800	0.825	V
	CPM5 primary power supply, high (H) voltage	0.854	0.880	0.906	V

Figure 14: Example Versal Datasheet showing Recommended Voltage limits

Example: VCCINT Voltage Ripple

Applying Equation 2 along with the VCCINT values listed in Figure 14 for low (L) voltage and assuming 1% DC tolerance for the voltage regulator results in the following voltage ripple value:

VoltageRipple = 0.70*((0.70-0.676)/0.70) – (1/100)) = 0.017 mV = 0.017 V = 17 mV

Current Step

The current step for a rail is unique to the specific design in the ACAP. The current step for a rail is calculated as the maximum step (or spike) of current that the rail may be subjected to during any point in the normal operation of the design. The current step value can be calculated in many ways with specific knowledge of the design. A common method to use is to assume the maximum current step to be some sort of percentage of the overall dynamic current on the rail. A typical percentage can be 25%, 33%, or even 100%.

$$CurrentStep = DynamicCurrent * \left(\frac{Step\%}{100}\right) \quad A$$

Equation 3: Versal Current Step Equation

AMD recommends utilizing the PDM tool to determine the dynamic currents for each rail. PDM also lists recommended step percentages for each rail, though the user is encouraged to study their design to determine if the step percentage should be higher or lower. Lower step current percentage will correspond with few decoupling capacitors required on the PCB.

Power Design

Supply	Voltage	Min Voltage	Max Voltage	Step Load %	Static (A)	Dynamic (A)	Total (A)	Powerup (A)	Power Rail Group
Platform Management Controller(PM									
VCC_PMC	0.800	0.775	0.825	33.00 %	0.033	0.145	0.178	1.233	0V80_PMC (Digital)
VCCO_503	1.800	1.710	1.890	100.00 %	0.000	0.004	0.004	0.300	1V8_PMC_IO (Digital)
VCCO_500	1.800	1.710	1.890	100.00 %	0.000	0.000	0.000		1V8_PMC_IO (Digital)
VCCO_501	1.800	1.710	1.890	100.00 %	0.000	0.000	0.000		1V8_PMC_IO (Digital)
VCCAUX_PMC	1.500	1.425	1.575	100.00 %	0.008	0.064	0.072	0.808	1V5 (Digital)
VCCAUX_SMON	1.500	1.425	1.575	100.00 %	0.003	0.000	0.003	0.403	1V5 (Digital)
VCC_FUSE	1.800	1.710	1.890		0.000	0.000	0.000		
Low Power Domain (LPD)									
VCC_PSLP	0.800	0.775	0.825	33.00 %	0.018	0.000	0.018	0.818	0V80_PSLP (Digital)
VCCO_502	1.800	1.710	1.890	100.00 %	0.000	0.000	0.000	0.300	1V8_PS_IO (Digital)
VCCINT_CPM5	0.800	0.775	0.825	100.00 %	0.086	0.000	0.086	0.536	0V80_PSLP (Digital)
Full Power Domain (FPD)									
VCC_PSFP	0.800	0.775	0.825	33.00 %	0.025	0.000	0.025	6.025	0V80_PSFP (Digital)
System Auxiliary									
VCCAUX	1.500	1.425	1.575	33.00 %	4.107	0.060	4.167	11.577	1V5_VCCAUX (Digital)
System Core									
VCC_SOC	0.800	0.775	0.825	33.00 %	0.634	0.000	0.634	7.867	0V80_SOC_IO (Digital)
VCC_IO	0.800	0.775	0.825	33.00 %	0.043	0.002	0.044	0.790	0V80_SOC_IO (Digital)
Programmable Logic Core									
VCCINT	0.800	0.775	0.825	25.00 %	5.941	314.128	320.069		0V80_VCCINT_RAM (Digital
VCC_RAM	0.800	0.775	0.825	33.00 %	0.150	0.740	0.891	1.012	0V80_VCCINT_RAM (Digital
Programmable Logic IO									
VCCO 1.5V	1.500	1.425	1.575	100.00 %	0.009	0.003	0.012	0.409	1V5_VCCO (Digital)
VCCO 1.35V	1.350	1.283	1.417	100.00 %	0.000	0.000	0.000		1V35_VCCO (Digital)
VCCO 1.2V	1.200	1.140	1.260	100.00 %	0.000	0.000	0.000		1V2_VCCO (Digital)

Figure 15: Example Portion from PDM showing Dynamic Currents and Step Percentages

Example: Current Step for VCCINT

Assuming the design values from Figure 15 for VCCINT, the dynamic current is 314.128 A and a Step Load of 25% results in the following step current value based on Equation 3.

$$CurrentStep = 314.128*(25/100) = 78.532 \text{ A}$$

Target Impedance Calculation

Utilizing the example *VoltageRipple* and *CurrentStep* values calculated above, the target impedance can be calculated using Equation 1:

$$VoltageRipple = 0.017/78.532 = 0.0002164 = 0.216 \text{ m}\Omega$$

With the target impedance calculated, the board designer can modify the board layout as well as add/subtract PCB capacitors in order to ensure the impedance of the network is as close to or below the target impedance as practical over the 100kHz to 15−20MHz range.

NOTE: It is not always practical to achieve the network impedance to be completely below the target impedance in the 100kHz to 15−20MHz range as it may take extreme amounts of PCB capacitors to attain this. If any portion of the impedance is above the target at a particular frequency, the design should be analyzed to determine if there is any switching activity at or near that frequency. If not, then it may be OK to allow this overage. If there is switching activity at that frequency, then either more capacitors can be added, or the design be modified away from that range.

Transient Simulations

A transient (time-based) simulation can be run to specifically look at how low the outputs of the BGA droop due to a current spike event. This method involves placing current sources on the die ports of the AMD PDN models and observing the BGA node(s) during the switching event.

Figure 16 shows a transient simulation schematic with current step sources at the die nodes for each ACAP rail. The current step values were calculated using Equation 3. Figure 17 is zoomed-in at the VCCINT are to show detail. The current step value of 78.532A is shown, along with a 10ns rise time, and a delay offset of 100ns.

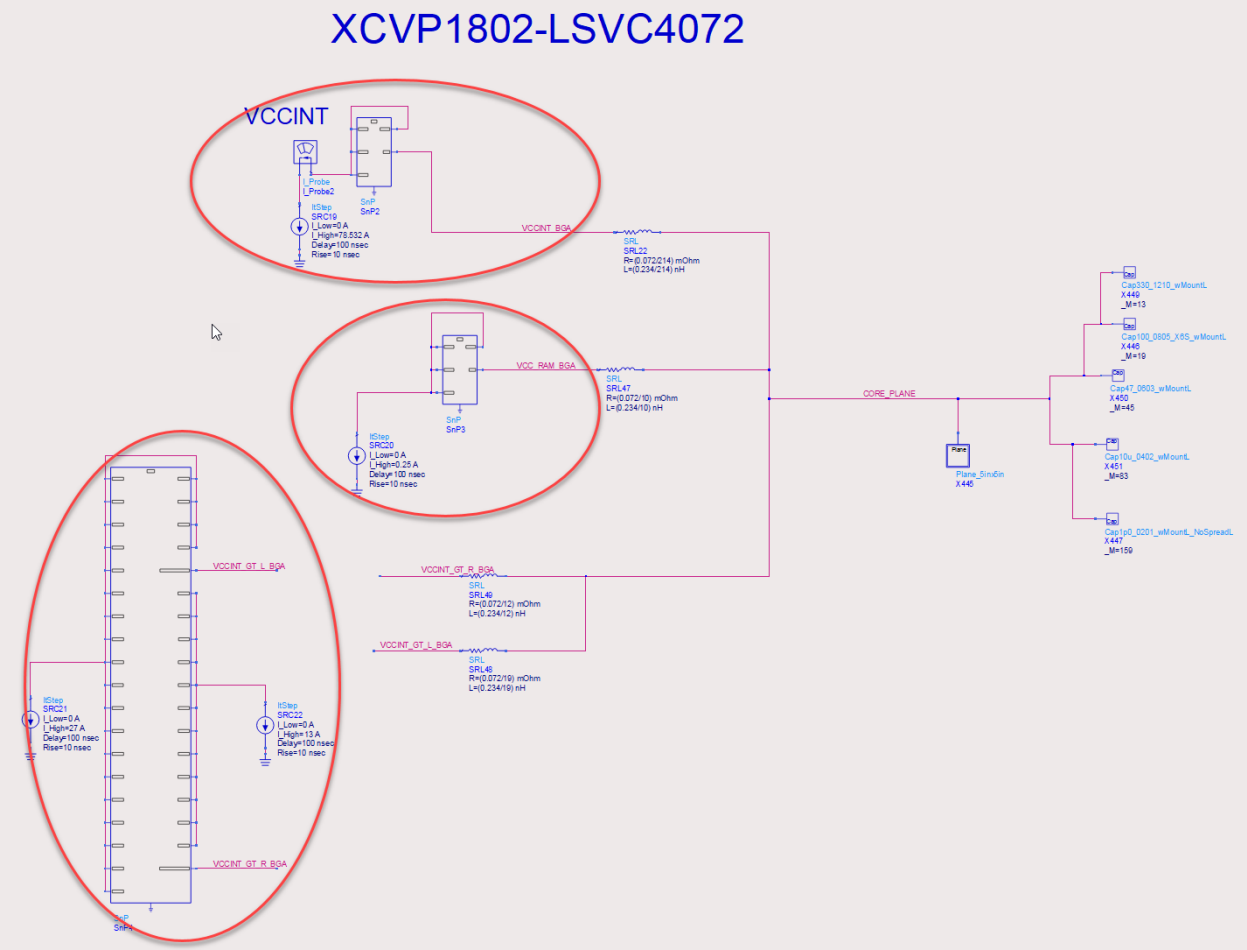


Figure 16: Schematic for Transient Simulations

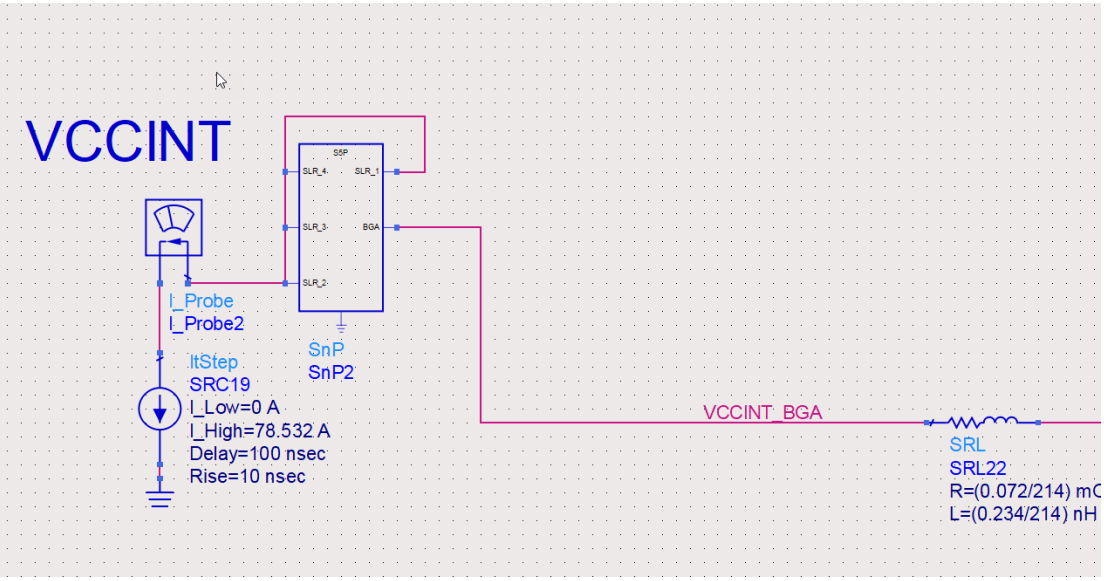


Figure 17: Zoom in of Transient Schematic at VCCINT

Figure 18 shows the droop simulation result at the VCCINT BGA port as a result of the switching event. The maximum droop is shown to be approximately 10.60mV, which is well below the 17mV target as calculated in Equation 2. If the voltage would drop below the target, then the PCB design could add more decoupling capacitors as well as redesign the power planes as necessary.

The transient simulation also shows the recovery of the voltage due to the action of the decoupling capacitors on the PCB. The transient simulation does not show any effects from the voltage regulator as the regulator was not included in the simulation.

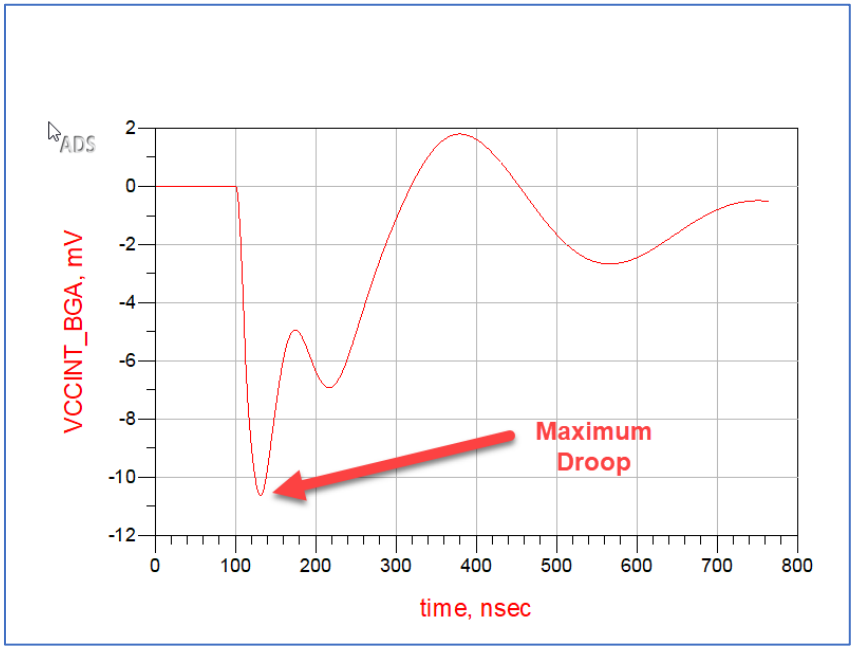


Figure 18: Example of VCCINT droop simulation

Conclusion

Frequency-Impedance and Transient simulations can be performed using the die/package PDN models provided by AMD, along with the Power Design Manager Tool (PDM). Simulations can be run at all stages of the PCB design to ensure adequate power delivery to the ACAP.

Appendix: Via Resistance and Inductance

Various calculators exist for via inductance and resistance. Two well-known formulas exist to calculate the per mil resistance and per mil inductance of a via. The formula for inductance accounts for the spacing in-between the power and ground return vias.

Via Resistance

$$Rvia = \rho / (\pi \times r_{pl} (2r_{hole} + r_{pl})) \ (\Omega/mil)$$ [source]

with ρ equal to 7.815 x $10e^{-4}$ Ω • mil (bulk resistivity of copper), r_{hole} = radius of finished via hole in mils, and r_{pl} equal to the plating thickness (typically 1 mil). This formula accounts for the open space of the finished via hole (resistance would be lower if the via is filled in, but this formula assumes open-space). . Example: The per mil resistance of a via with 8 mil finished hole size (r=4 mil) and plating thickness of 1 mil is 7.815 $X10e^{-4} / \pi \bullet 1(8 + 1) = 0.00002764$ Ω/mil or 0.02764 mΩ/mil. A 50 mil long via would thus be 1.382 mΩ.

Via Inductance

$$Lvia = (\mu_o/\pi) \times \ln[(s/2r) + \sqrt{((s/2r)^2 - 1))} \ ] \ (pH/mil)$$ [source, eq 4.72]

With μ_o equal to 32pH/mil (permeability of free space), s equals spacing between via and ground return via, and r equal to radius of finished via hole. Example: The per mil inductance of a via with 8 mil hole size (r=4 mil) and spaced 31.5 mil (0.8mm) from the ground return via is $32/\pi$ x ln $[(31.5/8) + \sqrt{((31.5/8)^2 -1)}] = 10.1869$ x ln[$3.9375 + \sqrt{(15.504 -1)}] = 20.85$ pH/mil. A 50 mil long via would thus be 1042.61 pH or 1.043 nH.