REDUCING IMPLEMENTATION COSTS FOR DIGITAL AUDIO IN BROADCAST APPLICATIONS

XILINX DIGITAL AUDIO REFERENCE DESIGNS

Broadcast Industry Demands

- Support industry standard interfaces for high-end audio and video applications
- Handle any audio in-and-out frequency
- Maintain highest audio quality while remaining cost competitive

The Xilinx Solution

- Complete reference designs for audio interfacing, embedding/de-embedding, and ASRC
- Pre-verified and easy to integrate into your own FPGA designs
- Reduce costs by eliminating need for external audio ASSPs

Complete Audio Design Solution

In many broadcast applications, the Audio Engineering Society AES3 audio standard for digital is embedded and multiplexed in the horizontal ancillary space (HANC) portion of triple-rate SDI video streams to ease the transport of combined audio and video. Audio applications may also require different sampling frequencies depending on the sources and destinations of the audio streams. Source material recorded with one sample rate often must be converted to another sample rate for processing using asynchronous sample rate conversion (ASRC). Xilinx provides digital audio reference designs with the unrivalled digital signal processing (DSP) performance of Xilinx FPGAs to address the full range of audio interfacing, embedding and conversion requirements.

Saving Time and Costs

Xilinx reference designs enable hardware engineers to rapidly integrate audio functionality into their products using FPGAs as a cost-effective and flexible alternative to application-specific standard products (ASSPs). With these robust, pre-verified designs, engineers can take full advantage of the DSP performance, bandwidth, and features of Xilinx FPGAs to implement system-on-chip designs that eliminate the need for separate components to perform audio processing tasks, thereby reducing costs, particularly for multi-channel audio applications.

Supporting all your Broadcast Connectivity Needs

Xilinx digital audio references designs are an integral part of the Xilinx Broadcast Connectivity Targeted Design Platform that brings overall lower system cost and high performance, lower power serial connectivity to broadcast video, audio, and network applications. The platform integrates all the hardware and software elements needed to quickly build systems and fully characterize and verify performance, including the latest generation Virtex®-6 and Spartan®-6 FPGAs, intellectual property (IP) blocks, design environments, and reference designs, along with a base set of digital audio/video development boards and industry-standard FPGA Mezzanine Card (FMC) daughter boards.

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DIGITAL AUDIO REFERENCE DESIGN FEATURES

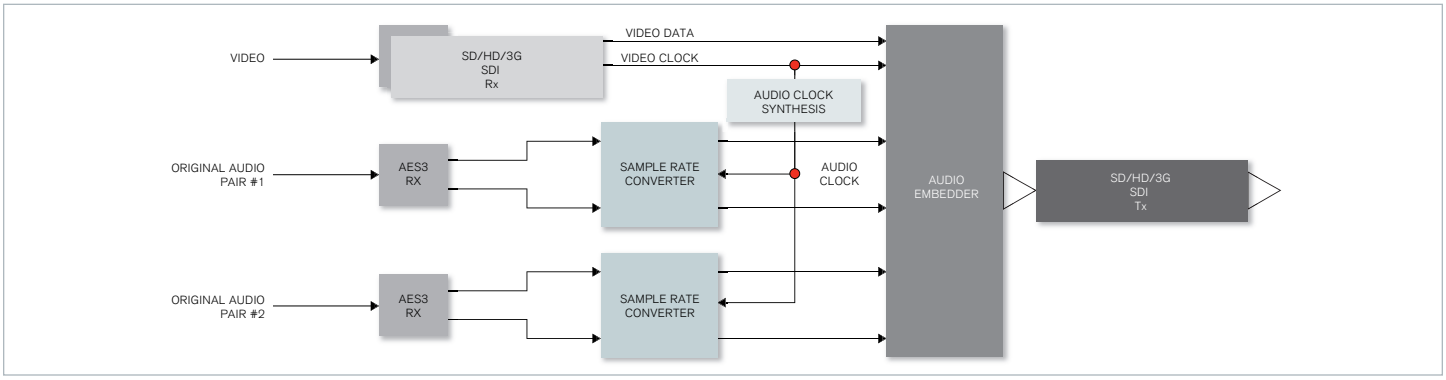
REFERENCE DESIGNS	FEATURES
AES3 Interface	AES3-2003, SMPTE 337, S/PDIF standards; Up to 192 KHz sample rate; Up to 24 bits per audio sample; User data supported; Channel status supported
Audio (De)Embedder	Triple-rate SDI per SMPTE 299M standards: input field to designate which line standard is being used; 24-bit audio at multiple sample rates, plus Z, C, U and V flags and an audio valid strobe to indicate timing; Synchronous and asynchronous audio; Single audio group granularity: one instance embeds 4 channels (2 channel pairs); Multiple audio groups can be embedded by daisy-chaining multiple instances of the design; Support for audio control packets; Overwriting of incoming embedded audio; Automatic clock phase and ECC code generation
Audio ASRC	-130dB THD+N typical performance AES3; 8kHz to 192kHz frequency in and out sample rate; Up to 24 bits per audio sample; Synchronous channels added with minimal additional resources; 1:1 asynchronous conversion; Input/output ratios 8:1 to 1:7.5 continuous; Automatic or manual ratio management; Rate change tracking; Deterministic latency; Sample clock jitter rejection; Lock status for external mute

DIGITAL AUDIO REFERENCE DESIGN FPGA RESOURCES

REFERENCE DESIGN	LUTS	FFS	BRAM	DSP BLOCKS
AES3 Tx	58	102	0	0
AES3 Rx	152	270	0	0
HD/3G-SDI Audio Embedded	889	652	0	0
HD/3G-SDI Audio De-embedded	550	687	0	0
ASRC (2 channels)	2393	2552	3	3
ASRC (16 channels)	8	20484	18568	51

Note: Table shows resources required for Virtex®-5 FPGAs. AES Interfaces and ASRC also available for Spartan®-3E FPGAs.

EXAMPLE APPLICATIONS: AES3 INTERFACES, ASRC AND AUDIO EMBEDDER



Take the NEXT STEP

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Printed in the U.S.A. PN 2420