

Xilinx MOST® Solution

The First Flexible End-to-End MOST Solution



The MOST Network Protocol Challenge

- Automotive designers using the MOST® network protocol have few implementation choices
- Unwanted hardware and software partitioning leads to lower integration levels, poorly coupled platform architectures and little ability to customize functions in an application

The Xilinx Solution

- By using a combination of Xilinx Automotive (XA) FPGAs, the MOST NIC (Network Interface Controller) LogiCORE™ IP, and Alliance Member hardware, IP and software solutions, designers can now choose the most suitable hardware and software partitions for their unique requirements

Unique Streaming Port IP Functionality

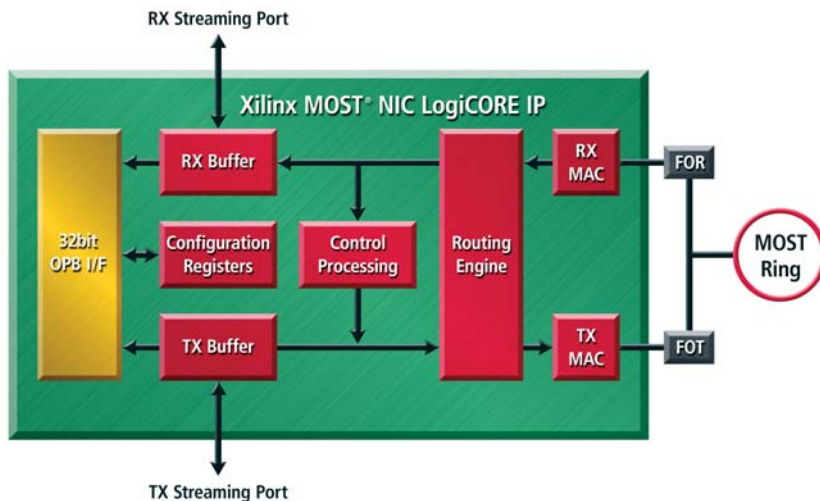
A unique feature of the MOST NIC LogiCORE IP is the inclusion of a Streaming Port allowing direct access to the real-time MOST synchronous channel data. This port, built upon the Xilinx LocalLink protocol, gives designers an extremely efficient and flexible method to take advantage of the FPGA's parallel processing capabilities.

Robust Feature Support

The MOST NIC LogiCORE IP provides support for a wide range of features, including: Transmit and receive ports for real time access to the synchronous portion of the data stream; Synchronous, Asynchronous, and Control channels; the ability to queue up to 2 transmit and 2 receive control channels; and total buffer storage for 32 logical channels, each with 32 bit deep buffers.

A Validated, Versatile Controller Solution

The Xilinx MOST NIC LogiCORE IP implements a complete controller that is designed to revision 2.4 of the MOST specification. Validation will be provided via independent system-level testing including interoperability tests with MOST devices available today. When used in conjunction with Xilinx processor solutions, such as the MicroBlaze™ 32-bit soft processor, or the embedded PowerPC™405 processor, along with a low level driver, the MOCEAN Network Services middleware stack, other Alliance Member IP and the IDT Clock Generation/Recovery chip, Xilinx provides a complete flexible system solution.



Powerful Alliance Program Member Support

Additional MOST IP, including Digital Transmission Content Protection (DTCP), Data Router, and Asynchronous Sample Rate Converter (ASRC) are being developed by Mocean Laboratories AB. Mocean is the world leader in soft MOST IP, and these custom IP cores open the door to flexible architectural possibilities that are not available with current MOST solutions. Integrated Device Technology, Inc., a leader in the silicon-based timing market, has partnered with Xilinx to build a device specifically for use with the Xilinx NIC LogiCORE IP. The IDT chip is able to generate a master clock and lock to the receive stream for clock recovery.

MOST NIC LogiCORE IP Facts

Supported Devices	Spartan-3/XA, Spartan-3E/XA, Virtex-4/XA
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Design Tool Requirements

Xilinx Implementation Tools	ISE™ 8.21 or higher
Simulation	ModelSim 6.1e or higher NC-Sim v5.5 or higher
Synthesis	XST, Synplify Pro 7.5 or higher

Full Automotive Certification

Xilinx, Inc. is certified to ISO-TS16949, as are the fabrication, assembly and test facilities used by Xilinx for automotive device production. The XA product family is also qualified to AEC-Q100 with PPAP documentation available for all devices.

Take the Next Step

To learn more about the Xilinx MOST NIC LogiCORE IP, visit (MOST landing page from Xilinx.com spotlight) www.xilinx.com/esp/automotive/autosolutions/most.htm.

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