

Ultra-Low Latency KEY-Value Store (KVS) for Xilinx Alveo

INTRODUCTION

Key-Value Store (KVS) is an essential service for multiple applications. Telecom directories, Internet Protocol forwarding tables, and de-duplicating storage systems, for example, all need key-value tables to associate data with unique identifiers. In datacenters, high performance KVS tables allow hundreds or thousands of machines to easily share data by simply associating values with keys and allowing client machines to read and write those keys and values over standard high-speed Ethernet.



PRODUCT OVERVIEW

- > FPGA accelerated ultra-low latency search
- > Sub μ -Joule/lookup energy consumption
- > 10 and 40 Gbps Ethernet line rate support
- > Easy to integrate with client software via open-source multi-language APIs
- > Supports standard create, read, update, and delete operations
- > FPGA Devices: Xilinx Alveo U50/U200/U250

Applications

- > Machine Learning
- > Telecom ESN and SIM tables
- > IPv4 and IPv6 addresses
- > NoSQL database acceleration
- > Stock market order IDs
- > Multiplayer game servers

	Key	Value
Examples:	Company	Phone #
Directory	Algo-Logic	(408) 707-3740
	IP Address	Interface : MAC Address
Forwarding Tables	204.2.34.5	Eth6 : 02:33:29:F2:AB:CC
	Content Hash	Storage Block ID
Data De-duplication	XYZ	948830038411
	Vehicle ID	GPS Location
Car Location	ATY1121	37.775, 122.41
	Vertex	Edge List
Graph Search	v140	v201, v206, v225

SOLUTION OVERVIEW

Algo-Logic’s KVS leverages Gateway Defined Networking® (GDN) on Field Programmable Gate Arrays (FPGAs) to perform lookups with the lowest latency (sub-microsecond), highest throughput, and least processing energy. Deploying GDN solutions save network operators time, cost, and power resulting in significantly lower Total Cost of Ownership (TCO).

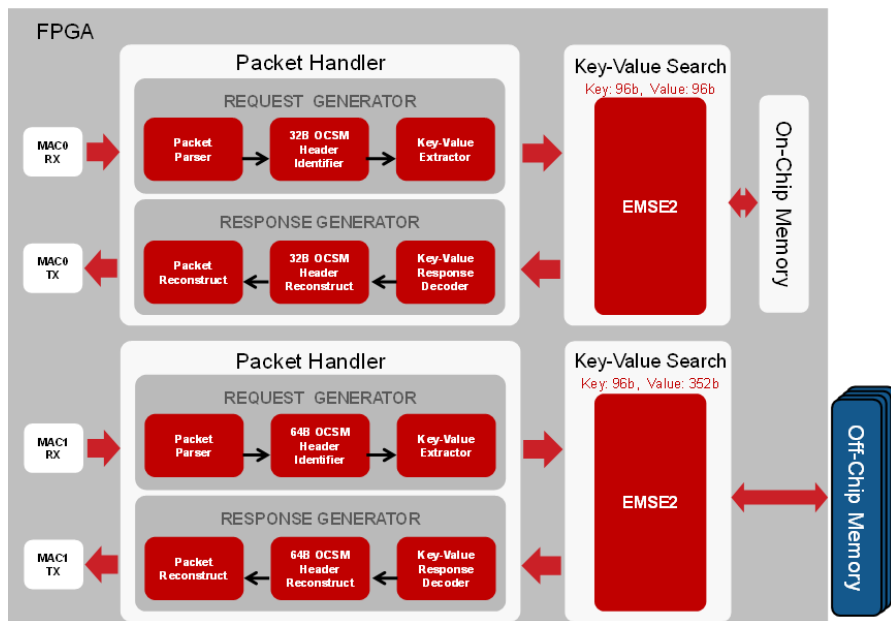
FEATURES

Ultra High Performance

- > Key/Value Search up to 150 MSPS
- > Latency sub 500 nanoseconds
- > Line-rate network at 10GbE or 40GbE

Highly Flexible Key/Value Table Size

- > Entry size 48K (on-chip) to 12M w/DDR SDRAM
- > Key size (typical): 96 bit
- > Value size (typical): 96 to 352 bits



TAKE THE NEXT STEP

To learn more please go to: <https://www.algo-logic.com/xilinx-alveo-u50-u200-u250>

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