Rethinking Digital Downconversion in Fast, Wideband ADCs

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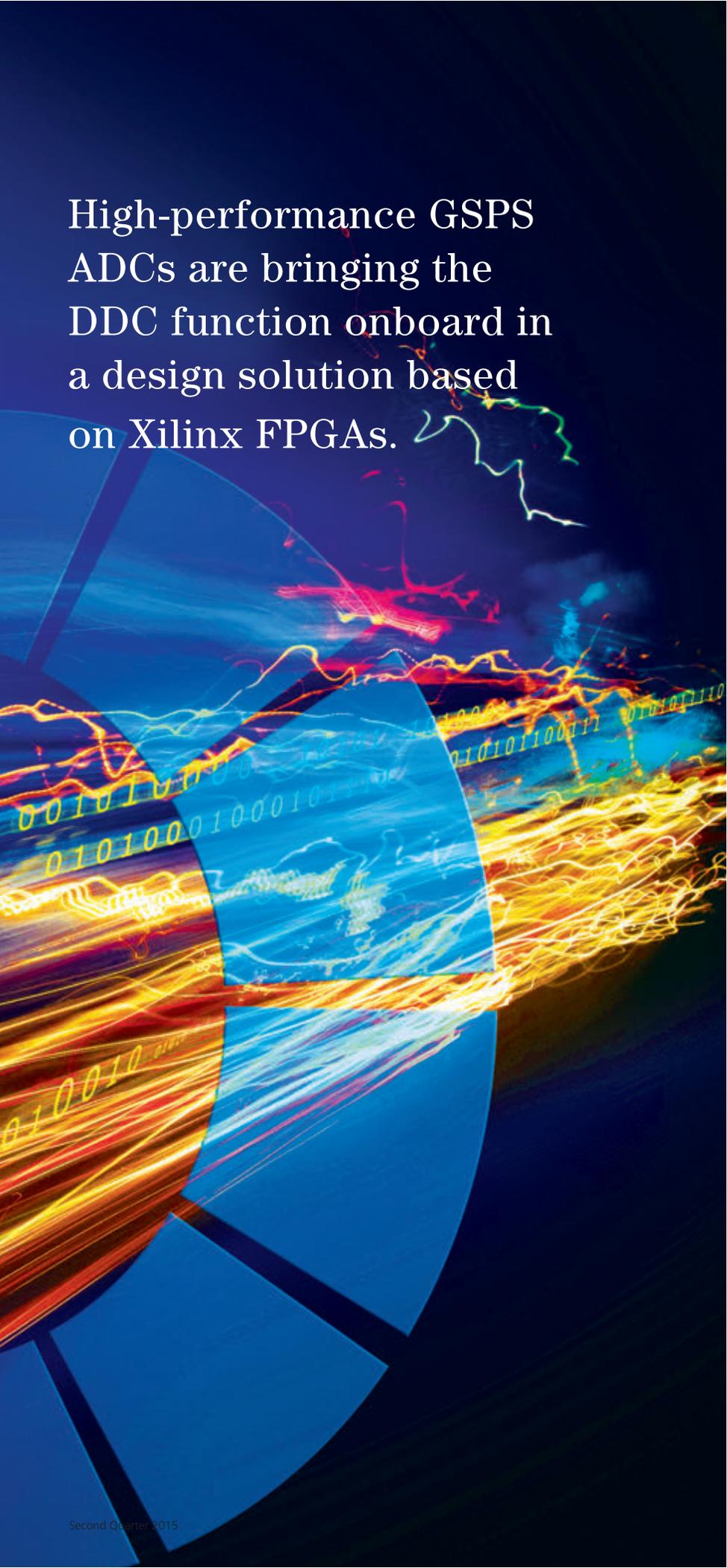
High-performance GSPS ADCs are bringing the DDC function onboard in a design solution based on Xilinx FPGAs.

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Wideband gigasample-per-second (GSPS) analog-to-digital converters offer many performance benefits to high-speed acquisition systems. These ADCs provide a wide frequency spectrum of visibility across high sample rates and input bandwidths. However, while some applications need a wideband front end, others require the ability to filter and tune to a narrower band of spectrum.

It can be inherently inefficient for an ADC to sample, process and burn the power to transmit a wideband spectrum, when only a narrow band is required in the application. An unnecessary system burden is created when the data link consumes a large bank of high-speed transceivers within a Xilinx® FPGA, only to then decimate and filter the wideband data in subsequent processing. The Xilinx FPGA transceiver resources can instead be better allocated to receive the lower bandwidth of interest and channelize the data from multiple ADCs. Additional filtering can be done within the FPGA's polyphase filter bank channelizer for frequency-division multiplexed (FDM) applications.

High-performance GSPS ADCs are now bringing the digital downconversion (DDC) function further up in the signal chain to reside within the ADC in a design solution based on Xilinx FPGAs. This approach offers several new design options to a high-speed system architect. However, because this function is relatively new to the ADC, there are design-related questions that engineers may have about the operation of the DDC blocks within GSPS ADCs. Let's clear up some of the more-common questions so that designers can begin using this new technique with more confidence.

To get the full performance benefit of DDCs, the design must also contain a filter-and-mixer component as a companion to the decimation.

WHAT IS DECIMATION?

In the simplest definition, decimation is the method of observing only a periodic subportion of the ADC output samples, while ignoring the rest. The result is to effectively reduce the sample rate of the ADC by downsampling. For example, a decimate-by-M mode in an ADC outputs only the first of Mth samples, while discarding all the other samples in between. This method continues to repeat for each multiple of M.

Sample decimation alone will only effectively reduce the sample rate of the ADC and correspondingly act as a low-pass filter. Without frequency translation and digital filtering, decimation will merely fold the harmonics of the fundamental and other spurious signals on top of one another in the frequency domain.

WHAT IS THE ROLE OF THE DDC?

Since decimation by itself does not prevent the folding of out-of-band signals, how does the DDC make this happen?

To get the full performance benefit of DDCs, the design must also contain a filter-and-mixer component that's used as a companion to the decimation function. Digital filtering effectively removes the out-of-band noise from the narrowly defined bandwidth that is set by the decimation ratio. The typical digital filter implementation for a DDC is a finite impulse response (FIR) filter. This filter is a function only of the past inputs, since there is no feedback. The passband of the filter should match the effective frequency spectrum width of the converter after the decimation.

HOW WIDE SHOULD THE DDC FILTERS BE?

The decimation ratios for DDCs are typically based on integer factors that are
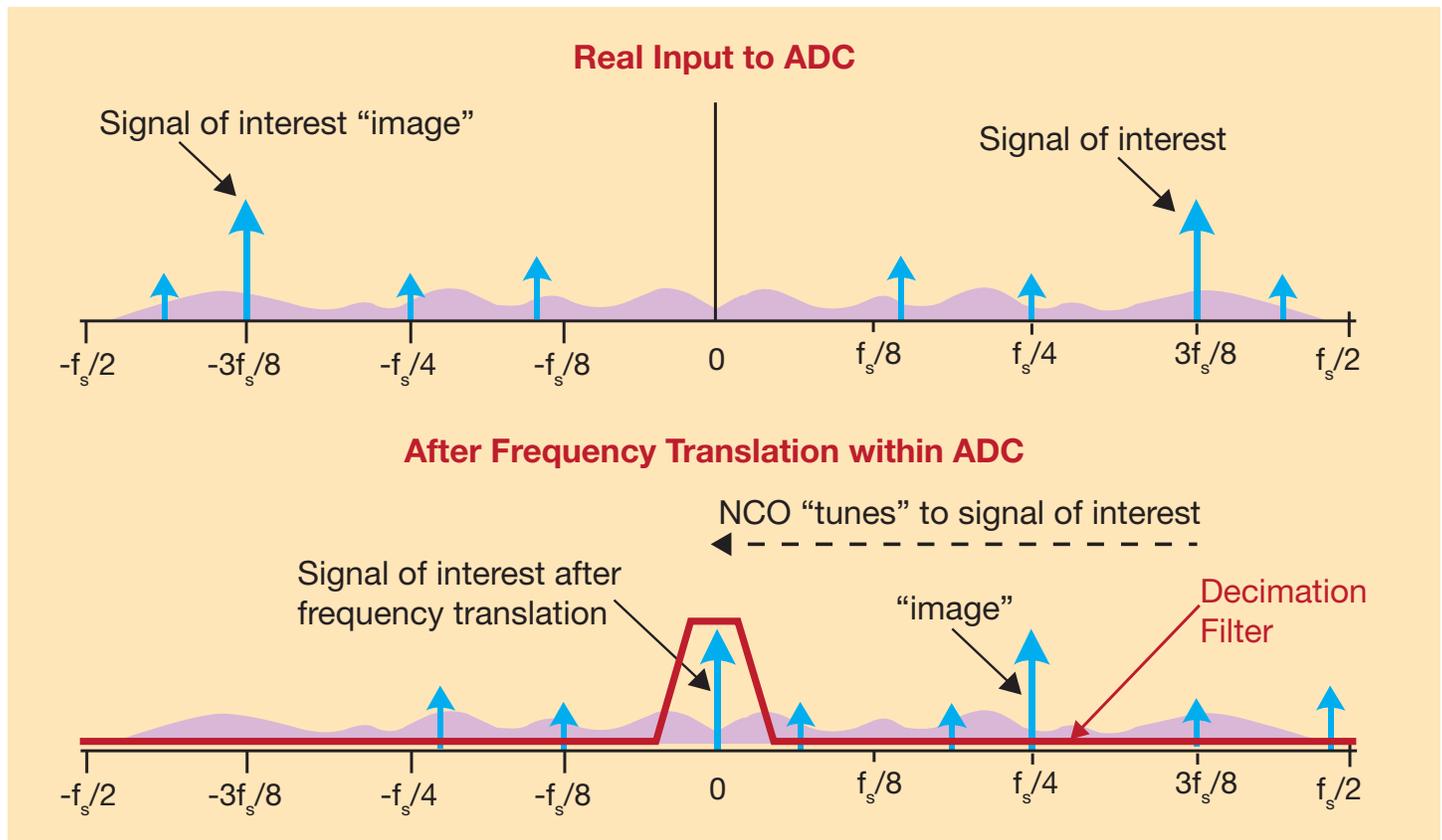
Figure 1 – Frequency translation using a low-pass filter and NCO effectively achieves a bandpass filter at the frequency of interest. Frequency planning ensures that unwanted harmonics, spurs and images fall out of band.
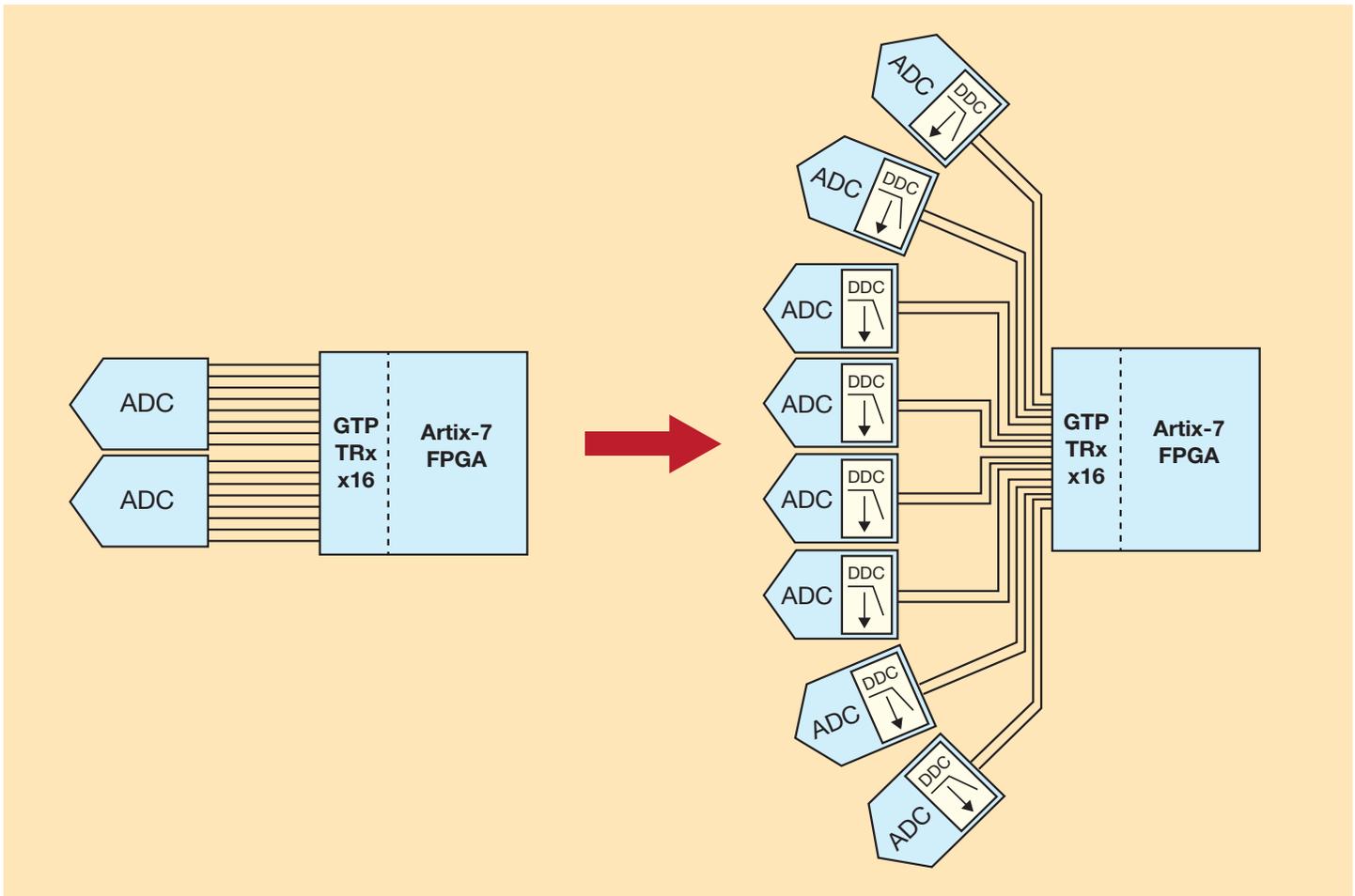
Figure 2 – The use of DDCs with a decimation factor of 8 allows the same 16 GTP 6.6-Gbps transceivers of the Xilinx Artix-7 to support eight ADCs with decimated I/Q data on two lanes of JESD204B each vs. only two ADCs that each output full bandwidth over eight lanes.

powers of 2 (2, 4, 8, 16, etc.). However, the decimation factor could actually be any ratio based on the DDC architecture, including fractional decimation. In the case of fractional decimation, an interpolation computation block is typically needed ahead of decimation to achieve a rational fraction ratio.

Ideally, the digital filter would precisely match the decimation frequency bandwidth and filter everything outside that band. However, a practical effective filter width will not exactly match to the full bandwidth of the decimation ratio. The filter width will therefore be some percentage of the decimation frequency, such as 85 percent or 90 percent. For example, the usable bandwidth of a decimation factor-of-8 filter may be practically the sample rate divided by 10, or $f_s/10$. The DDC filtering stage must provide a low passband ripple and a high stopband alias rejection.

IS THE FREQUENCY FIXED?

The next question is whether the DDC filters are fixed in frequency, or if they can be tuned and centered on a particular band of interest.

We have discussed the decimation and filtering stages of DDCs. But this is only valuable if the desired frequency is within the filter passband from DC. If that is not the case, then we need a way to tune the filter to a different part of the frequency spectrum to observe the signal of interest. The narrow bandwidth can be tuned within the first or second Nyquist zone by a numerically controlled oscillator (NCO). An NCO offers a method to tune and mix the filter band to a different portion of the wideband spectrum (Figure 1).

A digital tuning word provides a fractional divider of the sample rate with a frequency placement resolution defined by the number of bits used in the digital tuning word that allows the band of interest to be mixed. The tuning word has the tuning range and resolution to place the filter where it is needed. A typical NCO tuning word may be up to 48 bits of resolution across two Nyquist bands of the sampled frequency, which is adequate for most applications.

The NCO is accompanied by a mixer. Operating much like an analog quadrature mixer, this device performs the downconversion of real and complex input signals by using the NCO frequency as a local oscillator.

The filter follows the frequency translation stage. After the carrier band of interest is tuned down to DC, the filter effectively lowers the sample rate while providing sufficient alias rejection from unwanted adjacent carriers around the tuned bandwidth of interest.

The use of a single decimate-by-8 DDC allows the same Xilinx Artix-7 FPGA system to support four times more ADCs.

When mixing a real input signal down to baseband, 6 dB of signal loss is introduced due to the filtering of the negative image. The NCO introduces an additional small insertion loss. The total loss of a real input signal mixed down to baseband is typically slightly more than 6 dB. The NCO allows the input spectrum to be tuned to dc, where it can be effectively filtered by the subsequent filter blocks to prevent aliasing. The DDC may also contain an independently controlled digital gain stage. A gain stage allows the system to enable +6 dB or more of gain to center the dynamic range of the signal within the full scale of the output bits.

INTERPROCESSOR INTERRUPTS

The decimation of the ADC samples removes the need to send unwanted information downstream in the signal chain to eventually get discarded anyway. Therefore, since this data is filtered out, it reduces the output data bandwidth needed on the back end of the ADC. This amount of reduction is offset by the increase in data from both the I/Q data output. For example, a decimate-by-16 filter with both I and Q data would reduce the wideband output data by a factor of 8.

This minimized data rate reduces the complexity of system layout by lowering the number of output JESD204B lanes from the ADC. The reduction in ADC output bandwidth can allow the design of a compact system that otherwise may not be achievable. For example, in a case where system power and size limit

a board to using a single FPGA, the number of high-speed serial transceivers supported can limit the number of ADCs without the use of DDCs.

For a case where only a narrow bandwidth is observed in this system, decimation within the ADCs helps remove this limitation. The use of a single decimate-by-8 DDC allows the same Xilinx Artix®-7 FPGA system to support four times more ADCs by reducing the output bandwidth of the ADCs to just two output data lanes. For this particular case, as many as eight ADCs using DDCs could now be designed with the same existing 16 GTP transceivers in the Artix-7 FPGA (Figure 2). This allows more efficient use of Xilinx FPGA resources as a multichannel digital receiver for a set of FDM channels.

DO DDC FILTERS AFFECT SNR AND SFDR?

The next question to examine is how the analog performance of signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) change when the DDC filters are on vs. when they are off.

Since the wideband noise of the converter is filtered out and only a narrow spectrum is observed, we should expect the signal power relative to the observed noise to be higher. The dynamic range of the ADC will be better within the passband of the filter. The improved SNR by use of the DDC is inherently an advantage of decimating and filtering the wideband spectrum.

Digital filtering by the DDC is used to filter the noise outside of a smaller

bandwidth. The SNR calculation of the ADC must then include a correction factor for this filtering that accounts for the processing gain of the filtered noise. Using a perfect digital filter, for every power-of-two reduction in bandwidth, the processing gain due to the filtered noise will increase by +3 dB:

Ideal SNR (with processing gain) = 6.02*N + 1.76 dB + 10log10(fs/(2*BW))

A distinct advantage of using DDCs is the ability to have the harmonics of the fundamental signal fall outside the band of interest. With proper frequency planning, digital filtering will prevent the harmonics from being seen within the narrow DDC bandwidth and therefore will increase the SFDR performance of the system.

In the systems where only a narrow bandwidth is needed, a DDC provides ADC processing gain by filtering out the wideband noise. This increases the signal-to-noise ratio seen within the bandwidth of interest. An additional benefit is that, with proper frequency planning, the typically dominant second- and third-order harmonics of the fundamental fall outside the tuned bandwidth of interest and are digitally filtered. This increases the SFDR of the system.

Sampling theorems dictate that harmonics or other higher-order system spurs can fold back around the end of each Nyquist band. This is also true for DDCs, which have the potential for unwanted second- or third-order harmonics to fold back into the passband and decrease the SFDR. Therefore, to navigate around such

sampling problems, you should implement your system frequency plan for the DDC passband filter width and NCO tuning position.

ARE EXTERNAL FILTERS REQUIRED?

System ADCs using internal DDCs can use additional analog filters, as would normally be done without DDC filtering. For wideband applications, the DDCs provide some relaxation in the filtering that's needed at the front end of the ADC.

The digital filtering within the DDC will do some of the work and relax what otherwise would require a strict front-end anti-alias analog filter. However, a wideband front end will now allow multiple uses for the DDC to either observe multiple bands simultaneously or even sweep the band of interest with the NCO to find a changing input signal.

CAN AN ADC PROVIDE MULTIPLE DDCS?

The final question for engineers contemplating internal digital downconversion with an FPGA is whether an ADC provides just one DDC. The answer is no; in fact, multiple bands can be observed.

For multiple DDCs within an ADC, each can have its own NCO that tunes to separate bands across the Nyquist zone. This scheme makes it possible to observe multiple frequency bands simultaneously and removes the burden on the system FPGA transceiver count and decimation blocks, which can be reassigned to other processing activities such as channelizing multiple ADCs for FDM systems.

High-speed ADCs now have the processing power to bring the DDC function up the signal chain. For those systems that do not need to use the full bandwidth of a wideband Nyquist-rate ADC, the DDC operation filters the unwanted data and noise. This can improve the SNR and SFDR of the signal acquisition. The lower bandwidth reduces the data interface burden to the transceivers of an FPGA, like Artix-7, and allows for the design of more-complex signal-acquisition systems.