AC701 EVALUATION BOARD HW-A7-AC701
(XC7A200T-FBG676)

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SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DISCLAIMER		
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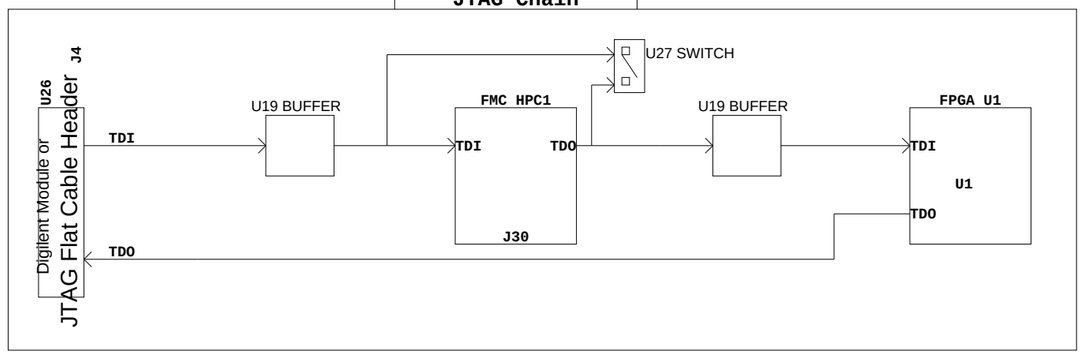
JTAG Chain



IIC Addressing

0b1110100	PCA9548a
0b1011101	SI570
0bxxxxx00	FMC HPC 1
0b1010100	IIC EEPROM
0b1010000	SFP+
0b0111001	ADV7511
0b1010000 0b0011000	DDR3 SODIMM
0b1010000	SI5324

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ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
BLOCK DIAGRAM

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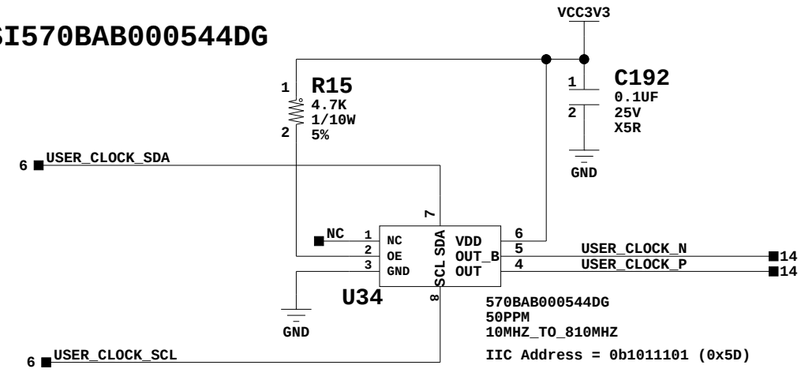
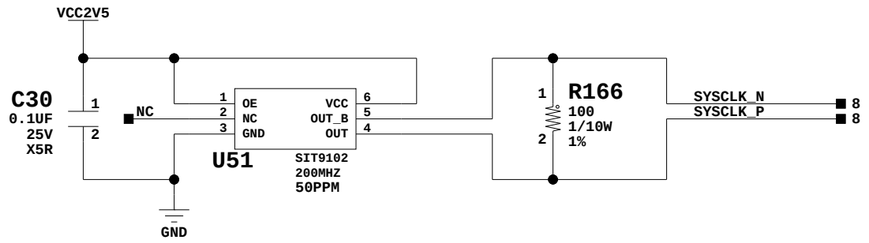
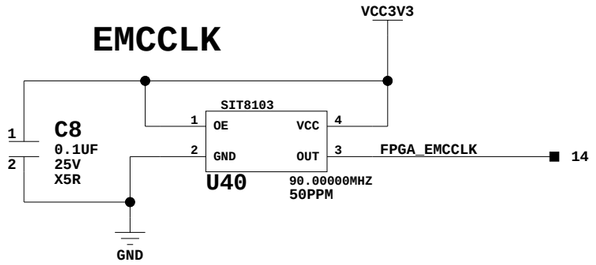
SI570BAB000544DG

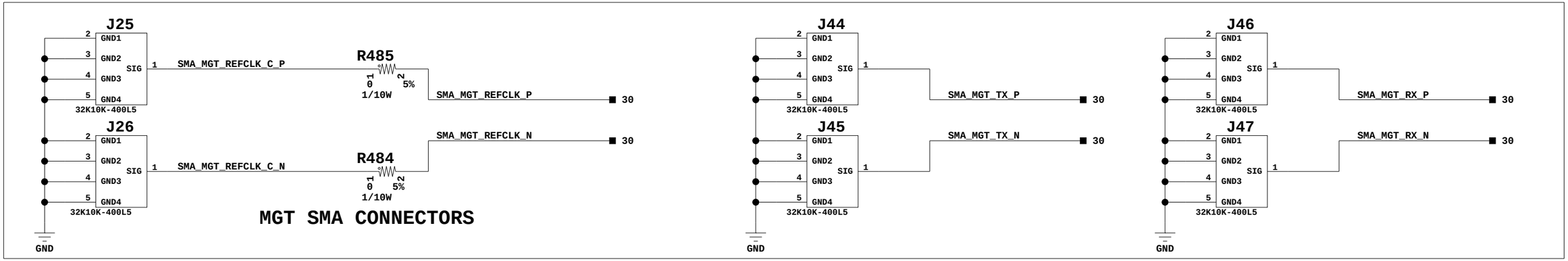


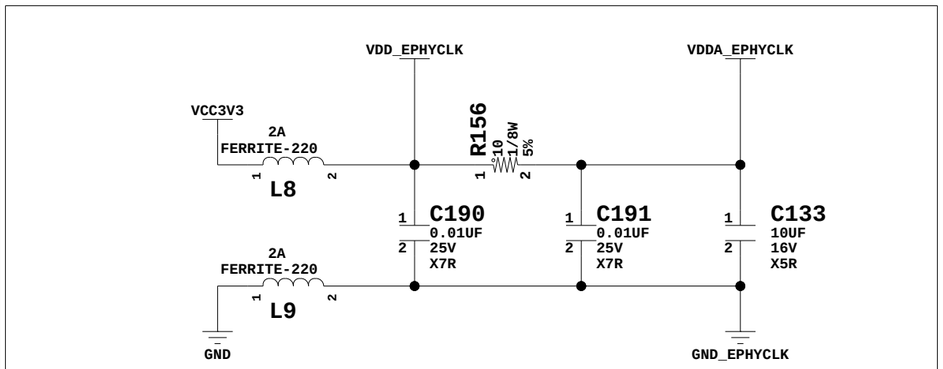
SIT9102AI-243N25E200.0000

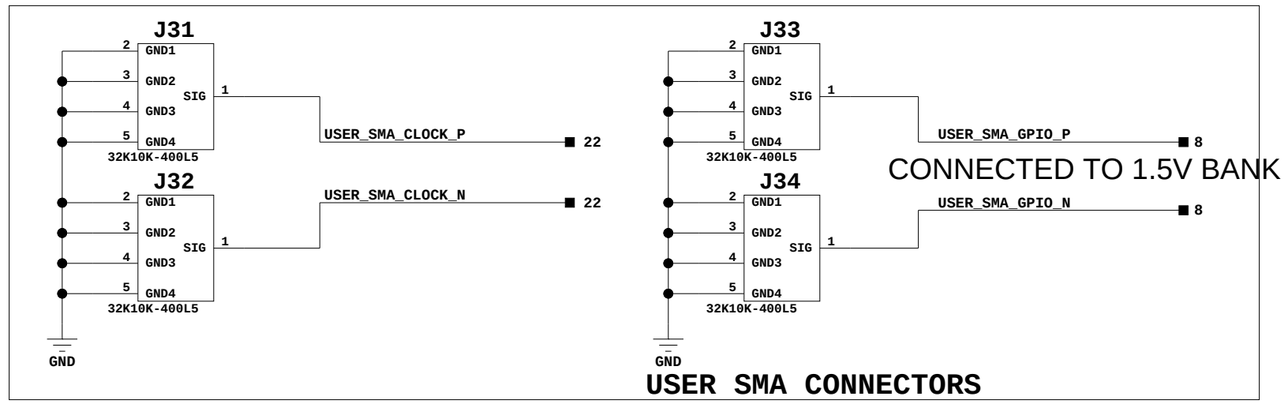


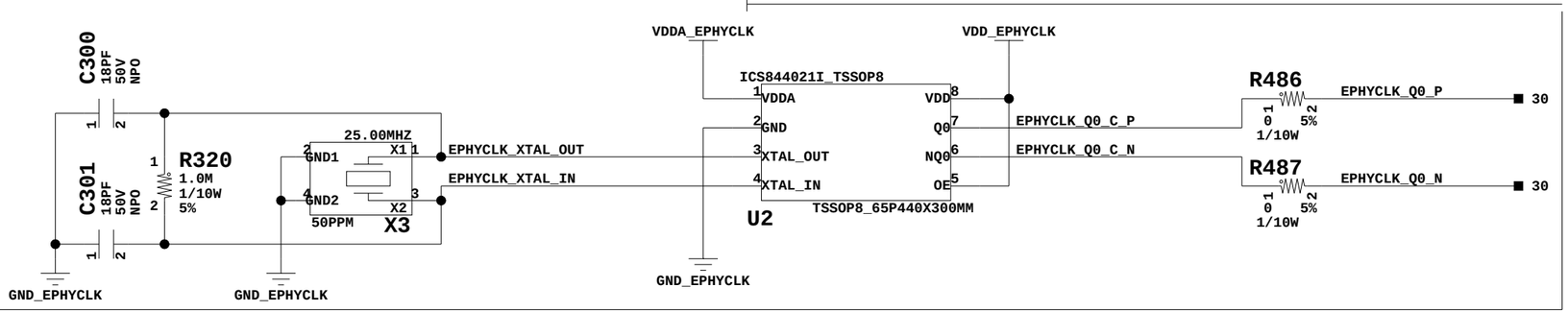
EMCCLK











Clocks

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PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD CLOCKS		
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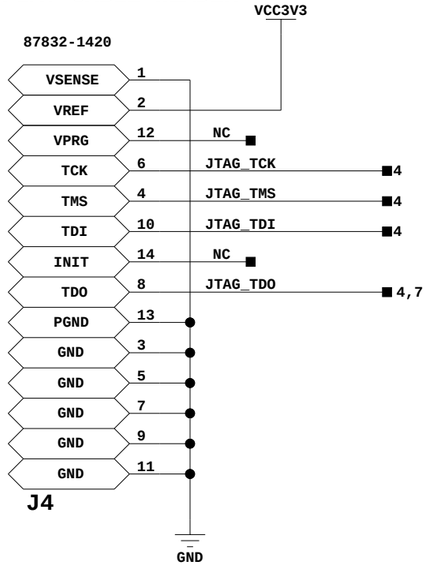
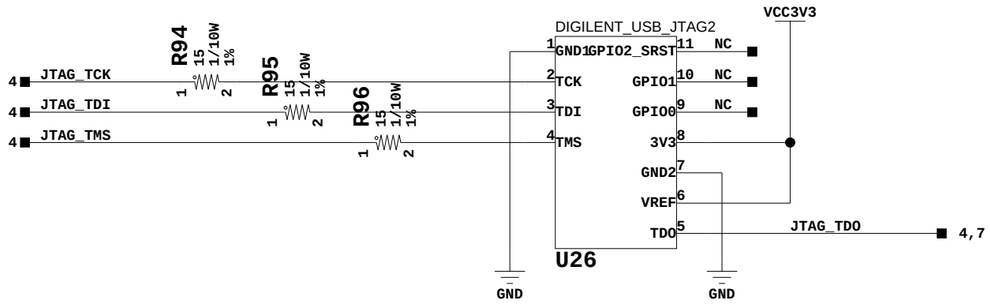
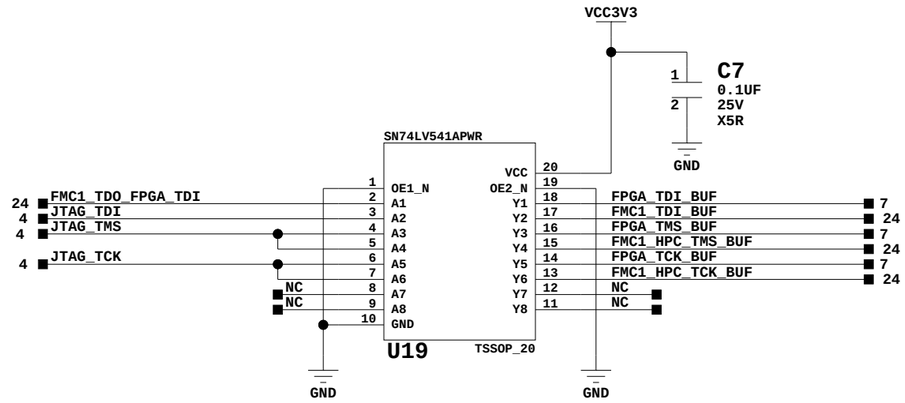
JTAG FLAT-CABLE HEADER

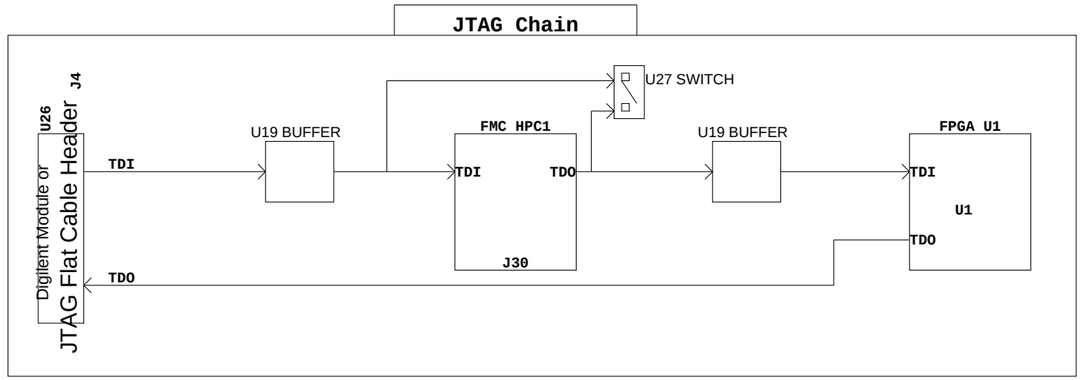


USB JTAG DIGILENT MODULE



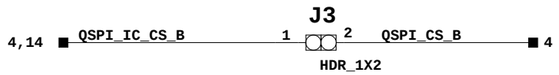


JTAG Chain

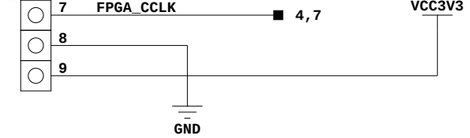


ON = SPI DEVICE

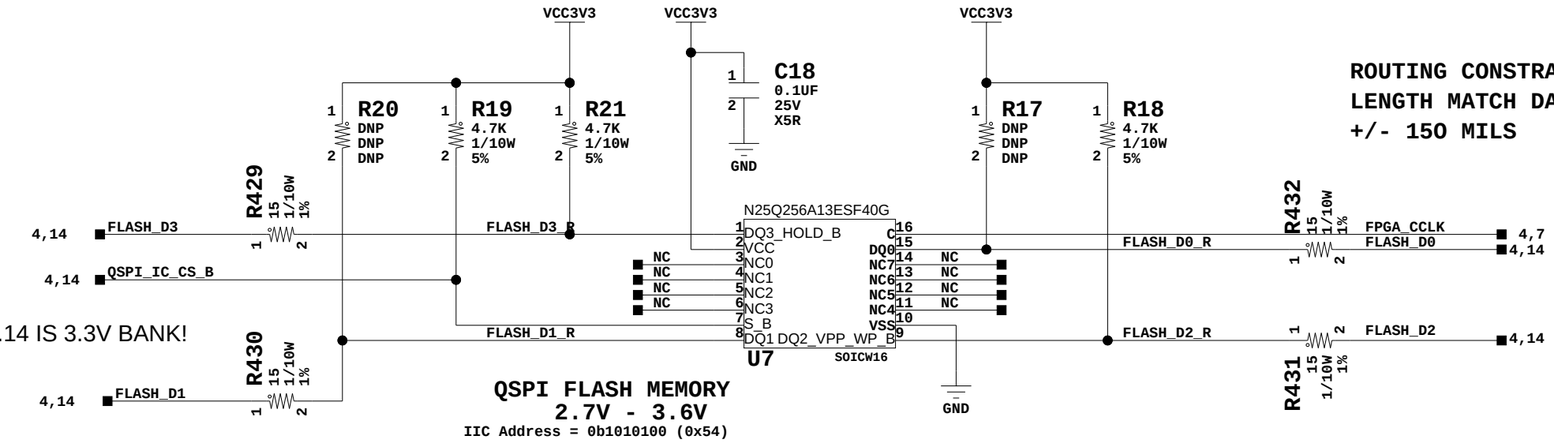
OFF = SPI EXTERNAL



SPI SELECT JUMPER



SPI EXTERNAL
PROGRAMMING HEADER



QSPI FLASH MEMORY
2.7V - 3.6V
IIC Address = 0b1010100 (0x54)

PG.14 IS 3.3V BANK!

ROUTING CONSTRAINT:
LENGTH MATCH DATA AND CLOCK
+/- 150 MILS

FPGA Configuration Options

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD CONFIGURATION		
Date:	9-20-2012_14:39	Ver:	1.0
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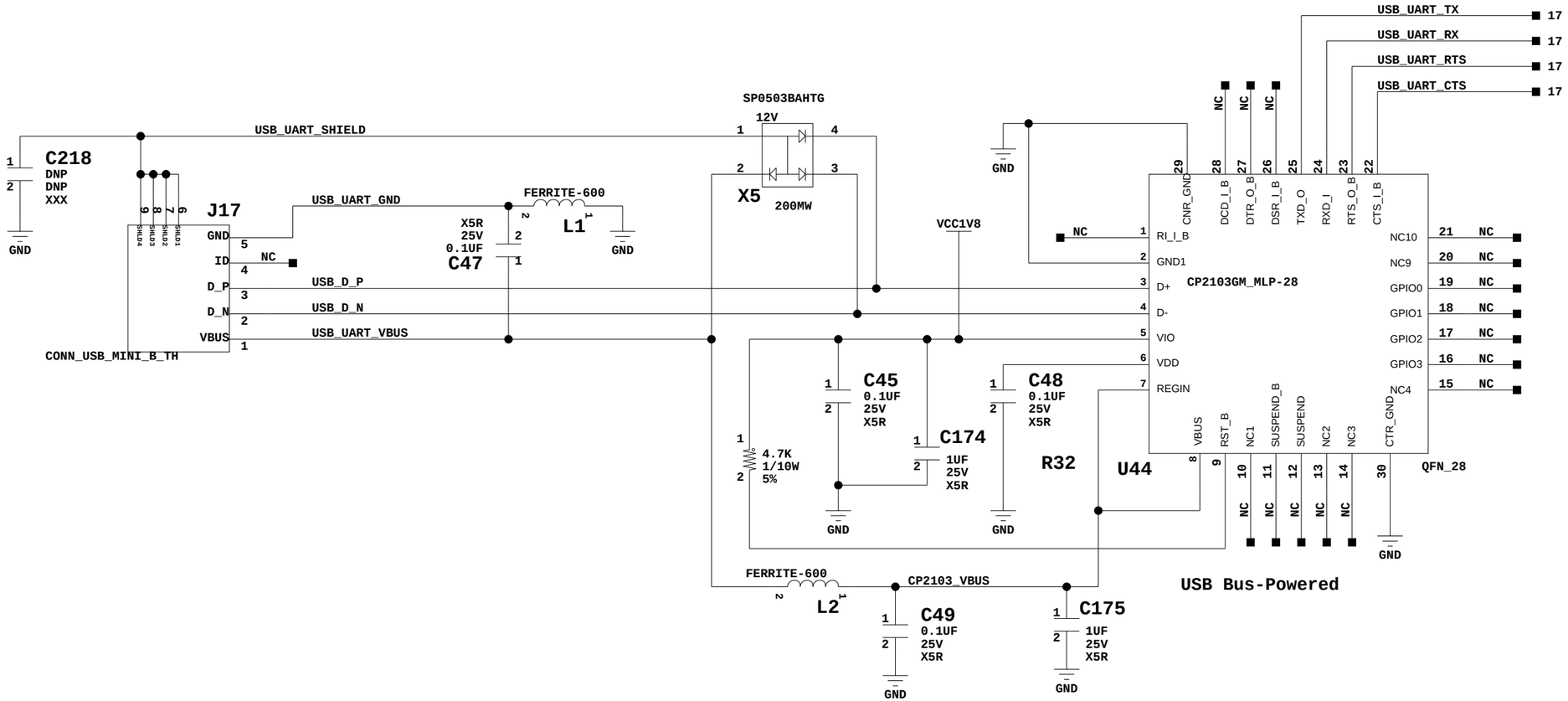

USB UART

XILINX	ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD USB-to-UART BRIDGE
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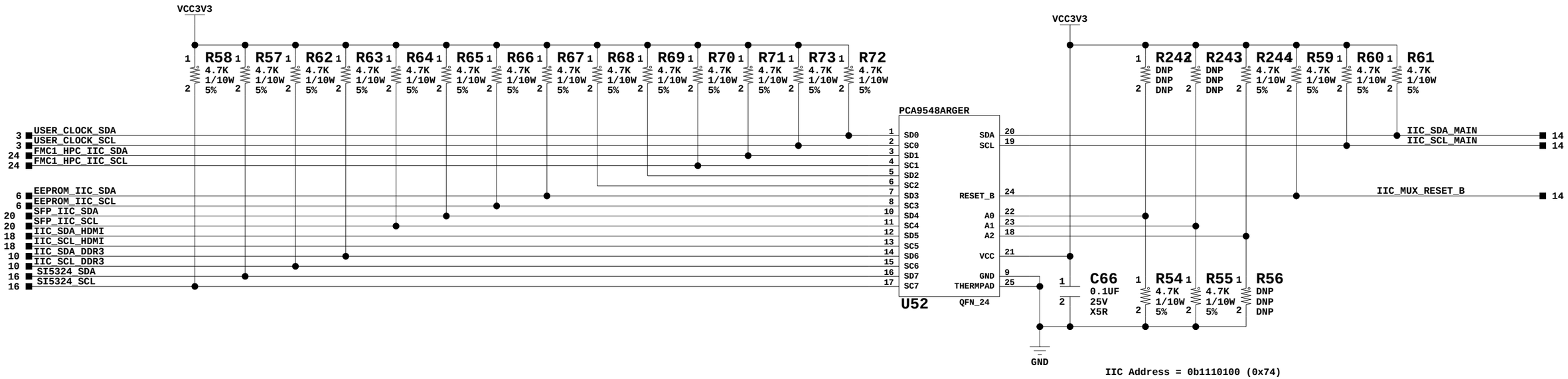

IIC MUX, EEPROM

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD IIC MUX and EEPROM		
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TP FOR INT, DONE TIMING MEASUREMENT

SOC_IRON_FG676

BANK 0
XC7A200TFBG676

U1

SOC_IRON_FG676

DXN_0_R11	R11	XADC_DXN 29
VCCADC_0_M12	M12	XADC_VCC 29
GNDADC_0_M11	M11	
DXP_0_R12	R12	XADC_DXP 29
VREFN_0_N11	N11	
VREFP_0_P12	P12	XADC_VREFP 29
VP_0_N12	N12	XADC_VP_R_P 29
VN_0_P11	P11	XADC_VN_R_N 29
VCCBATT_0_G14	G14	FPGA_VBATT 7
CCLK_0_H13	H13	FPGA_CCLK 4
TCK_0_H12	H12	FPGA_TCK_BUF 4
TMS_0_H11	H11	FPGA_TMS_BUF 4
TDO_0_J10	J10	JTAG_TDO 4
TDI_0_H10	H10	FPGA_TDI_BUF 4
INIT_B_0_V11	V11	FPGA_INIT_B 7
PROGRAM_B_0_AE16	AE16	FPGA_PROG_B 4,7
CFGBVS_0_AB15	AB15	CFGBVS
DONE_0_W10	W10	FPGA_DONE 7
M2_0_W9	W9	FPGA_M2 7
M0_0_AB7	AB7	FPGA_M0 7
M1_0_Y9	Y9	FPGA_M1 7

FPGA_3V3

Y14 VCCO_0_Y14
W11 VCCO_0_W11

HDR_1X2
J52

FPGA_3V3

R233
DNP
DNP
DNP

C1 0.1UF 25V X5R
C2 0.1UF 25V X5R
C217 DNP DNP XXX

XADC_AGND
GND

FPGA_3V3
C163 100UF 6.3 X5R
GND

FPGA_3V3
R42 4.7K 1/10W 5%
4,7 FPGA_PROG_B
Pushbutton TL3301EF100QG
SW9
GND

FPGA_3V3
R469 4.7K 1/10W 5%
7 FPGA_INIT_B
SN74AVC1T45
U66 SC70_6
VCCB VCCA DIR GND
VCC3V3
GND GND

R306 261 1/10W 1%
R307 261 1/10W 1%
DS1 RED GRN LED-GRN-RED
VCC3V3
GND

VCC3V3
R396 261 1/10W
7 FPGA_DONE
LED-GRN-SMT
DS10
GND

VCC1V8
D6 BAS40-04 40V 200MW
NC
R83 4.7K 1/10W 5%
7 FPGA_VBATT
B1 1.5V SEIKO TS518FE_FL35E
GND

FPGA_3V3
SDA03H1SBD
SW1
7 FPGA_M2
7 FPGA_M1
7 FPGA_M0
NC
R339 1.21K 1/10W 1%
R338 1.21K 1/10W 1%
R337 1.21K 1/10W 1%
GND

Encryption Key Battery B1
FPGA Bank 0, Prog. PB, INIT LED

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ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANK0, PROG.PB,INIT LED		
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SOC_IRON_FG676

BANK 34
XC7A200TFBG676

IO_0_34_N8	N8	DDR3_RESET_B	
IO_L1P_T0_34_K3	K3	DDR3_A9	10
IO_L1N_T0_34_J3	J3	DDR3_A1	10
IO_L2P_T0_34_M7	M7	DDR3_A5	10
IO_L2N_T0_34_L7	L7	DDR3_A12	10
IO_L3P_T0_DQS_34_M4	M4	DDR3_A0	10
IO_L3N_T0_DQS_34_L4	L4	DDR3_A3	10
IO_L4P_T0_34_L5	L5	DDR3_A11	10
IO_L4N_T0_34_K5	K5	DDR3_A4	10
IO_L5P_T0_34_N7	N7	DDR3_A10	10
IO_L5N_T0_34_N6	N6	DDR3_A13	10
IO_L6P_T0_34_M6	M6	DDR3_A7	10
IO_L6N_T0_VREF_34_M5	M5		
IO_L7P_T1_34_K1	K1	DDR3_A6	
IO_L7N_T1_34_J1	J1	DDR3_A2	10
IO_L8P_T1_34_L3	L3	DDR3_A14	10
IO_L8N_T1_34_K2	K2	DDR3_A15	10
IO_L9P_T1_DQS_34_N1	N1	DDR3_BA0	10
IO_L9N_T1_DQS_34_M1	M1	DDR3_BA1	10
IO_L10P_T1_34_H2	H2	DDR3_BA2	10
IO_L10N_T1_34_H1	H1	DDR3_A8	10
IO_L11P_T1_SRCC_34_M2	M2	DDR3_CLK0_P	10
IO_L11N_T1_SRCC_34_L2	L2	DDR3_CLK0_N	10
IO_L12P_T1_MRCC_34_N3	N3	DDR3_CLK1_P	10
IO_L12N_T1_MRCC_34_N2	N2	DDR3_CLK1_N	10
IO_L13P_T2_MRCC_34_R3	R3	SYSCLK_P	3
IO_L13N_T2_MRCC_34_P3	P3	SYSCLK_N	3
IO_L14P_T2_SRCC_34_P4	P4	DDR3_CKE0	10
IO_L14N_T2_SRCC_34_N4	N4	DDR3_CKE1	10
IO_L15P_T2_DQS_34_R1	R1	DDR3_WE_B	10
IO_L15N_T2_DQS_34_P1	P1	DDR3_RAS_B	10
IO_L16P_T2_34_T4	T4	DDR3_CAS_B	10
IO_L16N_T2_34_T3	T3	DDR3_S0_B	10
IO_L17P_T2_34_T2	T2	DDR3_S1_B	10
IO_L17N_T2_34_R2	R2	DDR3_ODT0	10
IO_L18P_T2_34_U2	U2	DDR3_ODT1	10
IO_L18N_T2_34_U1	U1	DDR3_TEMP_EVENT	10
IO_L19P_T3_34_P6	P6	GPIO_SW_N	21
IO_L19N_T3_VREF_34_P5	P5		
IO_L20P_T3_34_T5	T5	GPIO_SW_S	21
IO_L20N_T3_34_R5	R5	GPIO_SW_W	21
IO_L21P_T3_DQS_34_U6	U6	GPIO_SW_C	21
IO_L21N_T3_DQS_34_U5	U5	GPIO_SW_E	21
IO_L22P_T3_34_R8	R8	GPIO_DIP_SW0	21
IO_L22N_T3_34_P8	P8	GPIO_DIP_SW1	21
IO_L23P_T3_34_R7	R7	GPIO_DIP_SW2	21
IO_L23N_T3_34_R6	R6	GPIO_DIP_SW3	21
IO_L24P_T3_34_T8	T8	USER_SMA_GPIO_P	3
IO_L24N_T3_34_T7	T7	USER_SMA_GPIO_N	3
IO_25_34_U4	U4	CPU_RESET	21

VTTVREF

C462 0.1UF 25V X5R — 1: VTTVREF, 2: GND

C491 0.1UF 25V X5R — 1: VTTVREF, 2: GND

FPGA_1V5

T6	VCCO_34_T6	
P2	VCCO_34_P2	
N5	VCCO_34_N5	
M8	VCCO_34_M8	
L1	VCCO_34_L1	
K4	VCCO_34_K4	

U1 SOC_IRON_FG676

SOC_IRON_FG676

BANK 35
XC7A200TFBG676

IO_0_35_J8	J8	NC	
IO_L1P_T0_AD4P_35_E6	E6	DDR3_D63	10,12
IO_L1N_T0_AD4N_35_D6	D6	DDR3_D62	10,12
IO_L2P_T0_AD12P_35_H8	H8	DDR3_D61	10,12
IO_L2N_T0_AD12N_35_G8	G8	DDR3_D60	10,12
IO_L3P_T0_DQS_AD5P_35_H7	H7	DDR3_DQS7_P	10,12
IO_L3N_T0_DQS_AD5N_35_G7	G7	DDR3_DQS7_N	10,12
IO_L4P_T0_35_F8	F8	DDR3_D59	10,12
IO_L4N_T0_35_F7	F7	DDR3_D58	10,12
IO_L5P_T0_AD13P_35_H6	H6	DDR3_D57	10,12
IO_L5N_T0_AD13N_35_G6	G6	DDR3_D56	10,12
IO_L6P_T0_35_H9	H9	DDR3_DM7	10
IO_L6N_T0_VREF_35_G9	G9		
IO_L7P_T1_AD6P_35_J6	J6	DDR3_D55	
IO_L7N_T1_AD6N_35_J5	J5	DDR3_D54	10,12
IO_L8P_T1_AD14P_35_L8	L8	DDR3_D53	10,12
IO_L8N_T1_AD14N_35_K8	K8	DDR3_D52	10,12
IO_L9P_T1_DQS_AD7P_35_J4	J4	DDR3_DQS6_P	10,12
IO_L9N_T1_DQS_AD7N_35_H4	H4	DDR3_DQS6_N	10,12
IO_L10P_T1_AD15P_35_K7	K7	DDR3_D51	10,12
IO_L10N_T1_AD15N_35_K6	K6	DDR3_D50	10,12
IO_L11P_T1_SRCC_35_G4	G4	DDR3_D49	10,12
IO_L11N_T1_SRCC_35_F4	F4	DDR3_D48	10,12
IO_L12P_T1_MRCC_35_G5	G5	DDR3_DM6	10
IO_L12N_T1_MRCC_35_F5	F5	NC	
IO_L13P_T2_MRCC_35_E5	E5	DDR3_D47	
IO_L13N_T2_MRCC_35_D5	D5	DDR3_D46	10,12
IO_L14P_T2_SRCC_35_D4	D4	DDR3_D45	10,12
IO_L14N_T2_SRCC_35_C4	C4	DDR3_D44	10,12
IO_L15P_T2_DQS_35_B5	B5	DDR3_DQS5_P	10,12
IO_L15N_T2_DQS_35_A5	A5	DDR3_DQS5_N	10,12
IO_L16P_T2_35_B4	B4	DDR3_D43	10,12
IO_L16N_T2_35_A4	A4	DDR3_D42	10,12
IO_L17P_T2_35_D3	D3	DDR3_D41	10,12
IO_L17N_T2_35_C3	C3	DDR3_D40	10,12
IO_L18P_T2_35_F3	F3	DDR3_DM5	10
IO_L18N_T2_35_E3	E3	NC	
IO_L19P_T3_35_C2	C2	DDR3_D39	10,12
IO_L19N_T3_VREF_35_B2	B2		
IO_L20P_T3_35_A3	A3	DDR3_D38	10,12
IO_L20N_T3_35_A2	A2	DDR3_D37	10,12
IO_L21P_T3_DQS_35_C1	C1	DDR3_DQS4_P	10,12
IO_L21N_T3_DQS_35_B1	B1	DDR3_DQS4_N	10,12
IO_L22P_T3_35_F2	F2	DDR3_D36	10,12
IO_L22N_T3_35_E2	E2	DDR3_D35	10,12
IO_L23P_T3_35_E1	E1	DDR3_D34	10,12
IO_L23N_T3_35_D1	D1	DDR3_D33	10,12
IO_L24P_T3_35_G2	G2	DDR3_D32	10,12
IO_L24N_T3_35_G1	G1	DDR3_DM4	10
IO_25_35_H3	H3	NC	

VTTVREF

C463 0.1UF 25V X5R — 1: VTTVREF, 2: GND

C492 0.1UF 25V X5R — 1: VTTVREF, 2: GND

FPGA_1V5

J7	VCCO_35_J7	
G3	VCCO_35_G3	
F6	VCCO_35_F6	
D2	VCCO_35_D2	
C5	VCCO_35_C5	
A1	VCCO_35_A1	

U1 SOC_IRON_FG676

FPGA_1V5

C158 100UF 6.3 X5R — 1: FPGA_1V5, 2: GND

FPGA_1V5

C402 100UF 6.3 X5R — 1: FPGA_1V5, 2: GND

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANKS34,35 DDR3 SODIMM IF		
Date:	9-20-2012_14:39	Ver:	1.0
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XC7A200T-FBG676 ONLY

SOC_IRON_FG676

BANK 33
XC7A200TFBG676

IO_0_33_V4	V4	NC	
IO_L1P_T0_33_V1	V1	DDR3_D31	10,11
IO_L1N_T0_33_W1	W1	DDR3_D30	10,11
IO_L2P_T0_33_W5	W5	DDR3_D29	10,11
IO_L2N_T0_33_W4	W4	DDR3_D28	10,11
IO_L3P_T0_DQS_33_V3	V3	DDR3_DQS3_P	10,11
IO_L3N_T0_DQS_33_V2	V2	DDR3_DQS3_N	10,11
IO_L4P_T0_33_V6	V6	DDR3_D27	10,11
IO_L4N_T0_33_W6	W6	DDR3_D26	10,11
IO_L5P_T0_33_W3	W3	DDR3_D25	10,11
IO_L5N_T0_33_Y3	Y3	DDR3_D24	10,11
IO_L6P_T0_33_U7	U7	DDR3_DM3	10
IO_L6N_T0_VREF_33_V7	V7		
IO_L7P_T1_33_AB1	AB1	DDR3_D23	
IO_L7N_T1_33_AC1	AC1	DDR3_D22	10,11
IO_L8P_T1_33_Y2	Y2	DDR3_D21	10,11
IO_L8N_T1_33_Y1	Y1	DDR3_D20	10,11
IO_L9P_T1_DQS_33_AD1	AD1	DDR3_DQS2_P	10,11
IO_L9N_T1_DQS_33_AE1	AE1	DDR3_DQS2_N	10,11
IO_L10P_T1_33_AE2	AE2	DDR3_D19	10,11
IO_L10N_T1_33_AF2	AF2	DDR3_D18	10,11
IO_L11P_T1_SRCC_33_AB2	AB2	DDR3_D17	10,11
IO_L11N_T1_SRCC_33_AC2	AC2	DDR3_D16	10,11
IO_L12P_T1_MRCC_33_AA3	AA3	DDR3_DM2	10
IO_L12N_T1_MRCC_33_AA2	AA2	NC	
IO_L13P_T2_MRCC_33_AA4	AA4	DDR3_D15	
IO_L13N_T2_MRCC_33_AB4	AB4	DDR3_D14	10,11
IO_L14P_T2_SRCC_33_AC3	AC3	DDR3_D13	10,11
IO_L14N_T2_SRCC_33_AD3	AD3	DDR3_D12	10,11
IO_L15P_T2_DQS_33_AD5	AD5	DDR3_DQS1_P	10,11
IO_L15N_T2_DQS_33_AE5	AE5	DDR3_DQS1_N	10,11
IO_L16P_T2_33_AE3	AE3	DDR3_D11	10,11
IO_L16N_T2_33_AF3	AF3	DDR3_D10	10,11
IO_L17P_T2_33_AF5	AF5	DDR3_D9	10,11
IO_L17N_T2_33_AF4	AF4	DDR3_D8	10,11
IO_L18P_T2_33_AC4	AC4	DDR3_DM1	10
IO_L18N_T2_33_AD4	AD4	NC	
IO_L19P_T3_33_Y7	Y7	DDR3_D7	10,11
IO_L19N_T3_VREF_33_AA7	AA7		
IO_L20P_T3_33_Y6	Y6	DDR3_D6	
IO_L20N_T3_33_Y5	Y5	DDR3_D5	10,11
IO_L21P_T3_DQS_33_V8	V8	DDR3_DQS0_P	10,11
IO_L21N_T3_DQS_33_W8	W8	DDR3_DQS0_N	10,11
IO_L22P_T3_33_AA5	AA5	DDR3_D4	10,11
IO_L22N_T3_33_AB5	AB5	DDR3_D3	10,11
IO_L23P_T3_33_Y8	Y8	DDR3_D2	10,11
IO_L23N_T3_33_AA8	AA8	DDR3_D1	10,11
IO_L24P_T3_33_AB6	AB6	DDR3_D0	10,11
IO_L24N_T3_33_AC6	AC6	DDR3_DM0	10
IO_25_33_V9	V9	NC	

VTTVREF

C461 1 2 0.1UF 25V X5R

C490 1 2 0.1UF 25V X5R

GND

FPGA_1V5

Y4	VCCO_33_Y4
W7	VCCO_33_W7
U3	VCCO_33_U3
AD2	VCCO_33_AD2
AC5	VCCO_33_AC5
AA1	VCCO_33_AA1

U1

SOC_IRON_FG676

FPGA_1V5

C157 1 2 100UF 6.3 X5R

GND

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANK33, DDR3 SODIMM IF		
Date:	9-20-2012_14:39	Ver:	1.0
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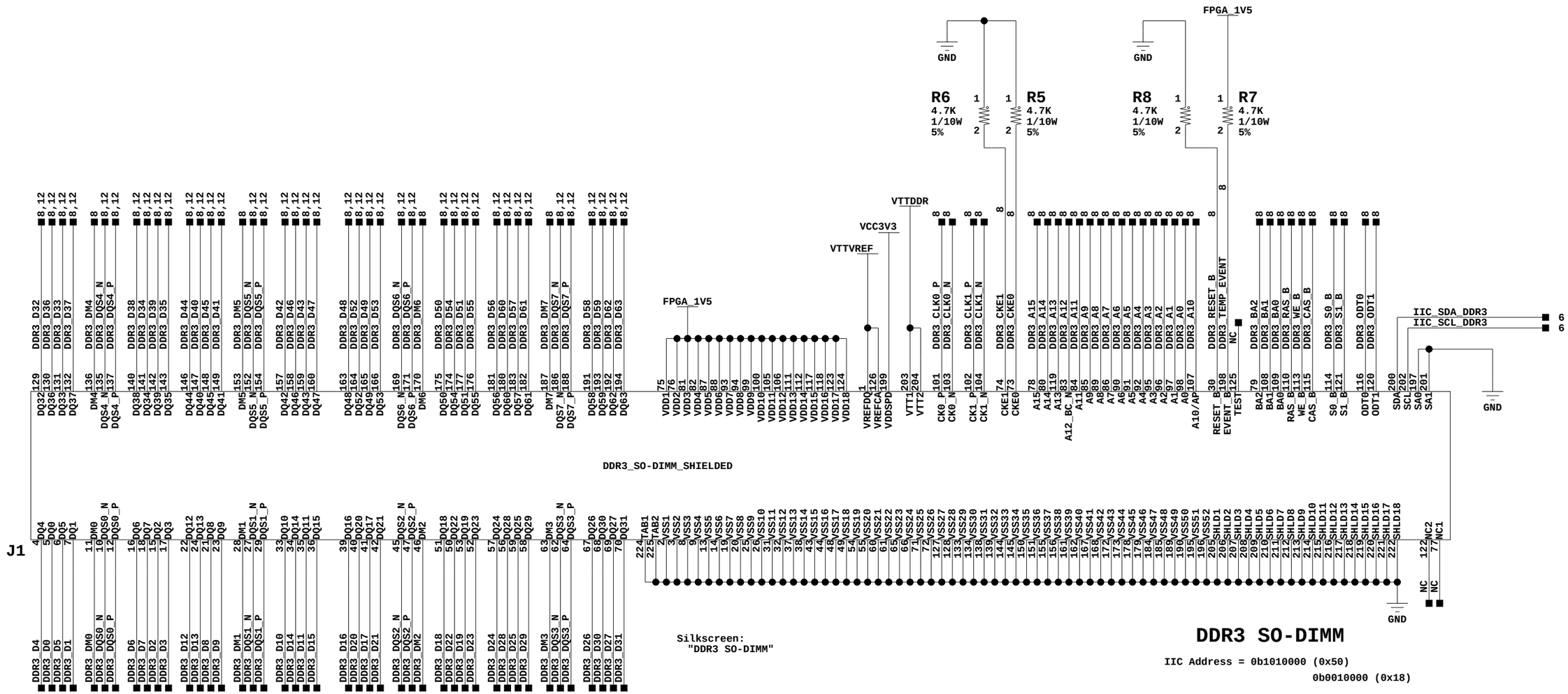

DDR3 SO-DIMM

IIC Address = 0b1010000 (0x50)
0b0010000 (0x18)

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM SOCKET J1		
Date:	9-20-2012_14:39	Ver:	1.0
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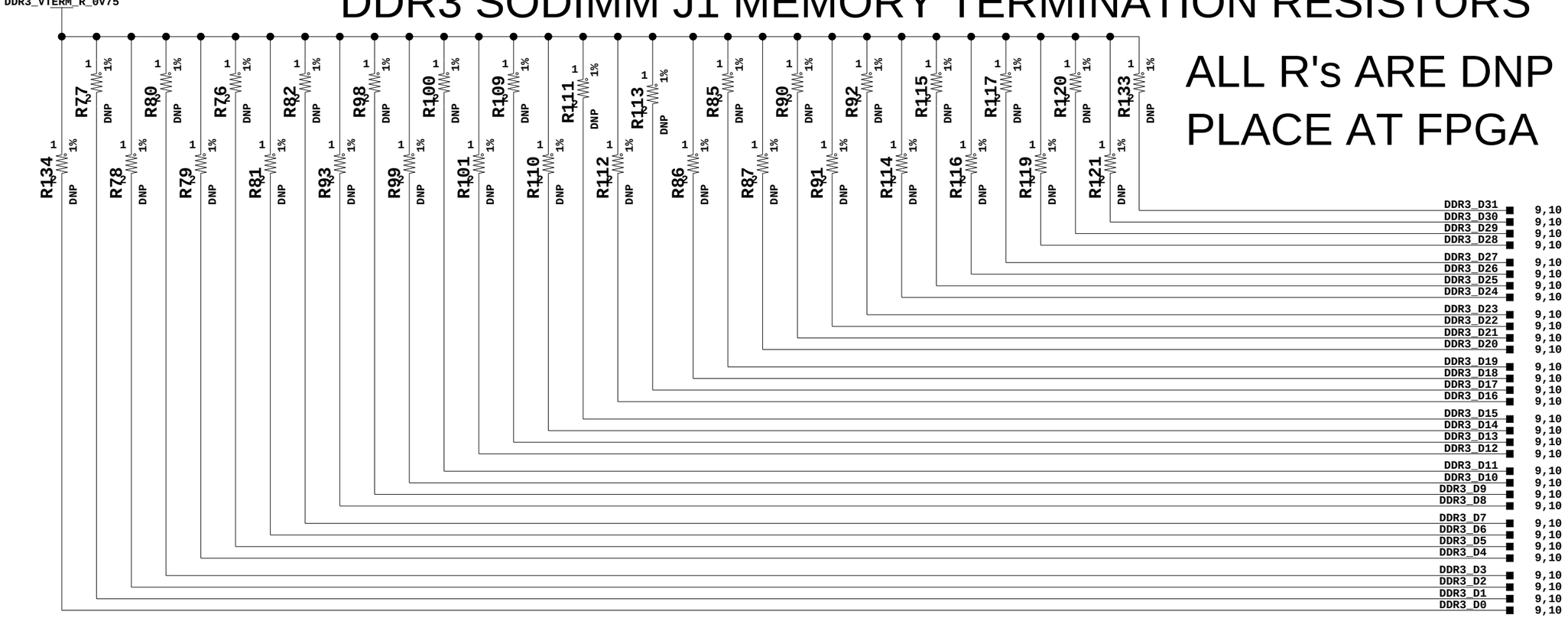
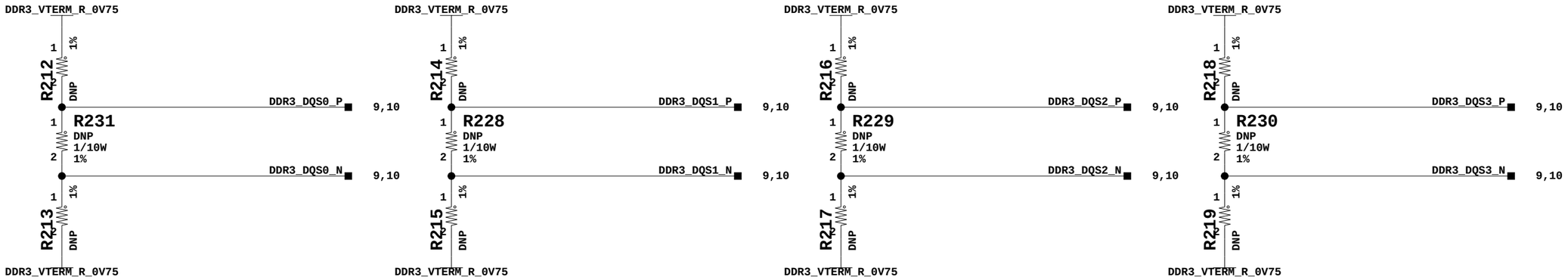
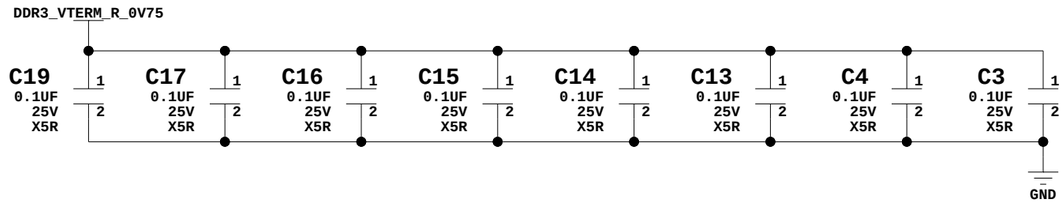
DDR3 SODIMM J1 MEMORY TERMINATION RESISTORS

ALL R's ARE DNP
PLACE AT FPGA







XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM TERM. RESISTORS		
Date:	9-20-2012_14:39	Ver:	1.0
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DDR3 SODIMM J1 MEMORY TERMINATION RESISTORS

DDR3_VTERM_R_0V75

R136 1 DNP 1% 2
R139 1 DNP 1% 2
R142 1 DNP 1% 2
R143 1 DNP 1% 2
R144 1 DNP 1% 2
R135 1 DNP 1% 2
R145 1 DNP 1% 2
R146 1 DNP 1% 2
R171 1 DNP 1% 2
R175 1 DNP 1% 2
R176 1 DNP 1% 2
R172 1 DNP 1% 2
R177 1 DNP 1% 2
R173 1 DNP 1% 2
R178 1 DNP 1% 2
R174 1 DNP 1% 2
R157 1 DNP 1% 2
R159 1 DNP 1% 2
R158 1 DNP 1% 2
R155 1 DNP 1% 2
R160 1 DNP 1% 2
R161 1 DNP 1% 2
R162 1 DNP 1% 2
R163 1 DNP 1% 2
R182 1 DNP 1% 2
R164 1 DNP 1% 2
R181 1 DNP 1% 2
R168 1 DNP 1% 2
R180 1 DNP 1% 2
R169 1 DNP 1% 2
R179 1 DNP 1% 2
R170 1 DNP 1% 2

ALL R's ARE DNP
PLACE AT FPGA

DDR3_D63 8,10
DDR3_D62 8,10
DDR3_D61 8,10
DDR3_D60 8,10
DDR3_D59 8,10
DDR3_D58 8,10
DDR3_D57 8,10
DDR3_D56 8,10
DDR3_D55 8,10
DDR3_D54 8,10
DDR3_D53 8,10
DDR3_D52 8,10
DDR3_D51 8,10
DDR3_D50 8,10
DDR3_D49 8,10
DDR3_D48 8,10
DDR3_D47 8,10
DDR3_D46 8,10
DDR3_D45 8,10
DDR3_D44 8,10
DDR3_D43 8,10
DDR3_D42 8,10
DDR3_D41 8,10
DDR3_D40 8,10
DDR3_D39 8,10
DDR3_D38 8,10
DDR3_D37 8,10
DDR3_D36 8,10
DDR3_D35 8,10
DDR3_D34 8,10
DDR3_D33 8,10
DDR3_D32 8,10

DDR3_VTERM_R_0V75
R220 1 DNP 1% 2
R237 1 DNP 1/10W 1% 2
R221 1 DNP 1% 2
DDR3_VTERM_R_0V75
DDR3_DQS4_P 8,10
DDR3_DQS4_N 8,10

DDR3_VTERM_R_0V75
R222 1 DNP 1% 2
R238 1 DNP 1/10W 1% 2
R223 1 DNP 1% 2
DDR3_VTERM_R_0V75
DDR3_DQS5_P 8,10
DDR3_DQS5_N 8,10

DDR3_VTERM_R_0V75
R224 1 DNP 1% 2
R239 1 DNP 1/10W 1% 2
R225 1 DNP 1% 2
DDR3_VTERM_R_0V75
DDR3_DQS6_P 8,10
DDR3_DQS6_N 8,10

DDR3_VTERM_R_0V75
R226 1 DNP 1% 2
R240 1 DNP 1/10W 1% 2
R227 1 DNP 1% 2
DDR3_VTERM_R_0V75
DDR3_DQS7_P 8,10
DDR3_DQS7_N 8,10

DDR3_VTERM_R_0V75
C40 0.1UF 25V X5R 1 2
C39 0.1UF 25V X5R 1 2
C38 0.1UF 25V X5R 1 2
C37 0.1UF 25V X5R 1 2
C27 0.1UF 25V X5R 1 2
C26 0.1UF 25V X5R 1 2
C21 0.1UF 25V X5R 1 2
C20 0.1UF 25V X5R 1 2
GND

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM TERM. RESISTORS		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
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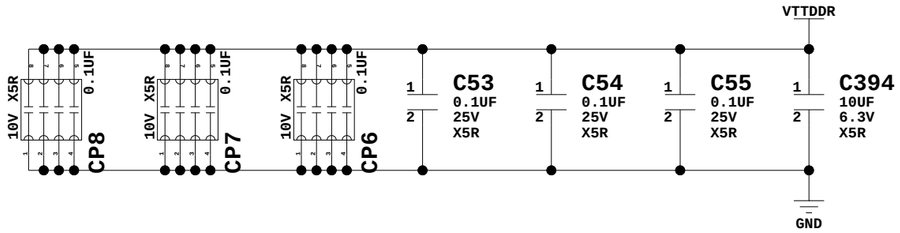
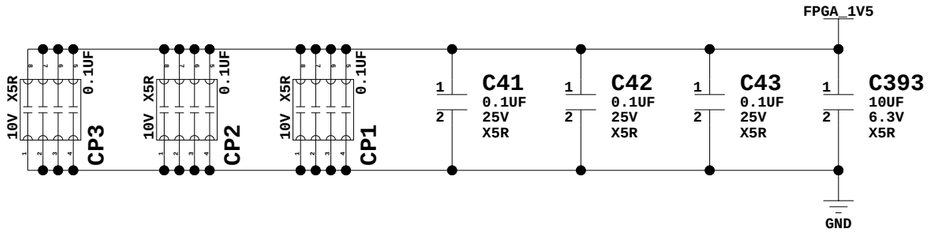
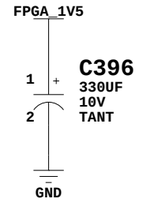
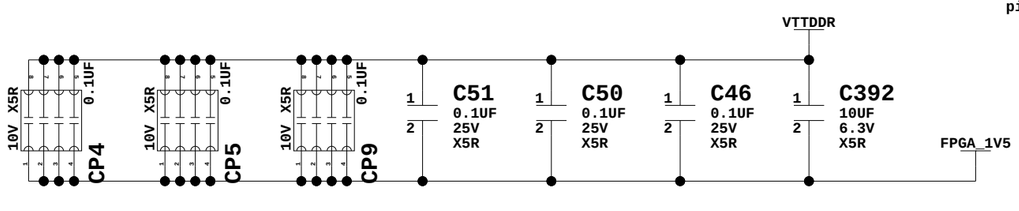
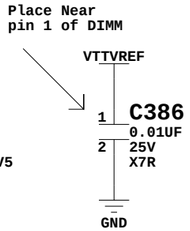
DDR3 SODIMM J1 MEMORY DECOUPLING CAPACITORS

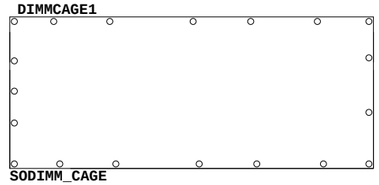












XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 SODIMM DECOUPLING	
Date:	9-20-2012_14:39	Ver: 1.0
Sheet Size: B		Rev: 01
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SOC_IRON_FG676

BANK 14
XC7A200TFBG676

IO_0_14_M19	M19	SI5324_INT_ALM_B 16
IO_L1P_T0_D00_MOSI_14_R14	R14	FLASH_D0 4
IO_L1N_T0_D01_DIN_14_R15	R15	FLASH_D1 4
IO_L2P_T0_D02_14_P14	P14	FLASH_D2 4
IO_L2N_T0_D03_14_N14	N14	FLASH_D3 4
IO_L3P_T0_DQS_PUDC_B_14_P15	P15	CTRL2_PWRGOOD 24,39,45
IO_L3N_T0_DQS_EMCCLK_14_P16	P16	FPGA_EMCCLK 3
IO_L4P_T0_D04_14_N16	N16	FMC1_HPC_PRSNT_M2C_B 24,26
IO_L4N_T0_D05_14_N17	N17	FMC1_HPC_PG_M2C 25
IO_L5P_T0_D06_14_R16	R16	FMC_VADJ_ON_B 45
IO_L5N_T0_D07_14_R17	R17	IIC_MUX_RESET_B 6
IO_L6P_T0_FCS_B_14_P18	P18	QSPI_IC_CS_B 4
IO_L6N_T0_D08_VREF_14_N18	N18	IIC_SCL_MAIN 6
IO_L7P_T1_D09_14_K25	K25	IIC_SDA_MAIN 6
IO_L7N_T1_D10_14_K26	K26	PCIE_WAKE_B 28
IO_L8P_T1_D11_14_M20	M20	PCIE_PERST 28
IO_L8N_T1_D12_14_L20	L20	LCD_E_LS 14
IO_L9P_T1_DQS_14_L24	L24	LCD_RW_LS 14
IO_L9N_T1_DQS_D13_14_L25	L25	LCD_DB4_LS 14
IO_L10P_T1_D14_14_M24	M24	LCD_DB5_LS 14
IO_L10N_T1_D15_14_M25	M25	LCD_DB6_LS 14
IO_L11P_T1_SRCC_14_L22	L22	LCD_DB7_LS 14
IO_L11N_T1_SRCC_14_L23	L23	LCD_RS_LS 14
IO_L12P_T1_MRCC_14_M21	M21	USER_CLOCK_P 3
IO_L12N_T1_MRCC_14_M22	M22	USER_CLOCK_N 3
IO_L13P_T2_MRCC_14_N21	N21	ROTARY_PUSH 21
IO_L13N_T2_MRCC_14_N22	N22	ROTARY_INCA 21
IO_L14P_T2_SRCC_14_P20	P20	ROTARY_INCB 21
IO_L14N_T2_SRCC_14_P21	P21	SDIO_CD_DAT3 14
IO_L15P_T2_DQS_RDWR_B_14_N23	N23	SDIO_CMD 14
IO_L15N_T2_DQSDOUT_CSOB_14_N24	N24	SDIO_CLK 14
IO_L16P_T2_CSI_B_14_P19	P19	SDIO_DAT0 14
IO_L16N_T2_A15_D31_14_N19	N19	SDIO_DAT1 14
IO_L17P_T2_A14_D30_14_P23	P23	SDIO_DAT2 14
IO_L17N_T2_A13_D29_14_P24	P24	SDIO_SDDET 14
IO_L18P_T2_A12_D28_14_R20	R20	SDIO_SDWP 14
IO_L18N_T2_A11_D27_14_R21	R21	PMBUS_CLK_LS 14
IO_L19P_T3_A10_D26_14_R25	R25	PMBUS_DATA_LS 14
IO_L19N_T3_A09_D25_VREF_14_P25	P25	PMBUS_CTRL_LS 14
IO_L20P_T3_A08_D24_14_N26	N26	PMBUS_ALERT_LS 14
IO_L20N_T3_A07_D23_14_M26	M26	GPIO_LED_0 21
IO_L21P_T3_DQS_14_T24	T24	GPIO_LED_1 21
IO_L21N_T3_DQS_A06_D22_14_T25	T25	GPIO_LED_2 21
IO_L22P_T3_A05_D21_14_R26	R26	GPIO_LED_3 21
IO_L22N_T3_A04_D20_14_P26	P26	PMOD_0 21
IO_L23P_T3_A03_D19_14_T22	T22	PMOD_1 21
IO_L23N_T3_A02_D18_14_R22	R22	PMOD_2 21
IO_L24P_T3_A01_D17_14_T23	T23	PMOD_3 21
IO_L24N_T3_A00_D16_14_R23	R23	SFP_LOS 20
IO_25_14_R18	R18	SFP_TX_DISABLE 20

FPGA_3V3

R19	VCCO_14_R19
P22	VCCO_14_P22
N25	VCCO_14_N25
N15	VCCO_14_N15
L21	VCCO_14_L21
K24	VCCO_14_K24

U1 SOC_IRON_FG676

PWRCTL1_VCC4B_PG
CTRL2_PWRGOOD from TI controller U9 indicates both VCC3V3 and VCCO_VADJ FMC power rails are OK

VCC5V0

J23 HDR_2X7

14 LCD_DB7	1	2	LCD_DB6 14
14 LCD_DB5	3	4	LCD_DB4 14
NC	5	6	NC
NC	7	8	NC
14 LCD_E	9	10	LCD_RW 14
14 LCD_RS	11	12	LCD_VEE
	13	14	

GND

6.81K 1/10W 1% R118 VCC5V0

LCD Contrast Pot
R232 2K 1/2W 20% POT_3352W

GND

FPGA_3V3

C473 0.1UF 25V X5R

GND

VCC5V0

C472 0.1UF 25V X5R

GND

TXS0108E U45 TSSOP_20

	2	VCCA	VCCB	19	
14 LCD_E_LS	1	A1	B1	20	LCD_E 14
14 LCD_RW_LS	3	A2	B2	18	LCD_RW 14
14 LCD_DB4_LS	4	A3	B3	17	LCD_DB4 14
14 LCD_DB5_LS	5	A4	B4	16	LCD_DB5 14
14 LCD_DB6_LS	6	A5	B5	15	LCD_DB6 14
14 LCD_DB7_LS	7	A6	B6	14	LCD_DB7 14
14 LCD_RS_LS	8	A7	B7	13	LCD_RS 14
NC	9	A8	B8	12	NC
	10	OE	GND	11	

GND

VCC3V3

PMBUS Isolation

38,39,45	PMBUS_CLK	Q14 NDS331N	PMBUS_CLK_LS 14
38,39,45	PMBUS_DATA	Q15 NDS331N	PMBUS_DATA_LS 14
38,39	PMBUS_CTRL	Q19 NDS331N	PMBUS_CTRL_LS 14
38,39,45	PMBUS_ALERT	Q20 NDS331N	PMBUS_ALERT_LS 14

R313 2.00K R315 2.00K R314 2.00K R316 2.00K

FPGA_3V3

C155 100UF 6.3 X5R

GND

VCC3V3

C52 0.1UF 25V X5R

GND

R325 51.1K R319 51.1K R322 51.1K R321 51.1K R323 51.1K R318 51.1K R324 51.1K R317 51.1K

67840-8001 U29

14 SDIO_CD_DAT3	1	CD_DAT3	IOGND2	18	
14 SDIO_CMD	2	CMD	IOGND1	17	
	3	VSS1	GNDTAB4	16	
	4	VDD	GNDTAB3	15	
14 SDIO_CLK	5	CLK	GNDTAB2	14	
	6	VSS2	GNDTAB1	13	
14 SDIO_DAT0	7	DAT0			
14 SDIO_DAT1	8	DAT1			
14 SDIO_DAT2	9	DAT2			
14 SDIO_SDDET	10	DETECT			
14 SDIO_SDWP	11	PROTECT			
	12	DETECT_PROTECT			

GND GND

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD GPIO BANK14, SD SOCKET, LCD IF		
Date:	9-20-2012_14:39	Ver:	1.0
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CONFIGURATION MAPPING

PIN	SETTING	CONFIGURATION	
CONFIG0	VCCO_MIO1	PHYAD[1]=1	PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0	PHYAD[2]=1
CONFIG2	GND	ENA_XC=0	PHYAD[4]=0
	EPHY_LED0	ENA_XC=0	PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1	PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0	RGMII_RX=0
	EPHY_LED0	RGMII_TX=0	RGMII_RX=1
	EPHY_LED1	RGMII_TX=1	RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1	RGMII_RX=1

GEM / MDIO - POWER & DECOUPLING

VCC1V8 — L12 FERRITE-220 — VCC1V8_FILT

MAGNETICS / RJ45

VCC1V8_FILT — C400 4.7UF 10V — C90 0.1UF 25V — GND

VCC1V8_FILT — AVDDX, AVDDR, AVDDC

C398 4.7UF 10V; C86 C87 C85 C84 C88 C83 0.1UF 25V — GND

VCC1V8_FILT — AVDD

C397 4.7UF 10V; C81 C82 C80 C79 C89 C64 0.1UF 25V — GND

VCC1V8 — VDDO, VDDOR

C403 4.7UF 10V; C98 C99 C97 C96 C100 0.1UF 25V — GND

1. TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESITORS ON HSDAC_P AND HSDAC_N.
2. SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

J35 HDR_1X3 — VCC1V8 — R274 1.00K 1/16W

J37 HDR_1X3 — PHY_LED1 15 — PHY_LED0 15

J36 HDR_1X3 — PHY_LED0 15

J5 HDR_1X2

R271 1.00K 1/16W — GND

VCC1V8 — R2 4.7K 1/10W

88E1116R

17 PHY_MDIO	45	MDIO	MGMT
17 PHY_MDC	48	MDC	
15,17 PHY_TX_CLK	60	TX_CLK	RGMII
15,17 PHY_TX_CTRL	63	TX_CTRL	
15,17 PHY_TXD3	62	TXD3	
15,17 PHY_TXD2	61	TXD2	
15,17 PHY_TXD1	59	TXD1	
15,17 PHY_TXD0	58	TXD0	
17 PHY_RX_CLK	53	RX_CLK	
17 PHY_RX_CTRL	49	RX_CTRL	
17 PHY_RXD3	55	RXD3	
17 PHY_RXD2	54	RXD2	
17 PHY_RXD1	51	RXD1	
17 PHY_RXD0	50	RXD0	
PHY_CONFIG3	3	CONFIG3	
PHY_CONFIG2	2	CONFIG2	
PHY_LED0	1	CONFIG1	
15	64	CONFIG0	
15 PHY_XTAL_IN	38	XTAL_IN	
15 PHY_XTAL_OUT	39	XTAL_OUT	
	4	COMA_B	
PHY_VREF	57	VREF	
17 PHY_RESET_B	10	RESET_B	

MDI	MDI0_P	31	PHY_MDI0_P
	MDI0_N	30	PHY_MDI0_N
	MDI1_P	26	PHY_MDI1_P
	MDI1_N	25	PHY_MDI1_N
	MDI2_P	24	PHY_MDI2_P
	MDI2_N	23	PHY_MDI2_N
	MDI3_P	20	PHY_MDI3_P
	MDI3_N	19	PHY_MDI3_N
RSET		33	PHY_RSET
CTRL18		17	NC
DIS_REG12		12	
LED0		6	PHY_LED0 15
LED1		8	PHY_LED1 15
LED2		9	PHY_LED2 15
TEST	HSDAC_P	36	PHY_HSDAC_P
	HSDAC_N	35	PHY_HSDAC_N
	TSTPT	32	NC
JTAG	TRST_B	11	PHY_TRST_B
	TCK	42	NC
	TMS	41	NC
	TDI	43	NC
	TDO	44	NC

QFN_64

U12

PHY POWER SYMBOL & CAPS MOVED TO PG. 16

VCC1V8_FILT — C56 0.1UF 25V — C395 1000PF 50V X7R — GND

RJ45 — P4 — 10/100/1000 RJ45 AND MAGNETICS

1	TD0_P
2	TD0_N
3	TD1_P
6	TD1_N
4	TD2_P
5	TD2_N
7	TD3_P
8	TD3_N
9	VCC
10	GND
SH2	SH2
SH1	SH1

R291 4.99K 1/10W — GND

J24 DNP — GND

L11 FERRITE-220 — GND

R1 4.7K 1/10W — R3 R10 DNP 2 PLACES — GND

VCC1V8 — R272 1.00K 1/16W — R273 1.00K 1/16W — GND

VCC1V8 — R448 R449 R447 R445 R443 R438 100 1/10W 1%

R450 R451 R446 R444 R442 R441 100 1/10W 1%

15,17 PHY_TX_CLK
15,17 PHY_TX_CTRL
15,17 PHY_TXD3
15,17 PHY_TXD2
15,17 PHY_TXD1
15,17 PHY_TXD0

VCC3V3 — R281 R280 R279 261 1/10W

LED-GRN-SMT — DS13 DS12 DS11

Q4 Q3 Q1 NDS331N

15 PHY_LED0 — 15 PHY_LED1 — 15 PHY_LED2 — GND

25.00MHZ
50PPM

X1 — NC 3 — NC 2 — 4 — 1

PHY_XTAL_OUT 15 — PHY_XTAL_IN 15

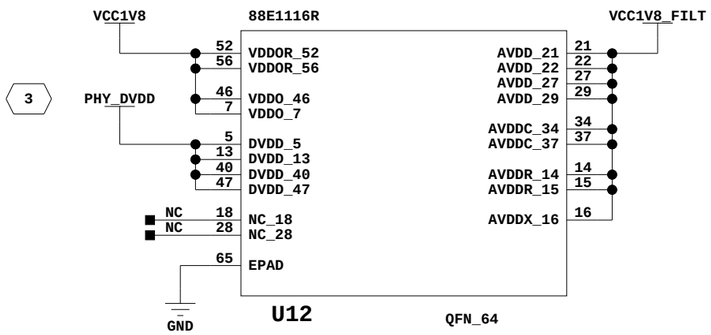
R275 DNP — C405 C406 18PF 50V NPO 2 PLACES — GND

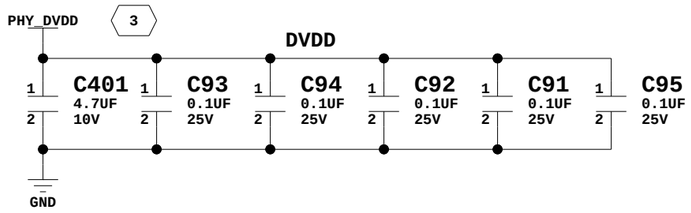
GEM / MDIO

XILINX

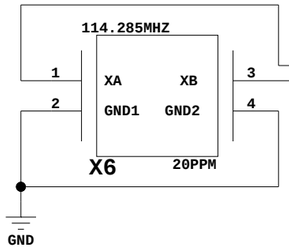
ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

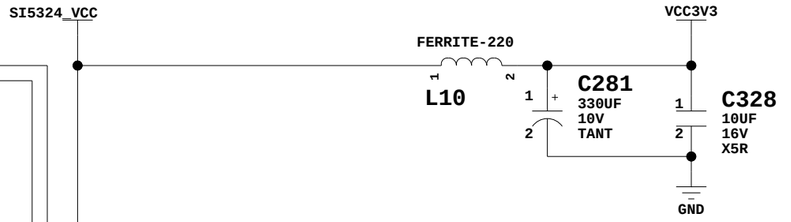
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD 10/100/1000 PHY		
Date:	10-9-2012_15:53	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	15 of 51	Drawn By	DN

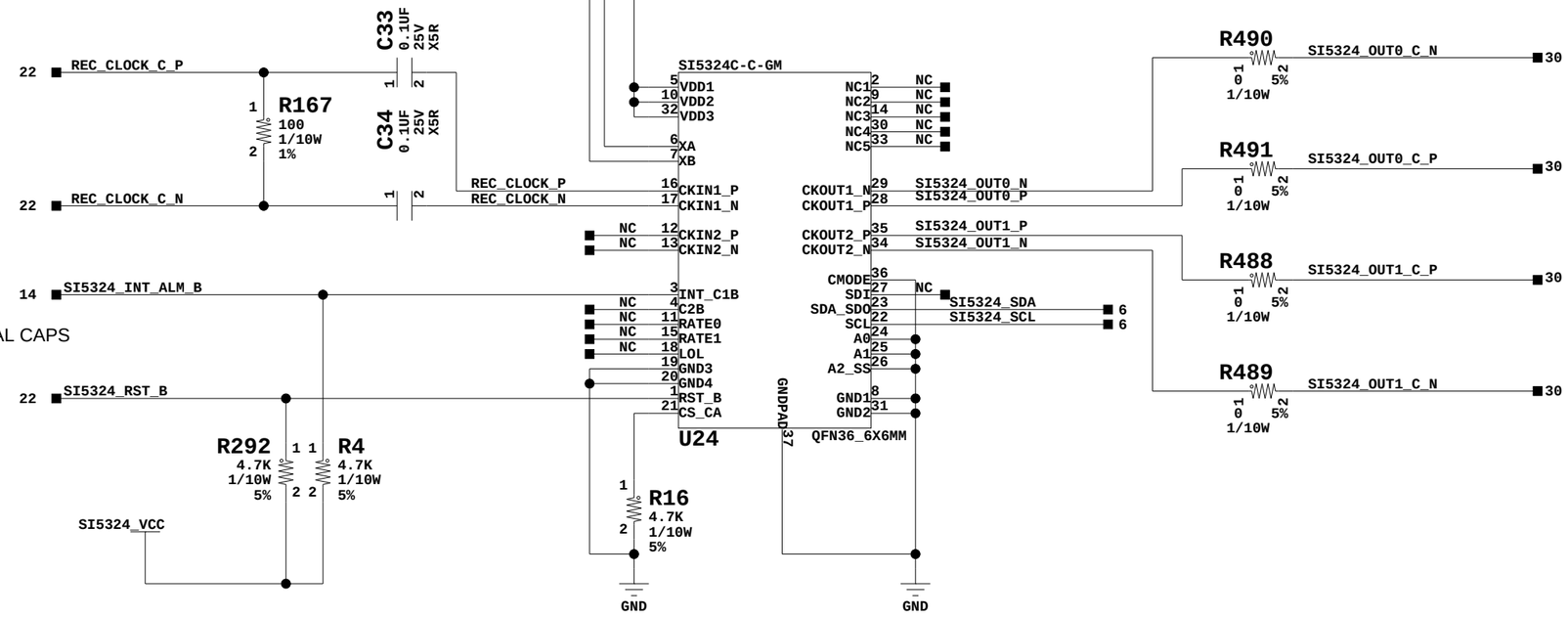




3 DVDD 1.2V IS SUPPLIED INTERNALLY. DVDD PINS 5,13,40,47 ARE FOR EXTERNAL CAPS







5324 Clock Recovery

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD SI5324 CLOCK RECOVERY		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
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SOC_IRON_FG676

BANK 13
XC7A200TFBG676

IO_0_13_U24	U24	HDMI_R_D21	19
IO_L1P_T0_13_U25	U25	HDMI_R_D16	19
IO_L1N_T0_13_U26	U26	HDMI_R_D11	19
IO_L2P_T0_13_V26	V26	HDMI_R_D7	19
IO_L2N_T0_13_W26	W26	HDMI_R_D8	19
IO_L3P_T0_DQS_13_AB26	AB26	HDMI_R_DE	19
IO_L3N_T0_DQS_13_AC26	AC26	HDMI_R_VSYNC	19
IO_L4P_T0_13_W25	W25	HDMI_R_D9	19
IO_L4N_T0_13_Y26	Y26	HDMI_R_D6	19
IO_L5P_T0_13_Y25	Y25	HDMI_R_D5	19
IO_L5N_T0_13_AA25	AA25	HDMI_R_D29	19
IO_L6P_T0_13_V24	V24	HDMI_R_D17	19
IO_L6N_T0_VREF_13_W24	W24	HDMI_R_D10	19
IO_L7P_T1_13_AA24	AA24	HDMI_R_D4	19
IO_L7N_T1_13_AB25	AB25	HDMI_R_D30	19
IO_L8P_T1_13_AA22	AA22	HDMI_R_HSYNC	19
IO_L8N_T1_13_AA23	AA23	HDMI_R_D28	19
IO_L9P_T1_DQS_13_AB24	AB24	HDMI_R_D32	19
IO_L9N_T1_DQS_13_AC24	AC24	HDMI_R_D31	19
IO_L10P_T1_13_V23	V23	HDMI_R_D23	19
IO_L10N_T1_13_W23	W23	HDMI_R_D19	19
IO_L11P_T1_SRCC_13_Y22	Y22	HDMI_R_D33	19
IO_L11N_T1_SRCC_13_Y23	Y23	HDMI_R_D34	19
IO_L12P_T1_MRCC_13_U22	U22	PHY_TX_CLK	15
IO_L12N_T1_MRCC_13_V22	V22	HDMI_R_D35	19
IO_L13P_T2_MRCC_13_U21	U21	PHY_RX_CLK	15
IO_L13N_T2_MRCC_13_V21	V21	HDMI_R_CLK	19
IO_L14P_T2_SRCC_13_W21	W21	HDMI_INT	18
IO_L14N_T2_SRCC_13_Y21	Y21	HDMI_R_SPDIF	19
IO_L15P_T2_DQS_13_T20	T20	HDMI_SPDIF_OUT_LS	17
IO_L15N_T2_DQS_13_U20	U20	HDMI_R_D18	19
IO_L16P_T2_13_W20	W20	HDMI_R_D20	19
IO_L16N_T2_13_Y20	Y20	HDMI_R_D22	19
IO_L17P_T2_13_T19	T19	USB_UART_TX	5
IO_L17N_T2_13_U19	U19	USB_UART_RX	5
IO_L18P_T2_13_V19	V19	USB_UART_RTS	5
IO_L18N_T2_13_W19	W19	USB_UART_CTS	5
IO_L19P_T3_13_V18	V18	PHY_RESET_B	15
IO_L19N_T3_VREF_13_W18	W18	PHY_MDC	15
IO_L20P_T3_13_T14	T14	PHY_MDIO	15
IO_L20N_T3_13_T15	T15	PHY_TX_CTRL	15
IO_L21P_T3_DQS_13_T17	T17	PHY_TXD3	15
IO_L21N_T3_DQS_13_T18	T18	PHY_TXD2	15
IO_L22P_T3_13_U15	U15	PHY_TXD1	15
IO_L22N_T3_13_U16	U16	PHY_TXD0	15
IO_L23P_T3_13_U14	U14	PHY_RX_CTRL	15
IO_L23N_T3_13_V14	V14	PHY_RXD3	15
IO_L24P_T3_13_V16	V16	PHY_RXD2	15
IO_L24N_T3_13_V17	V17	PHY_RXD1	15
IO_25_13_U17	U17	PHY_RXD0	15

FPGA_1V8

Y24	VCCO_13_Y24
V20	VCCO_13_V20
U23	VCCO_13_U23
T26	VCCO_13_T26
T16	VCCO_13_T16
AC25	VCCO_13_AC25

U1

SOC_IRON_FG676

FPGA_1V8

C60
0.1UF
25V
X5R

GND

VCC3V3

C59
0.1UF
25V
X5R

GND

SN74AVC1T45

		1	VCCA	VCCB	6	
17	HDMI_SPDIF_OUT_LS	3	A	B	4	HDMI_SPDIF_OUT	18
		2	GND	DIR	5	

SC70_6

U38

GND

GND

FPGA_1V8

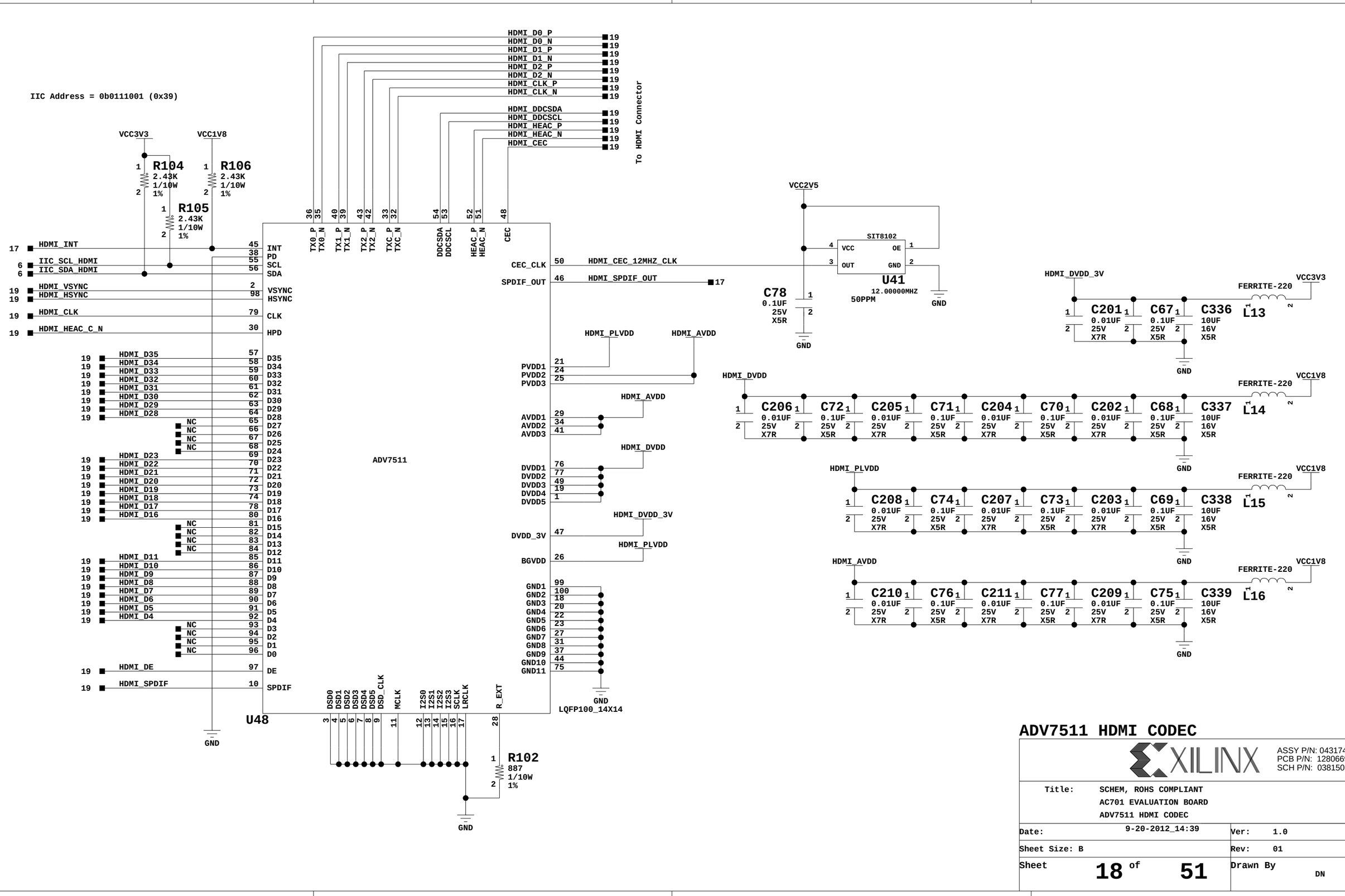
C156
100UF
6.3
X5R

GND

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANK13 HDIM/EPHY IF		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	17 of 51	Drawn By	DN



ADV7511 HDMI CODEC

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD ADV7511 HDMI CODEC		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
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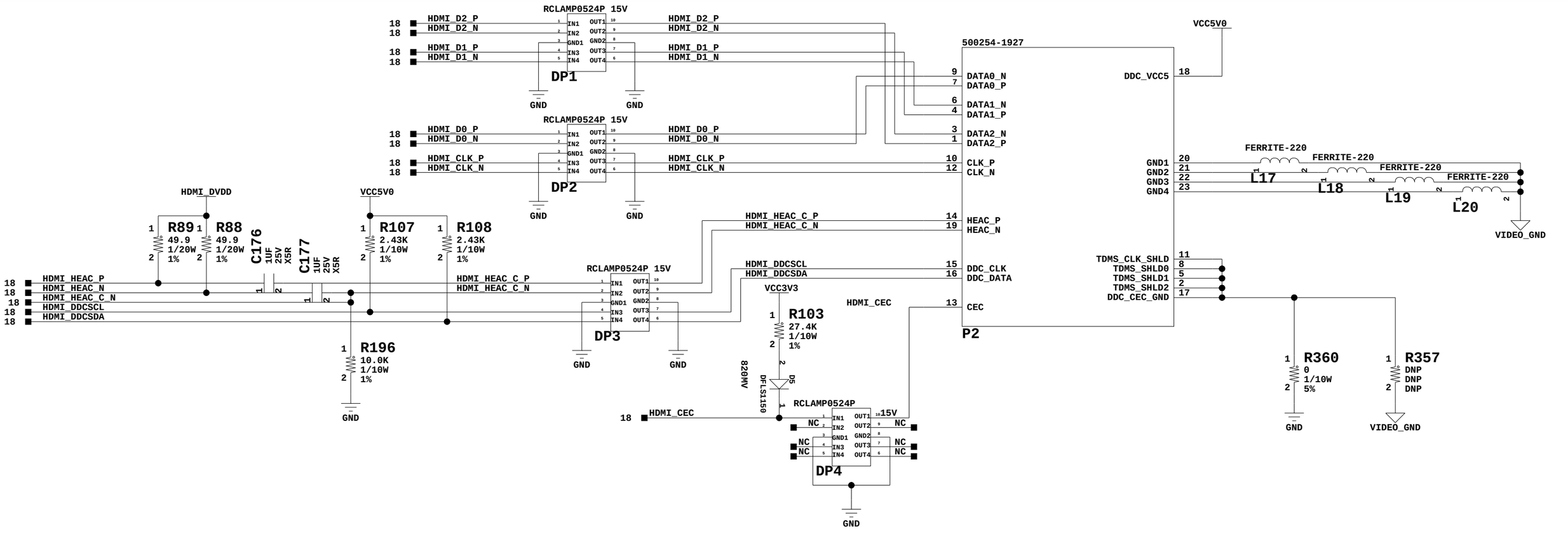
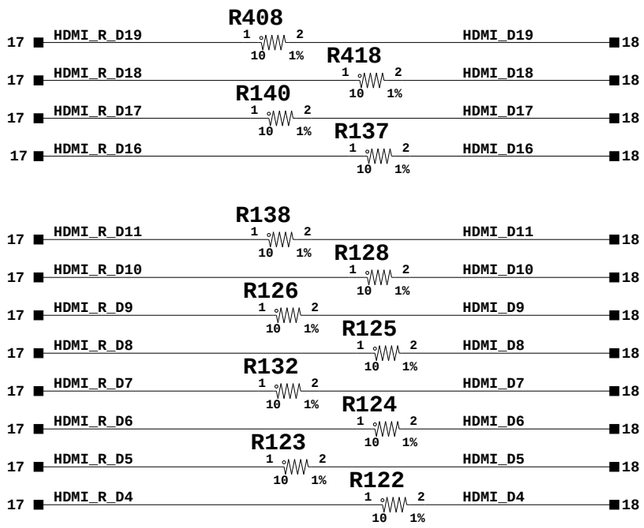
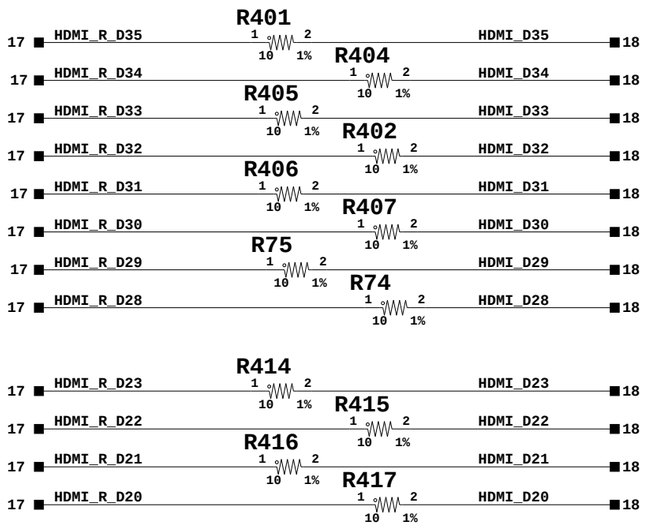
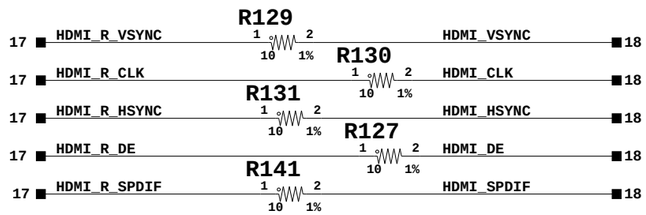


Place series Rs at FPGA







HDMI CONNECTOR

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD HDMI CONN. P2, HDMI SERIES R's		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
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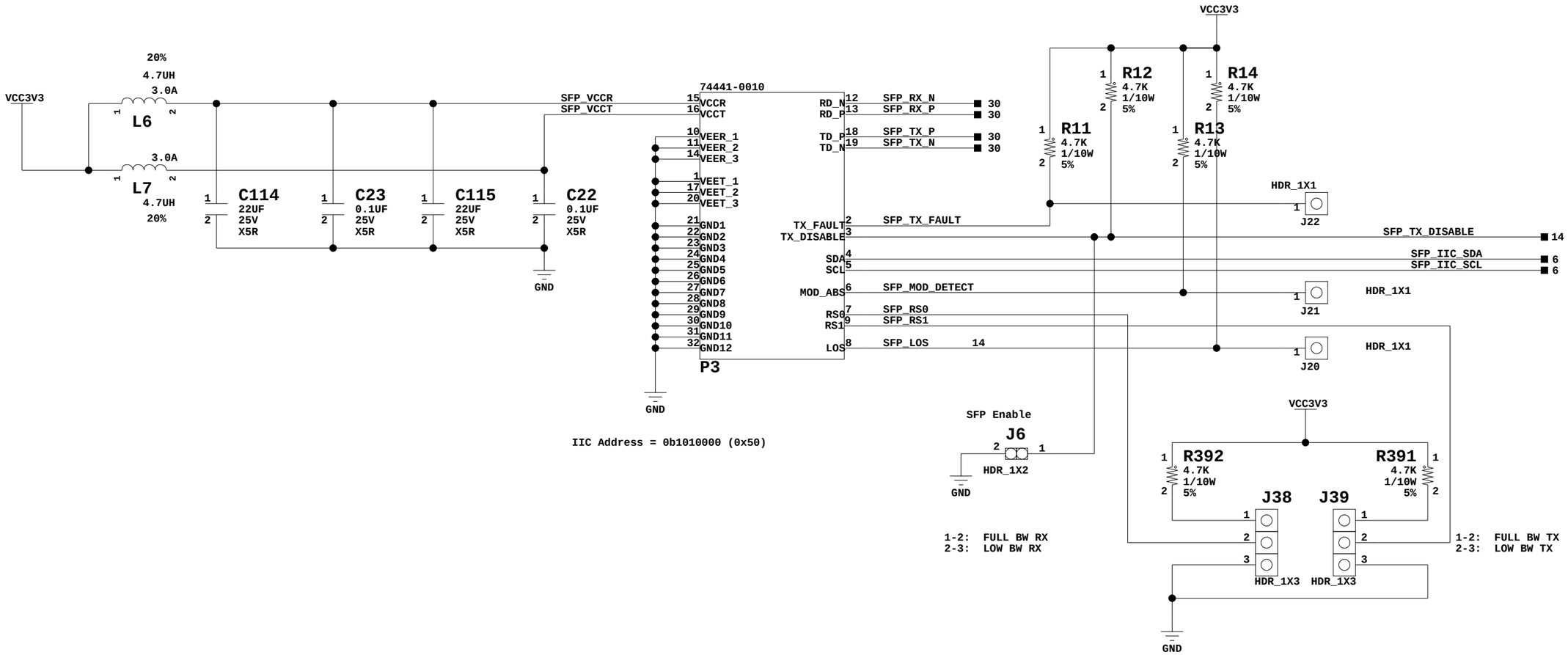
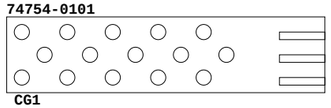


74754-0101



CG1

SFP+ Connector and Cage

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD SFP+ CONN. P3		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
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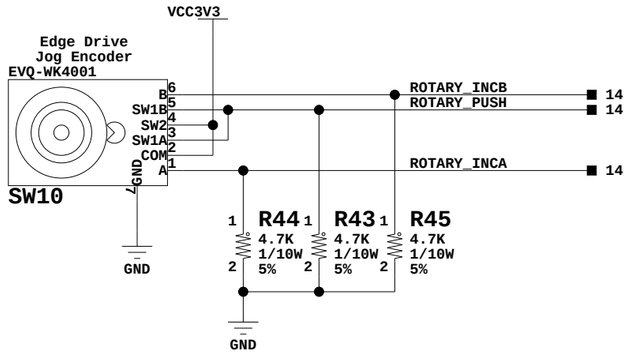
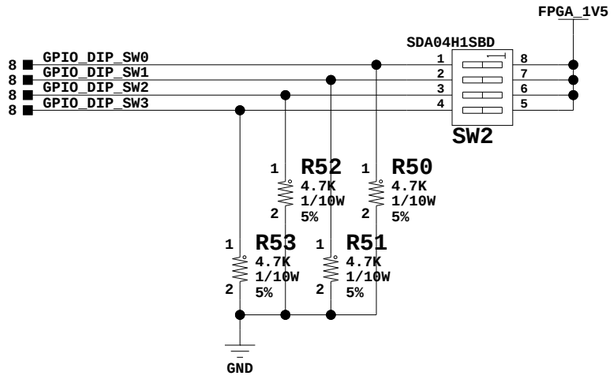
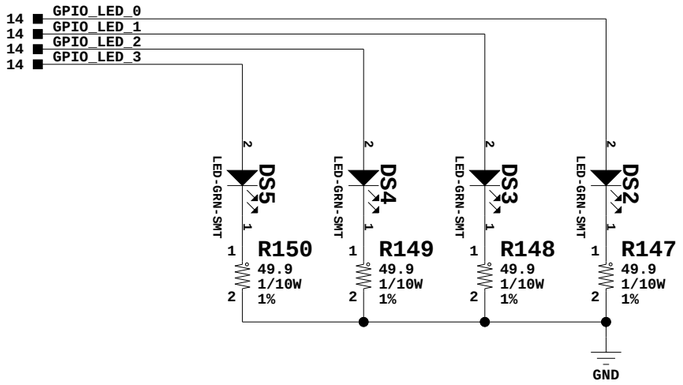
Rotary Switch

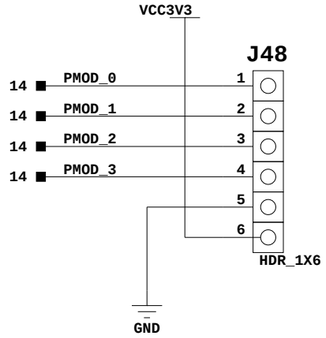


4-Pole DIP Switch

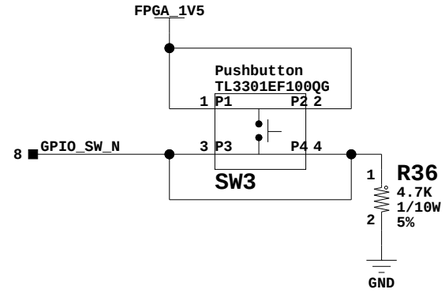


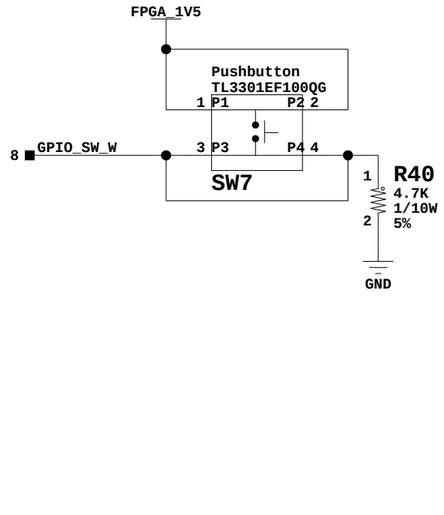
LEDs near top edge

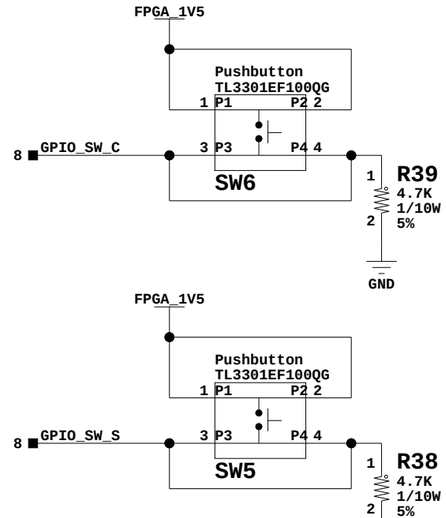


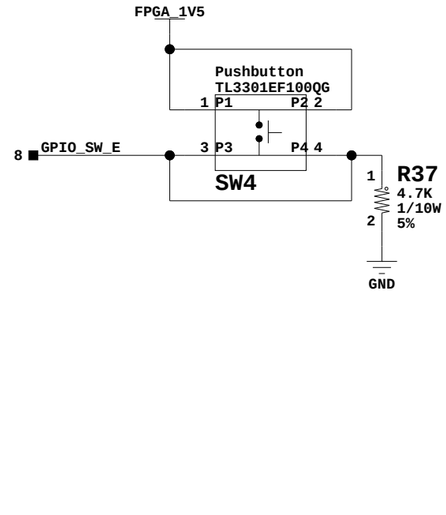


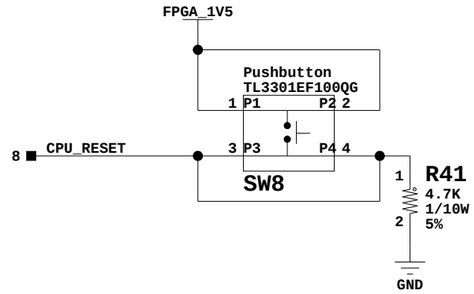
Directional Push-Buttons











XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD GPIO SWITCHES and LEDs		
Date:	9-20-2012_14:39	Ver:	1.0
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SOC_IRON_FG676

BANK 16
XC7A200TFBG676

IO_0_16_H17	H17	XADC_GPIO_0 ■ 29
IO_L1P_T0_16_H14	H14	FMC1_HPC_LA02_P ■ 26
IO_L1N_T0_16_H15	H15	FMC1_HPC_LA02_N ■ 26
IO_L2P_T0_16_G17	G17	FMC1_HPC_LA03_P ■ 25
IO_L2N_T0_16_F17	F17	FMC1_HPC_LA03_N ■ 25
IO_L3P_T0_DQS_16_F18	F18	FMC1_HPC_LA04_P ■ 26
IO_L3N_T0_DQS_16_F19	F19	FMC1_HPC_LA04_N ■ 26
IO_L4P_T0_16_G15	G15	FMC1_HPC_LA05_P ■ 24
IO_L4N_T0_16_F15	F15	FMC1_HPC_LA05_N ■ 24
IO_L5P_T0_16_G19	G19	FMC1_HPC_LA06_P ■ 24
IO_L5N_T0_16_F20	F20	FMC1_HPC_LA06_N ■ 24
IO_L6P_T0_16_H16	H16	FMC1_HPC_LA07_P ■ 26
IO_L6N_T0_VREF_16_G16	G16	FMC1_HPC_LA07_N ■ 26
IO_L7P_T1_16_C17	C17	FMC1_HPC_LA08_P ■ 25
IO_L7N_T1_16_B17	B17	FMC1_HPC_LA08_N ■ 25
IO_L8P_T1_16_E16	E16	FMC1_HPC_LA09_P ■ 24
IO_L8N_T1_16_D16	D16	FMC1_HPC_LA09_N ■ 24
IO_L9P_T1_DQS_16_A17	A17	FMC1_HPC_LA10_P ■ 24
IO_L9N_T1_DQS_16_A18	A18	FMC1_HPC_LA10_N ■ 24
IO_L10P_T1_16_B19	B19	FMC1_HPC_LA11_P ■ 26
IO_L10N_T1_16_A19	A19	FMC1_HPC_LA11_N ■ 26
IO_L11P_T1_SRCC_16_E17	E17	FMC1_HPC_LA01_CC_P ■ 24
IO_L11N_T1_SRCC_16_E18	E18	FMC1_HPC_LA01_CC_N ■ 24
IO_L12P_T1_MRCC_16_D18	D18	FMC1_HPC_LA00_CC_P ■ 25
IO_L12N_T1_MRCC_16_C18	C18	FMC1_HPC_LA00_CC_N ■ 25
IO_L13P_T2_MRCC_16_D19	D19	FMC1_HPC_CLK0_M2C_P ■ 26
IO_L13N_T2_MRCC_16_C19	C19	FMC1_HPC_CLK0_M2C_N ■ 26
IO_L14P_T2_SRCC_16_E20	E20	FMC1_HPC_LA12_P ■ 25
IO_L14N_T2_SRCC_16_D20	D20	FMC1_HPC_LA12_N ■ 25
IO_L15P_T2_DQS_16_B20	B20	FMC1_HPC_LA13_P ■ 24
IO_L15N_T2_DQS_16_A20	A20	FMC1_HPC_LA13_N ■ 24
IO_L16P_T2_16_C21	C21	FMC1_HPC_LA14_P ■ 24
IO_L16N_T2_16_B21	B21	FMC1_HPC_LA14_N ■ 24
IO_L17P_T2_16_B22	B22	FMC1_HPC_LA15_P ■ 26
IO_L17N_T2_16_A22	A22	FMC1_HPC_LA15_N ■ 26
IO_L18P_T2_16_E21	E21	FMC1_HPC_LA16_P ■ 25
IO_L18N_T2_16_D21	D21	FMC1_HPC_LA16_N ■ 25
IO_L19P_T3_16_C22	C22	NC
IO_L19N_T3_VREF_16_C23	C23	NC
IO_L20P_T3_16_B25	B25	XADC_MUX_ADDR0_LS
IO_L20N_T3_16_A25	A25	XADC_MUX_ADDR1_LS ■ 37
IO_L21P_T3_DQS_16_A23	A23	XADC_MUX_ADDR2_LS ■ 37
IO_L21N_T3_DQS_16_A24	A24	PCIE_MGT_CLK_SEL0 ■ 37
IO_L22P_T3_16_C26	C26	PCIE_MGT_CLK_SEL1 ■ 30
IO_L22N_T3_16_B26	B26	SFP_MGT_CLK_SEL0 ■ 30
IO_L23P_T3_16_C24	C24	SFP_MGT_CLK_SEL1 ■ 30
IO_L23N_T3_16_B24	B24	SI5324_RST_LS_B ■ 22
IO_L24P_T3_16_D23	D23	REC_CLOCK_C_P ■ 16
IO_L24N_T3_16_D24	D24	REC_CLOCK_C_N ■ 16
IO_25_16_E22	E22	XADC_GPIO_1 ■ 29

VCCO_VADJ

F16	VCCO_16_F16
E19	VCCO_16_E19
D22	VCCO_16_D22
C25	VCCO_16_C25
B18	VCCO_16_B18
A21	VCCO_16_A21

U1

SOC_IRON_FG676

SOC_IRON_FG676

BANK 15
XC7A200TFBG676

IO_0_15_K18	K18	XADC_GPIO_2 ■ 29
IO_L1P_T0_AD0P_15_K15	K15	XADC_VAUX0_R_P ■ 29
IO_L1N_T0_AD0N_15_J16	J16	XADC_VAUX0_R_N ■ 29
IO_L2P_T0_AD8P_15_J14	J14	XADC_VAUX8_R_P ■ 29
IO_L2N_T0_AD8N_15_J15	J15	XADC_VAUX8_R_N ■ 29
IO_L3P_T0_DQS_AD1P_15_K16	K16	XADC_AD1_R_P ■ 37
IO_L3N_T0_DQS_AD1N_15_K17	K17	XADC_AD1_R_N ■ 37
IO_L4P_T0_15_M14	M14	FMC1_HPC_LA19_P ■ 26
IO_L4N_T0_15_L14	L14	FMC1_HPC_LA19_N ■ 26
IO_L5P_T0_AD9P_15_M15	M15	XADC_AD9_R_P ■ 37
IO_L5N_T0_AD9N_15_L15	L15	XADC_AD9_R_N ■ 37
IO_L6P_T0_15_M16	M16	FMC1_HPC_LA20_P ■ 25
IO_L6N_T0_VREF_15_M17	M17	FMC1_HPC_LA20_N ■ 25
IO_L7P_T1_AD2P_15_J19	J19	FMC1_HPC_LA21_P ■ 26
IO_L7N_T1_AD2N_15_H19	H19	FMC1_HPC_LA21_N ■ 26
IO_L8P_T1_AD10P_15_L17	L17	FMC1_HPC_LA22_P ■ 25
IO_L8N_T1_AD10N_15_L18	L18	FMC1_HPC_LA22_N ■ 25
IO_L9P_T1_DQS_AD3P_15_K20	K20	FMC1_HPC_LA23_P ■ 24
IO_L9N_T1_DQS_AD3N_15_J20	J20	FMC1_HPC_LA23_N ■ 24
IO_L10P_T1_AD11P_15_J18	J18	FMC1_HPC_LA24_P ■ 26
IO_L10N_T1_AD11N_15_H18	H18	FMC1_HPC_LA24_N ■ 26
IO_L11P_T1_SRCC_15_G20	G20	FMC1_HPC_LA18_CC_P ■ 24
IO_L11N_T1_SRCC_15_G21	G21	FMC1_HPC_LA18_CC_N ■ 24
IO_L12P_T1_MRCC_15_K21	K21	FMC1_HPC_LA17_CC_P ■ 24
IO_L12N_T1_MRCC_15_J21	J21	FMC1_HPC_LA17_CC_N ■ 24
IO_L13P_T2_MRCC_15_H21	H21	FMC1_HPC_CLK1_M2C_P ■ 25
IO_L13N_T2_MRCC_15_H22	H22	FMC1_HPC_CLK1_M2C_N ■ 25
IO_L14P_T2_SRCC_15_J23	J23	USER_SMA_CLOCK_P ■ 3
IO_L14N_T2_SRCC_15_H23	H23	USER_SMA_CLOCK_N ■ 3
IO_L15P_T2_DQS_15_G22	G22	FMC1_HPC_LA25_P ■ 25
IO_L15N_T2_DQS_ADV_B_15_F22	F22	FMC1_HPC_LA25_N ■ 25
IO_L16P_T2_A28_15_J24	J24	FMC1_HPC_LA26_P ■ 24
IO_L16N_T2_A27_15_H24	H24	FMC1_HPC_LA26_N ■ 24
IO_L17P_T2_A26_15_F23	F23	FMC1_HPC_LA27_P ■ 24
IO_L17N_T2_A25_15_E23	E23	FMC1_HPC_LA27_N ■ 24
IO_L18P_T2_A24_15_K22	K22	FMC1_HPC_LA28_P ■ 26
IO_L18N_T2_A23_15_K23	K23	FMC1_HPC_LA28_N ■ 26
IO_L19P_T3_A22_15_G24	G24	FMC1_HPC_LA29_P ■ 25
IO_L19N_T3_A21_VREF_15_F24	F24	FMC1_HPC_LA29_N ■ 25
IO_L20P_T3_A20_15_E25	E25	FMC1_HPC_LA30_P ■ 26
IO_L20N_T3_A19_15_D25	D25	FMC1_HPC_LA30_N ■ 26
IO_L21P_T3_DQS_15_E26	E26	FMC1_HPC_LA31_P ■ 25
IO_L21N_T3_DQS_A18_15_D26	D26	FMC1_HPC_LA31_N ■ 25
IO_L22P_T3_A17_15_H26	H26	FMC1_HPC_LA32_P ■ 26
IO_L22N_T3_A16_15_G26	G26	FMC1_HPC_LA32_N ■ 26
IO_L23P_T3_FOE_B_15_G25	G25	FMC1_HPC_LA33_P ■ 25
IO_L23N_T3_FWE_B_15_F25	F25	FMC1_HPC_LA33_N ■ 25
IO_L24P_T3_RS1_15_J25	J25	SM_FAN_TACH ■ 38
IO_L24N_T3_RS0_15_J26	J26	SM_FAN_PWM ■ 38
IO_25_15_L19	L19	XADC_GPIO_3 ■ 29

VCCO_VADJ

M18	VCCO_15_M18
K14	VCCO_15_K14
J17	VCCO_15_J17
H20	VCCO_15_H20
G23	VCCO_15_G23
F26	VCCO_15_F26

U1

SOC_IRON_FG676

VCCO_VADJ

C159 100UF 6.3 X5R

GND

VCC3V3

C57 0.1UF 25V X5R

GND

VCCO_VADJ

C58 0.1UF 25V X5R

GND

VCCO_VADJ

C160 100UF 6.3 X5R

GND

SN74AVC1T45

	1 VCCA	VCCB 6	
16 SI5324_RST_B	3 A	B 4	SI5324_RST_LS_B 22
	2 GND	DIR 5	

SC70_6

U5

VCCA, VCCB = 1.2V-TO-3.6V
DIR = L => B-TO-A

GND GND

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANKS15,16 HPC FMC and XADC IF		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
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XC7A200T-FBG676 ONLY

SOC_IRON_FG676

BANK 12
XC7A200TFBG676

IO_0_12_AB22	AB22	NC	
IO_L1P_T0_12_AE25	AE25	FMC1_HPC_HA02_P	26
IO_L1N_T0_12_AE26	AE26	FMC1_HPC_HA02_N	26
IO_L2P_T0_12_AC22	AC22	FMC1_HPC_HA03_P	26
IO_L2N_T0_12_AC23	AC23	FMC1_HPC_HA03_N	26
IO_L3P_T0_DQS_12_AF24	AF24	FMC1_HPC_HA04_P	25
IO_L3N_T0_DQS_12_AF25	AF25	FMC1_HPC_HA04_N	25
IO_L4P_T0_12_AD25	AD25	FMC1_HPC_HA05_P	25
IO_L4N_T0_12_AD26	AD26	FMC1_HPC_HA05_N	25
IO_L5P_T0_12_AE23	AE23	FMC1_HPC_HA06_P	26
IO_L5N_T0_12_AF23	AF23	FMC1_HPC_HA06_N	26
IO_L6P_T0_12_AD23	AD23	FMC1_HPC_HA07_P	26
IO_L6N_T0_VREF_12_AD24	AD24	FMC1_HPC_HA07_N	26
IO_L7P_T1_12_AD21	AD21	FMC1_HPC_HA08_P	25
IO_L7N_T1_12_AE21	AE21	FMC1_HPC_HA08_N	25
IO_L8P_T1_12_AF19	AF19	FMC1_HPC_HA09_P	25
IO_L8N_T1_12_AF20	AF20	FMC1_HPC_HA09_N	25
IO_L9P_T1_DQS_12_AE22	AE22	FMC1_HPC_HA10_P	26
IO_L9N_T1_DQS_12_AF22	AF22	FMC1_HPC_HA10_N	26
IO_L10P_T1_12_AD20	AD20	FMC1_HPC_HA11_P	26
IO_L10N_T1_12_AE20	AE20	FMC1_HPC_HA11_N	26
IO_L11P_T1_SRCC_12_AB21	AB21	FMC1_HPC_HA01_CC_P	25
IO_L11N_T1_SRCC_12_AC21	AC21	FMC1_HPC_HA01_CC_N	25
IO_L12P_T1_MRCC_12_AA20	AA20	FMC1_HPC_HA17_CC_P	26
IO_L12N_T1_MRCC_12_AB20	AB20	FMC1_HPC_HA17_CC_N	26
IO_L13P_T2_MRCC_12_AA19	AA19	FMC1_HPC_HA00_CC_P	25
IO_L13N_T2_MRCC_12_AB19	AB19	FMC1_HPC_HA00_CC_N	25
IO_L14P_T2_SRCC_12_AC19	AC19	FMC1_HPC_HA12_P	25
IO_L14N_T2_SRCC_12_AD19	AD19	FMC1_HPC_HA12_N	25
IO_L15P_T2_DQS_12_AC18	AC18	FMC1_HPC_HA13_P	25
IO_L15N_T2_DQS_12_AD18	AD18	FMC1_HPC_HA13_N	25
IO_L16P_T2_12_AE18	AE18	FMC1_HPC_HA14_P	26
IO_L16N_T2_12_AF18	AF18	FMC1_HPC_HA14_N	26
IO_L17P_T2_12_Y18	Y18	FMC1_HPC_HA15_P	25
IO_L17N_T2_12_AA18	AA18	FMC1_HPC_HA15_N	25
IO_L18P_T2_12_AE17	AE17	FMC1_HPC_HA16_P	25
IO_L18N_T2_12_AF17	AF17	FMC1_HPC_HA16_N	25
IO_L19P_T3_12_AA17	AA17	FMC1_HPC_HA18_P	26
IO_L19N_T3_VREF_12_AB17	AB17	FMC1_HPC_HA18_N	26
IO_L20P_T3_12_AC17	AC17	FMC1_HPC_HA19_P	25
IO_L20N_T3_12_AD17	AD17	FMC1_HPC_HA19_N	25
IO_L21P_T3_DQS_12_Y16	Y16	FMC1_HPC_HA20_P	25
IO_L21N_T3_DQS_12_Y17	Y17	FMC1_HPC_HA20_N	25
IO_L22P_T3_12_AB16	AB16	FMC1_HPC_HA21_P	26
IO_L22N_T3_12_AC16	AC16	FMC1_HPC_HA21_N	26
IO_L23P_T3_12_Y15	Y15	FMC1_HPC_HA22_P	26
IO_L23N_T3_12_AA15	AA15	FMC1_HPC_HA22_N	26
IO_L24P_T3_12_W14	W14	FMC1_HPC_HA23_P	26
IO_L24N_T3_12_W15	W15	FMC1_HPC_HA23_N	26
IO_25_12_W16	W16	NC	

VCCO_VADJ

W17	VCCO_12_W17
AF26	VCCO_12_AF26
AE19	VCCO_12_AE19
AD22	VCCO_12_AD22
AB18	VCCO_12_AB18
AA21	VCCO_12_AA21

U1

SOC_IRON_FG676

VCCO_VADJ

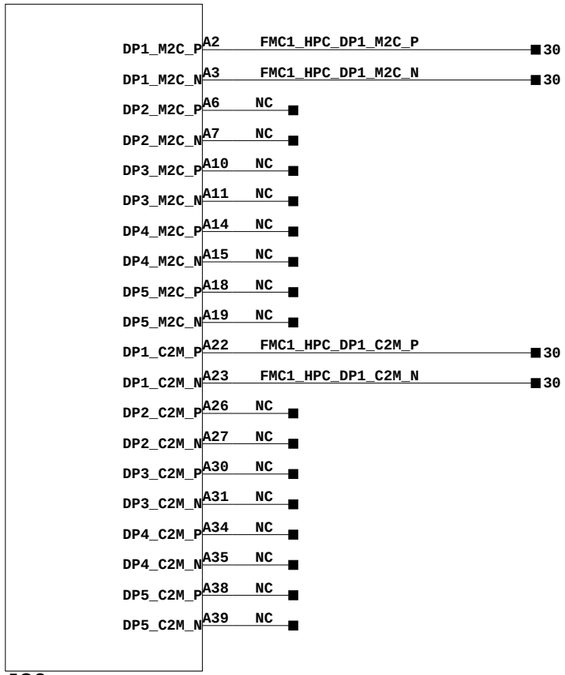
C161
100UF
6.3
X5R

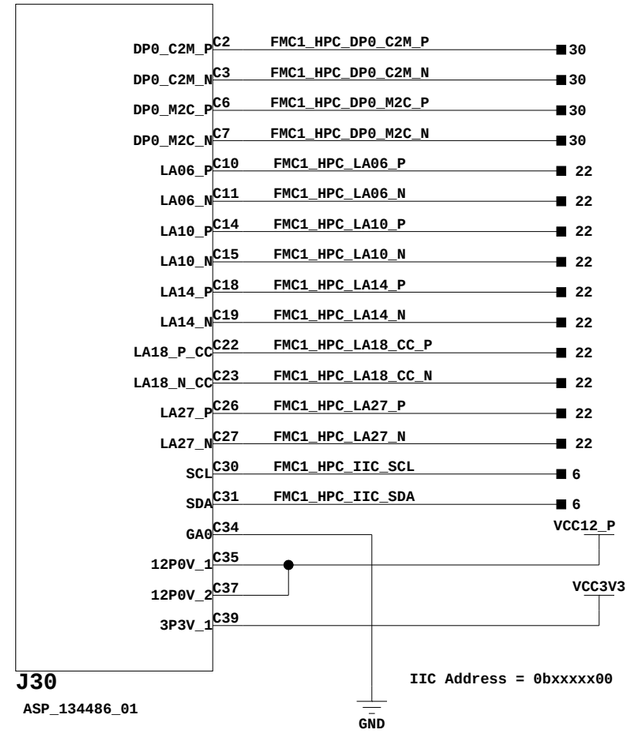
GND

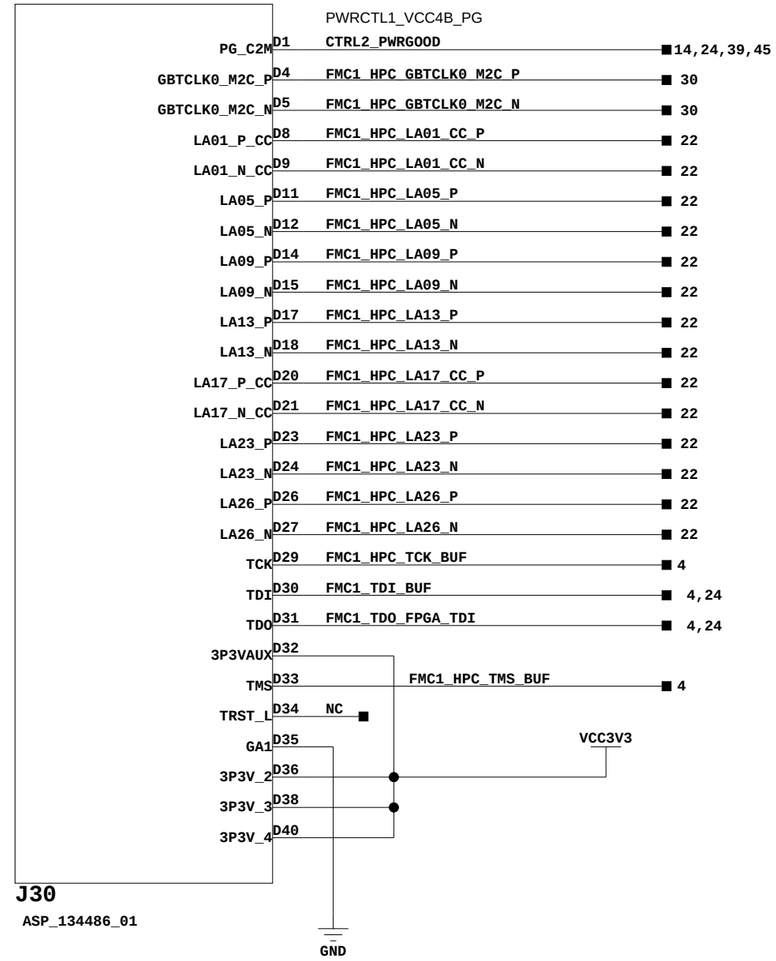
XILINX

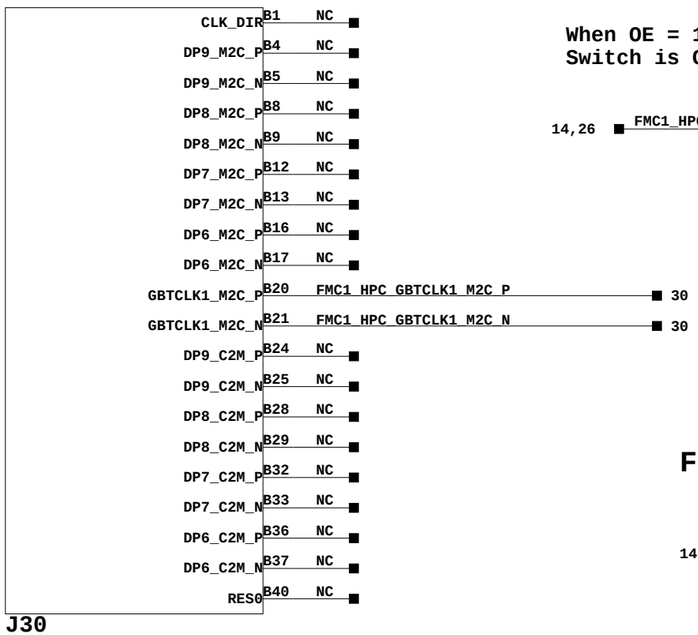
ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD BANK12 HPC FMC IF		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	23 of 51	Drawn By	DN

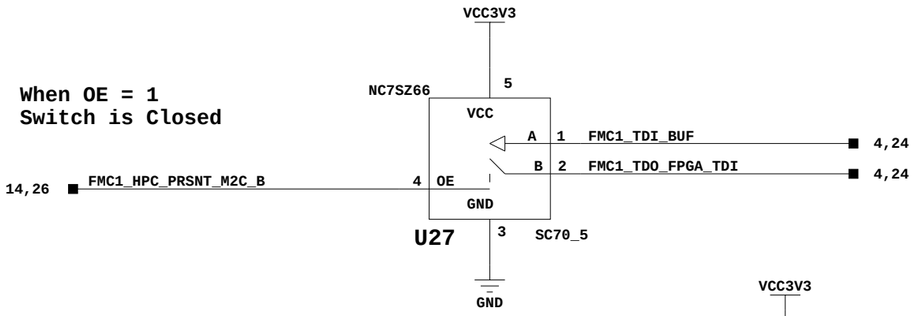




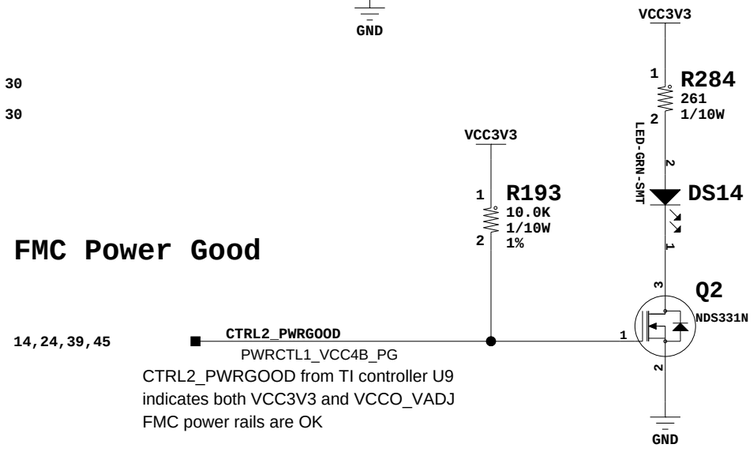




When OE = 1
Switch is Closed



FMC Power Good



CTRL2_PWRGOOD from TI controller U9 indicates both VCC3V3 and VCCO_VADJ FMC power rails are OK

ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows A, B, C, D

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS A, B, C, D		
Date:	9-20-2012_14:57	Ver:	1.0
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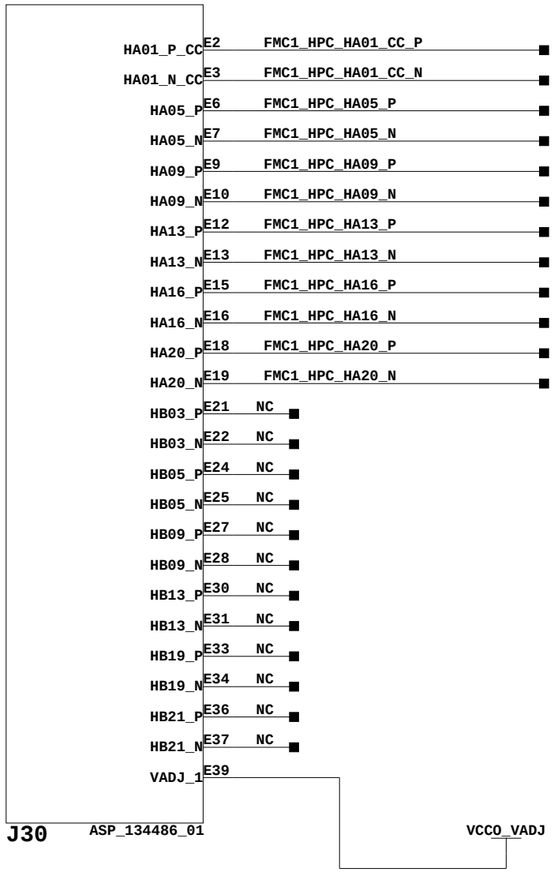
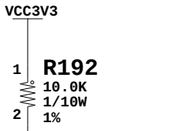
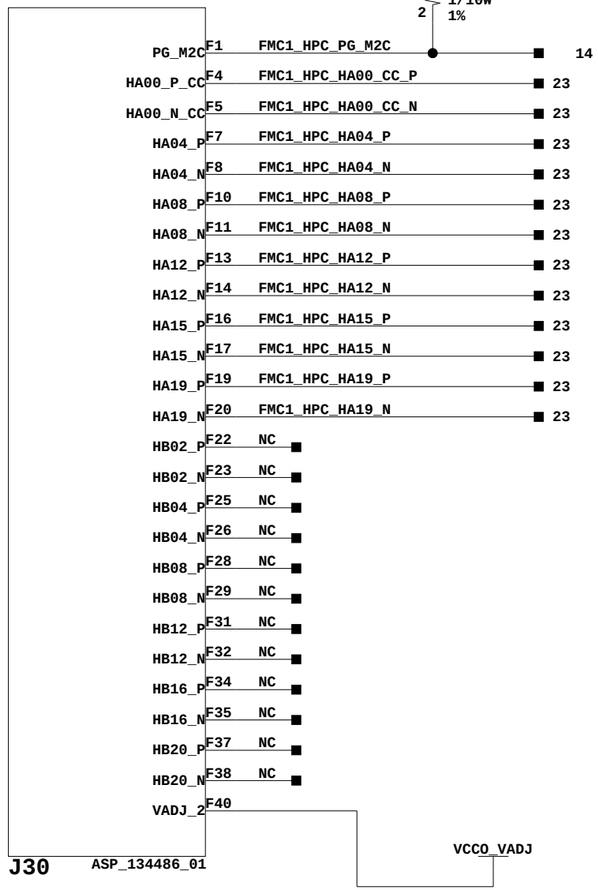
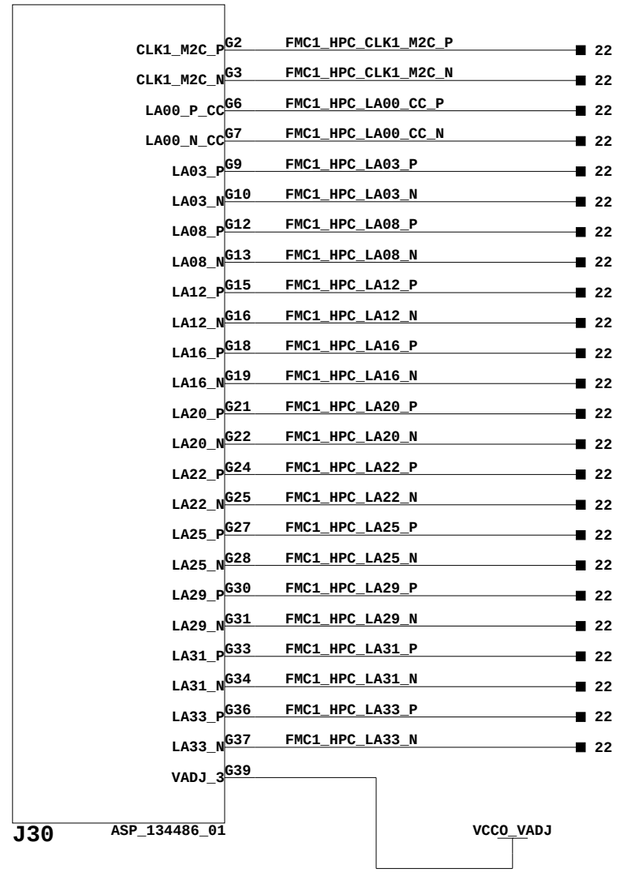
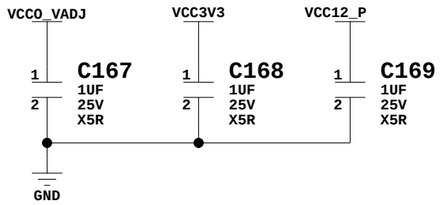








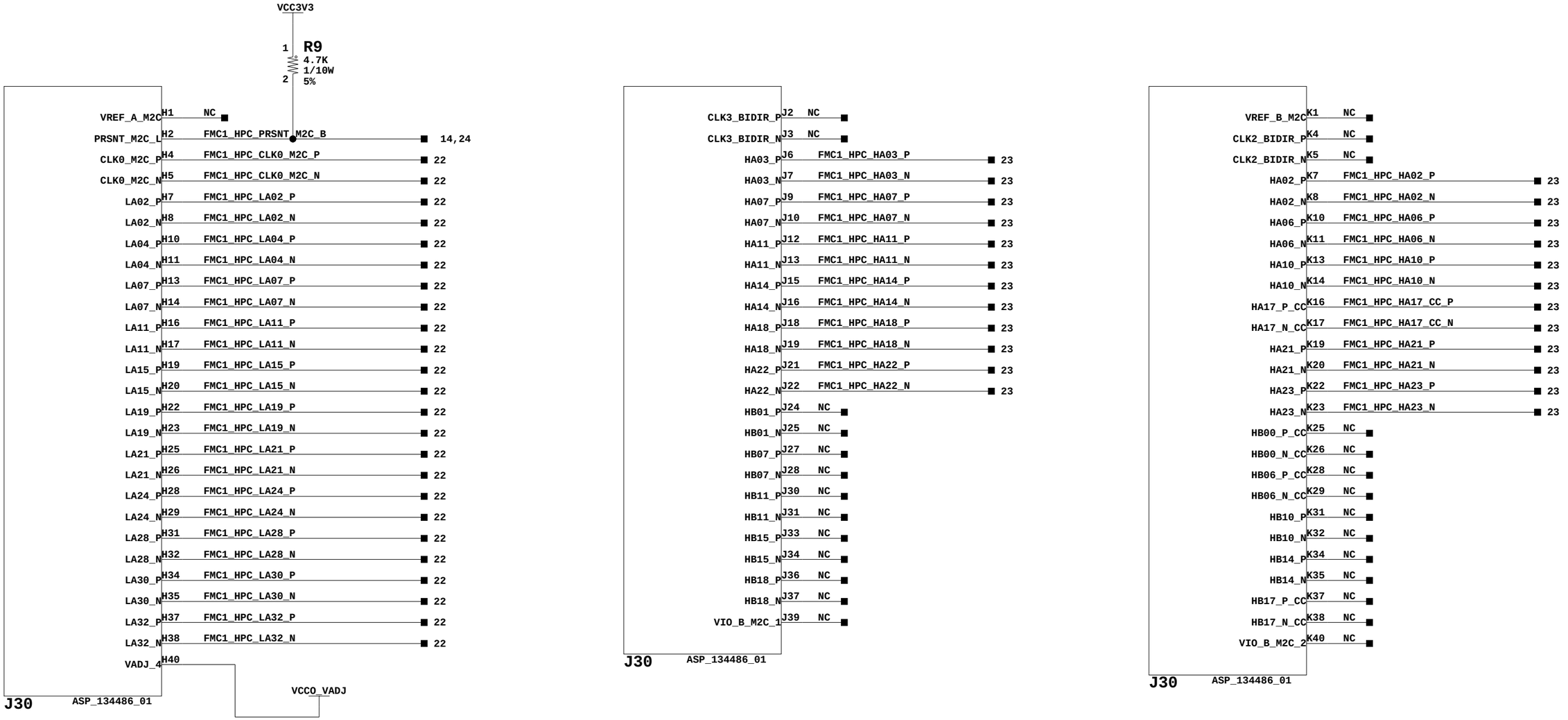


ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows E, F, G

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS E, F, G		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	25 of 51	Drawn By	DN

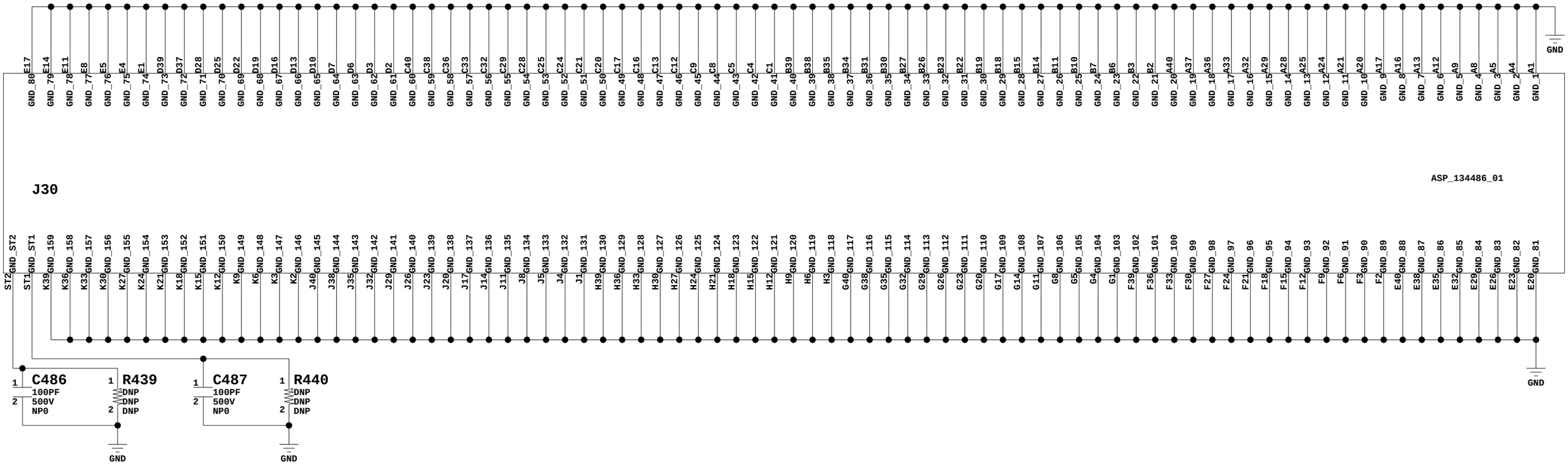


ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows H, J, K

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS H, J, K		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	26 of 51	Drawn By	DN

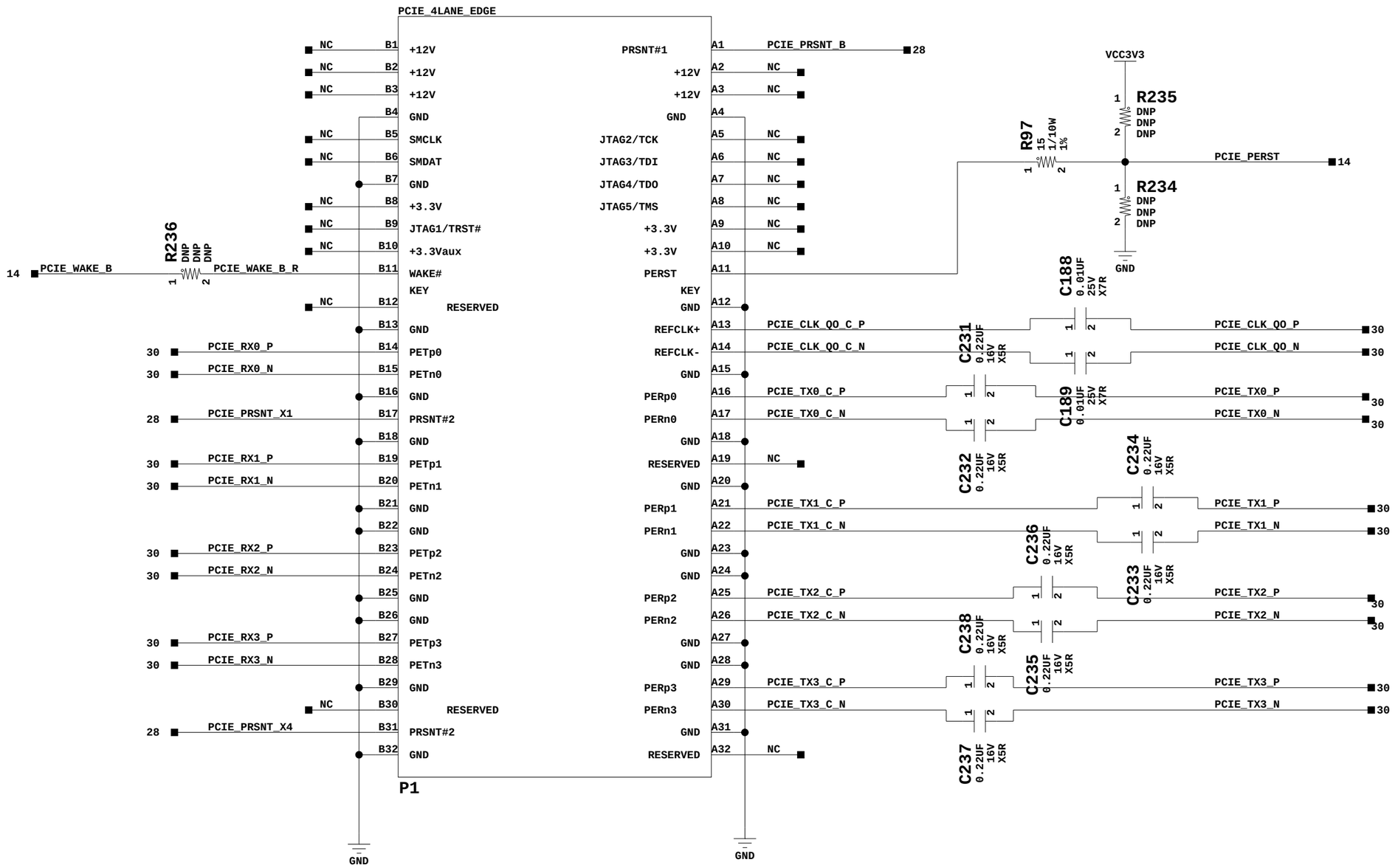


ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, GND

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FMC1 J30 ROWS GND		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	27 of 51	Drawn By	DN

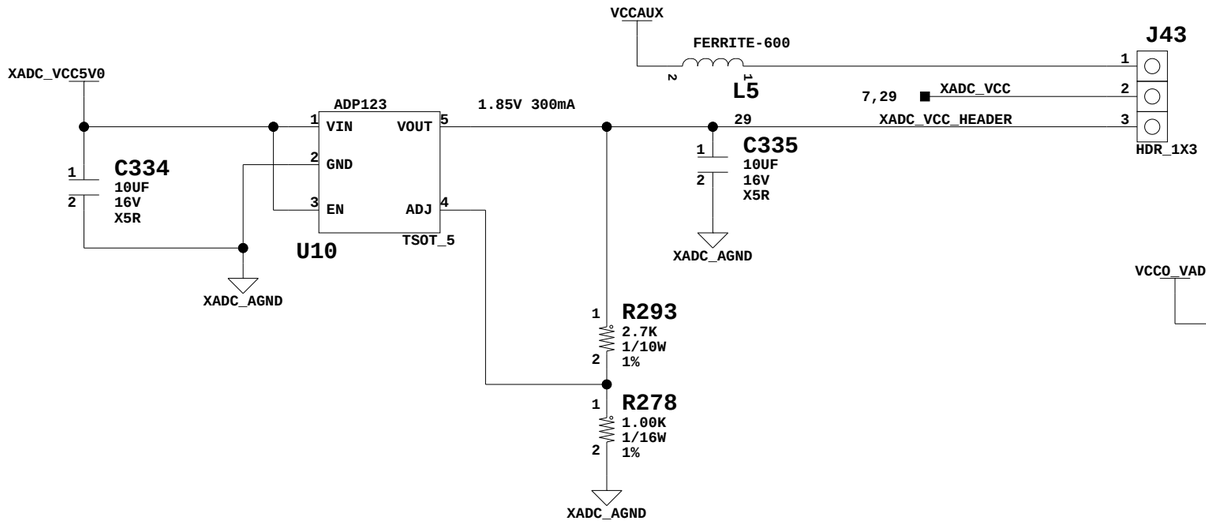


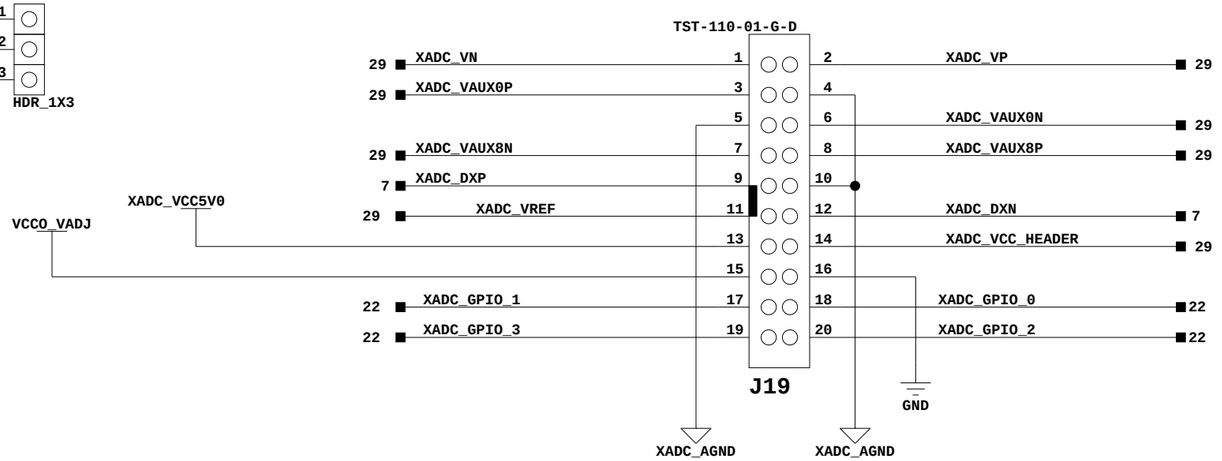
PCIe 4X Card Edge

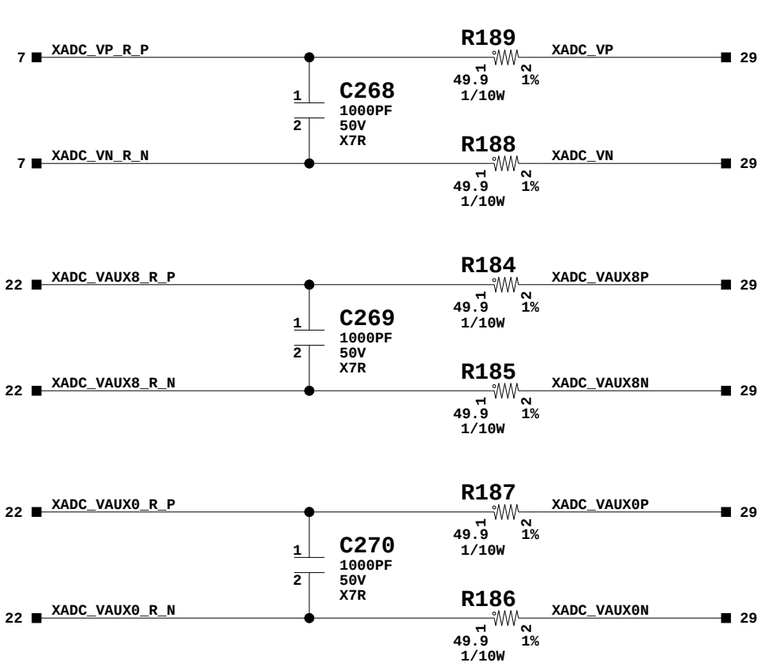
XILINX

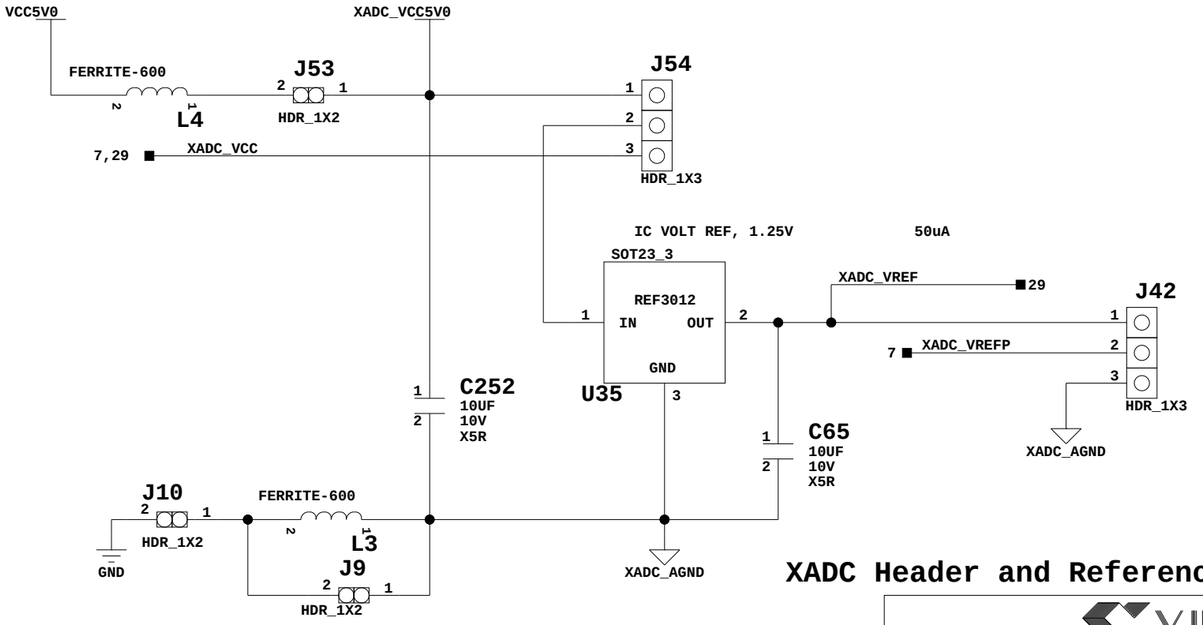
ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD PCIe 4X CARD EDGE CONN. P1		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	28 of 51	Drawn By	DN







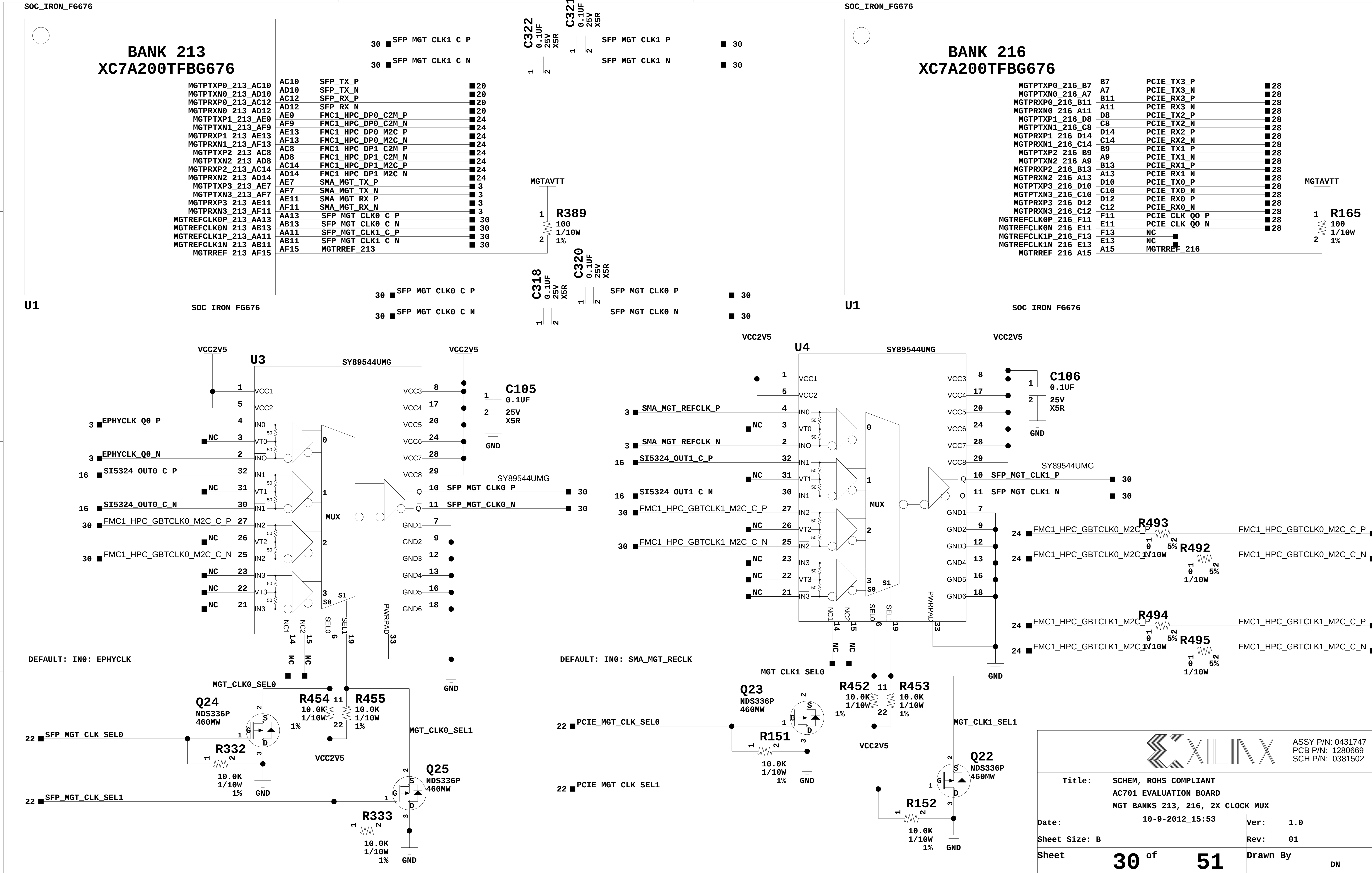


XADC Header and Reference

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC HDR. J19, XADC VREF.		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	29 of 51	Drawn By	DN



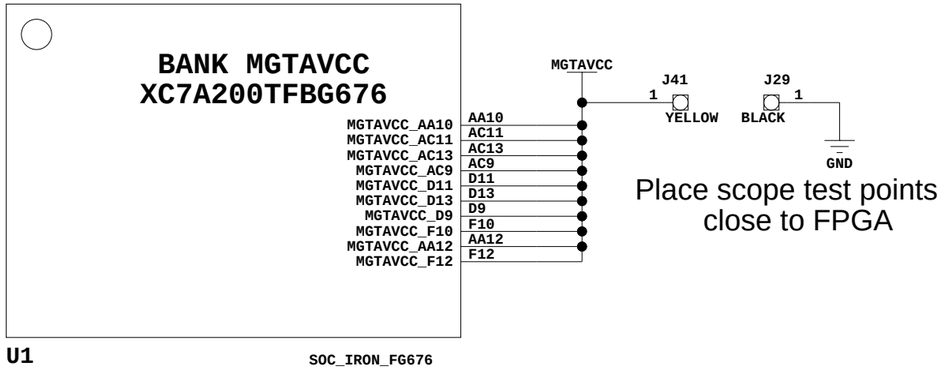
XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
MGT BANKS 213, 216, 2X CLOCK MUX

Date:	10-9-2012_15:53	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	30 of 51	Drawn By	DN

SOC_IRON_FG676

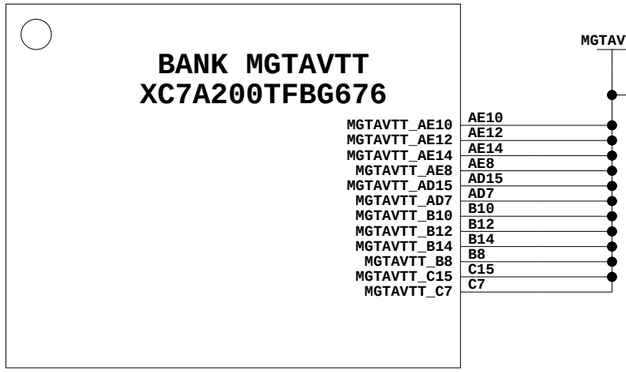


U1

SOC_IRON_FG676

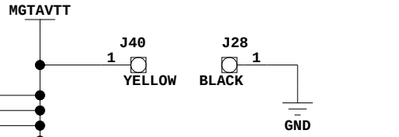
Place scope test points close to FPGA

SOC_IRON_FG676

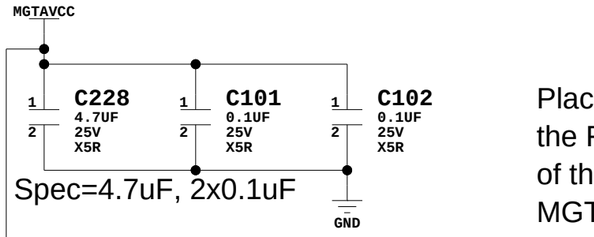


U1

SOC_IRON_FG676

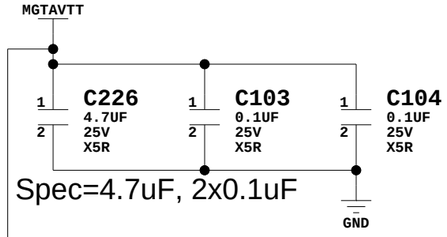


Place scope test points close to FPGA



Spec=4.7uF, 2x0.1uF

Place MGT 0.1uF caps within the FPGA via field on the bottom of the board, one for each MGT power pin/GND pin pair



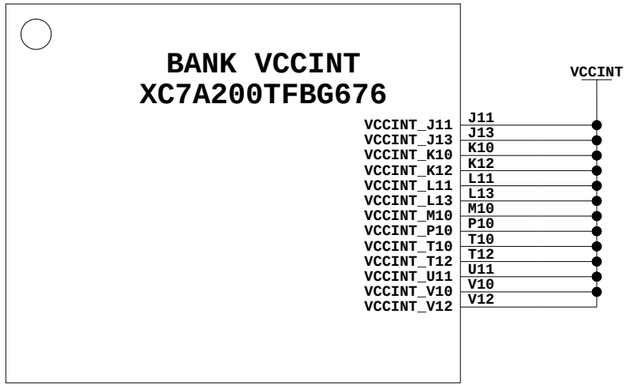
Spec=4.7uF, 2x0.1uF

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD MGT PWR. BANKS AVCC and AVTT		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	31 of 51	Drawn By	DN

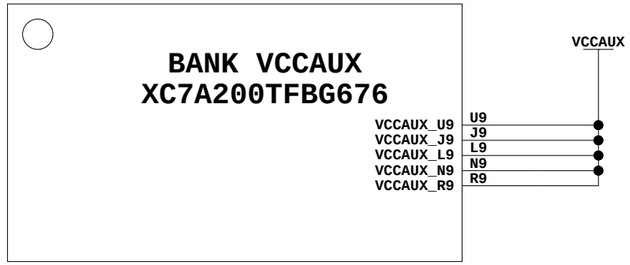
SOC_IRON_FG676



U1

SOC_IRON_FG676

SOC_IRON_FG676



U1

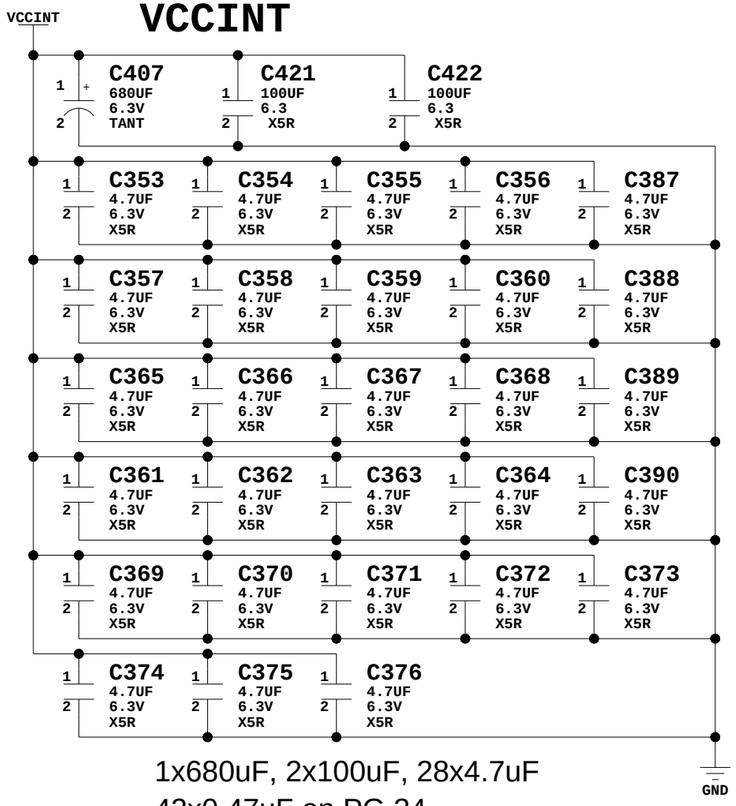
SOC_IRON_FG676

SOC_IRON_FG676

U1

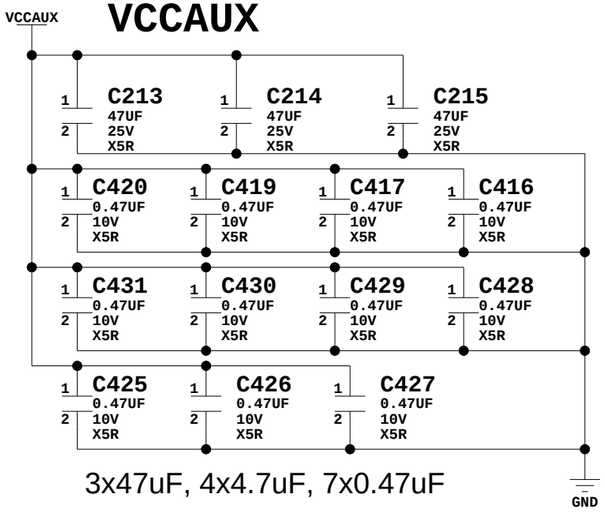
SOC_IRON_FG676

VCCINT



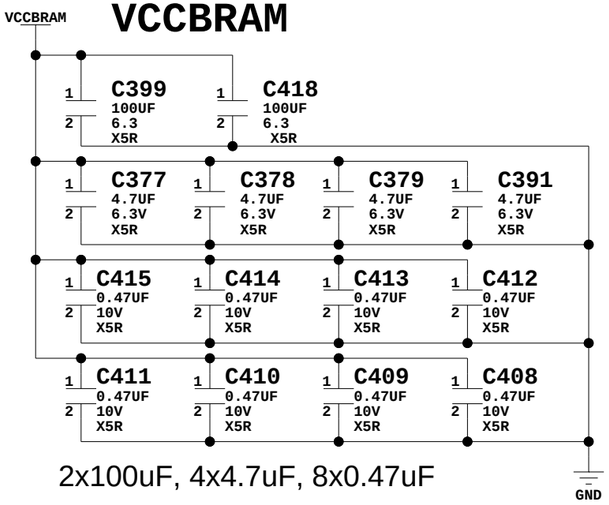
1x680uF, 2x100uF, 28x4.7uF
42x0.47uF on PG.34

VCCAUX



3x47uF, 4x4.7uF, 7x0.47uF

VCCBRAM



2x100uF, 4x4.7uF, 8x0.47uF

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FPGA CORE PWR. BANKS		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	32 of 51	Drawn By	DN

SOC_IRON_FG676

BANK GND
XC7A200TFBG676

K19	GND_K19	GND_E4	E4
P7	GND_P7	GND_E9	E9
AA26	GND_AA26	GND_E24	E24
A6	GND_A6	GND_F9	F9
A8	GND_A8	GND_F14	F14
A10	GND_A10	GND_F21	F21
A12	GND_A12	GND_E10	E10
A16	GND_A16	GND_E12	E12
AA6	GND_AA6	GND_E14	E14
A26	GND_A26	GND_E15	E15
AA14	GND_AA14	GND_G11	G11
AA16	GND_AA16	GND_G12	G12
A14	GND_A14	GND_G10	G10
AA9	GND_AA9	GND_H5	H5
AB8	GND_AB8	GND_H25	H25
AB9	GND_AB9	GND_J2	J2
AB10	GND_AB10	GND_J12	J12
AB3	GND_AB3	GND_G13	G13
AB14	GND_AB14	GND_G18	G18
AB23	GND_AB23	GND_K11	K11
AC7	GND_AC7	GND_K13	K13
AB12	GND_AB12	GND_J22	J22
AC15	GND_AC15	GND_K9	K9
AD6	GND_AD6	GND_L12	L12
AD9	GND_AD9	GND_L16	L16
AC20	GND_AC20	GND_L26	L26
AD16	GND_AD16	GND_M3	M3
AE4	GND_AE4	GND_M9	M9
AD11	GND_AD11	GND_L6	L6
AD13	GND_AD13	GND_L10	L10
AE6	GND_AE6	GND_M13	M13
AE15	GND_AE15	GND_N20	N20
AF6	GND_AF6	GND_F1	F1
AF8	GND_AF8	GND_M23	M23
AE24	GND_AE24	GND_N10	N10
AF1	GND_AF1	GND_R4	R4
AF12	GND_AF12	GND_R10	R10
AF14	GND_AF14	GND_P9	P9
AF16	GND_AF16	GND_P13	P13
AF21	GND_AF21	GND_T1	T1
AF10	GND_AF10	GND_T9	T9
B6	GND_B6	GND_R24	R24
B15	GND_B15	GND_U8	U8
B16	GND_B16	GND_U10	U10
B3	GND_B3	GND_U12	U12
B23	GND_B23	GND_U18	U18
C9	GND_C9	GND_T13	T13
C6	GND_C6	GND_P17	P17
C13	GND_C13	GND_T21	T21
C11	GND_C11	GND_V15	V15
C16	GND_C16	GND_V25	V25
T11	GND_T11	GND_W2	W2
C20	GND_C20	GND_V13	V13
D7	GND_D7	GND_Y10	Y10
D15	GND_D15	GND_Y11	Y11
D17	GND_D17	GND_Y12	Y12
V5	GND_V5	GND_Y13	Y13
E7	GND_E7	GND_Y19	Y19
E8	GND_E8	GND_W12	W12
		GND_W22	W22

GND GND

U1 SOC_IRON_FG676

VCCINT

VCCINT

C437	C436	C435	C434	C433	C432
C443	C442	C441	C440	C439	C438
C455	C454	C453	C452	C451	C450
C449	C448	C447	C446	C445	C444
C470	C469	C468	C467	C466	C465
C464	C460	C459	C458	C457	C456

0.47UF 10V X5R

42x0.47uF

GND

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

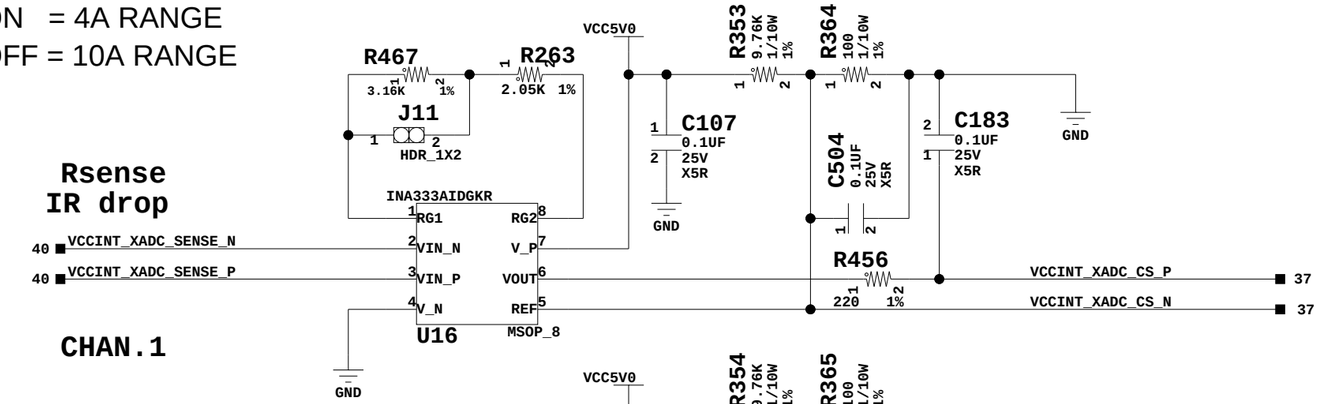
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FPGA PWR. BANK GND		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	33 of 51	Drawn By	DN

XADC I/F MONITORING CIRCUIT PAGE 1

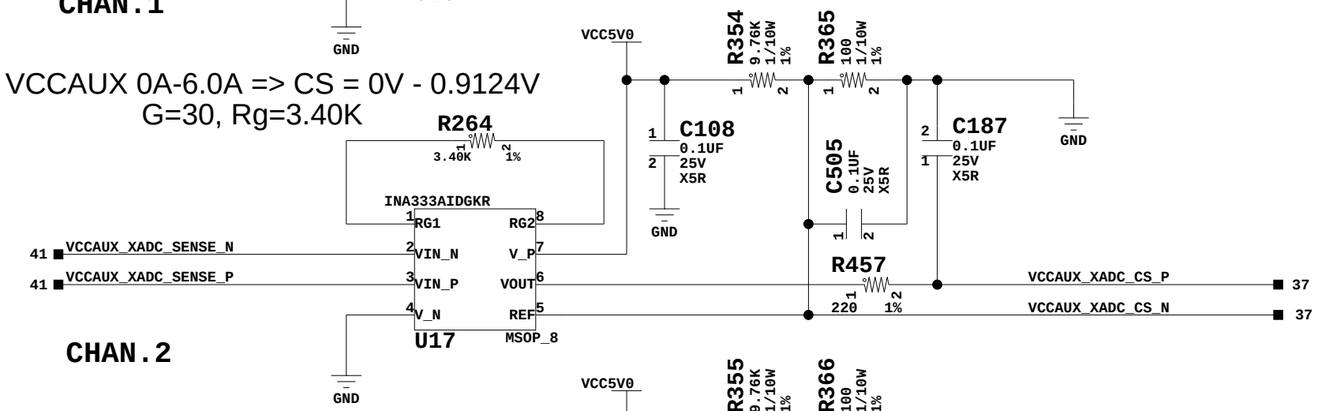
VCCINT 0A-10A => CS = 0V - 1.009V G=20, Rg=5.21K
VCCINT 0A-4A => CS = 0V - 0.996V G=50, Rg=2.05K

J11 ON = 4A RANGE

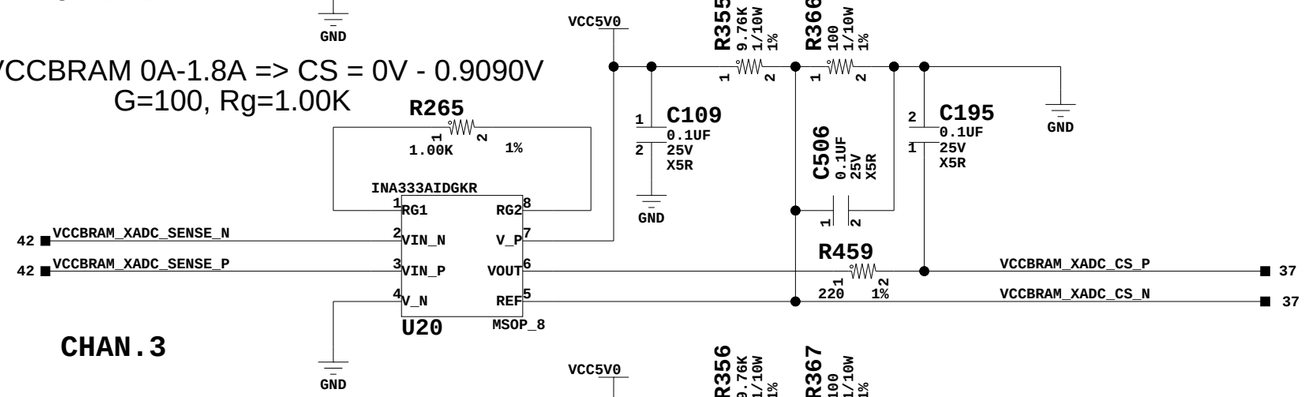
J11 OFF = 10A RANGE



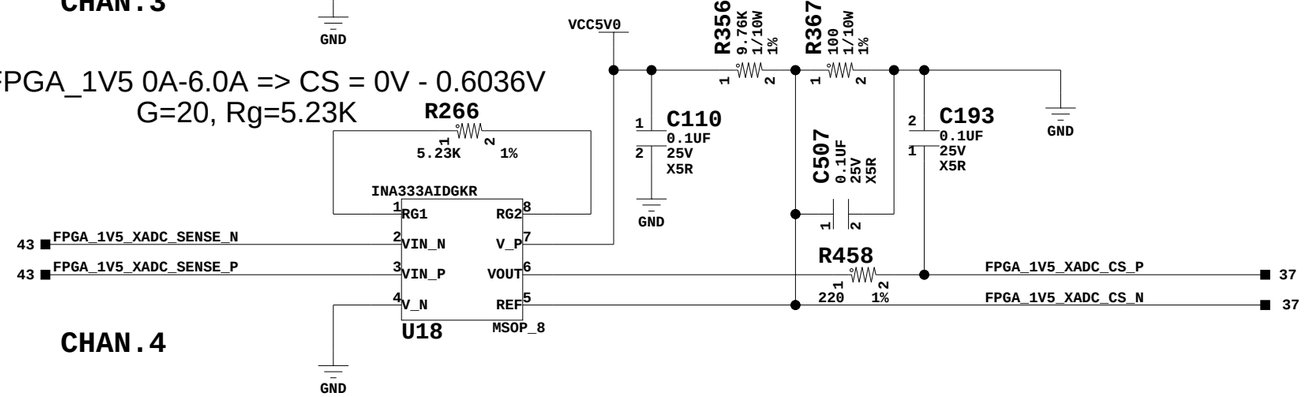
VCCAUX 0A-6.0A => CS = 0V - 0.9124V
G=30, Rg=3.40K



VCCBRAM 0A-1.8A => CS = 0V - 0.9090V
G=100, Rg=1.00K

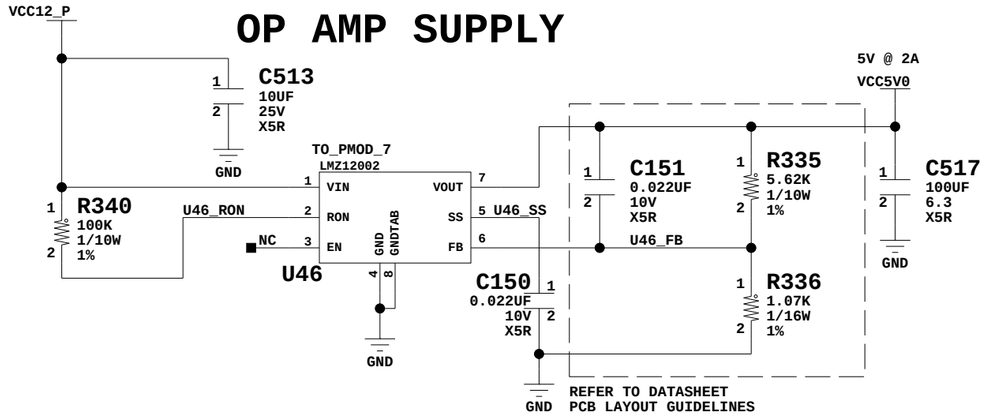


FPGA_1V5 0A-6.0A => CS = 0V - 0.6036V
G=20, Rg=5.23K

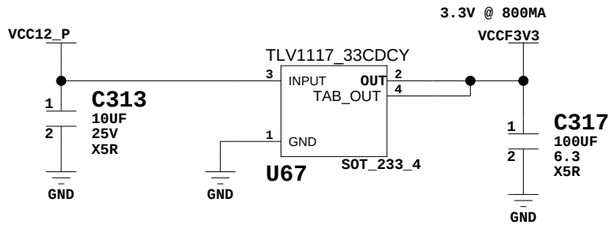


CONTROLLER #1

OP AMP SUPPLY



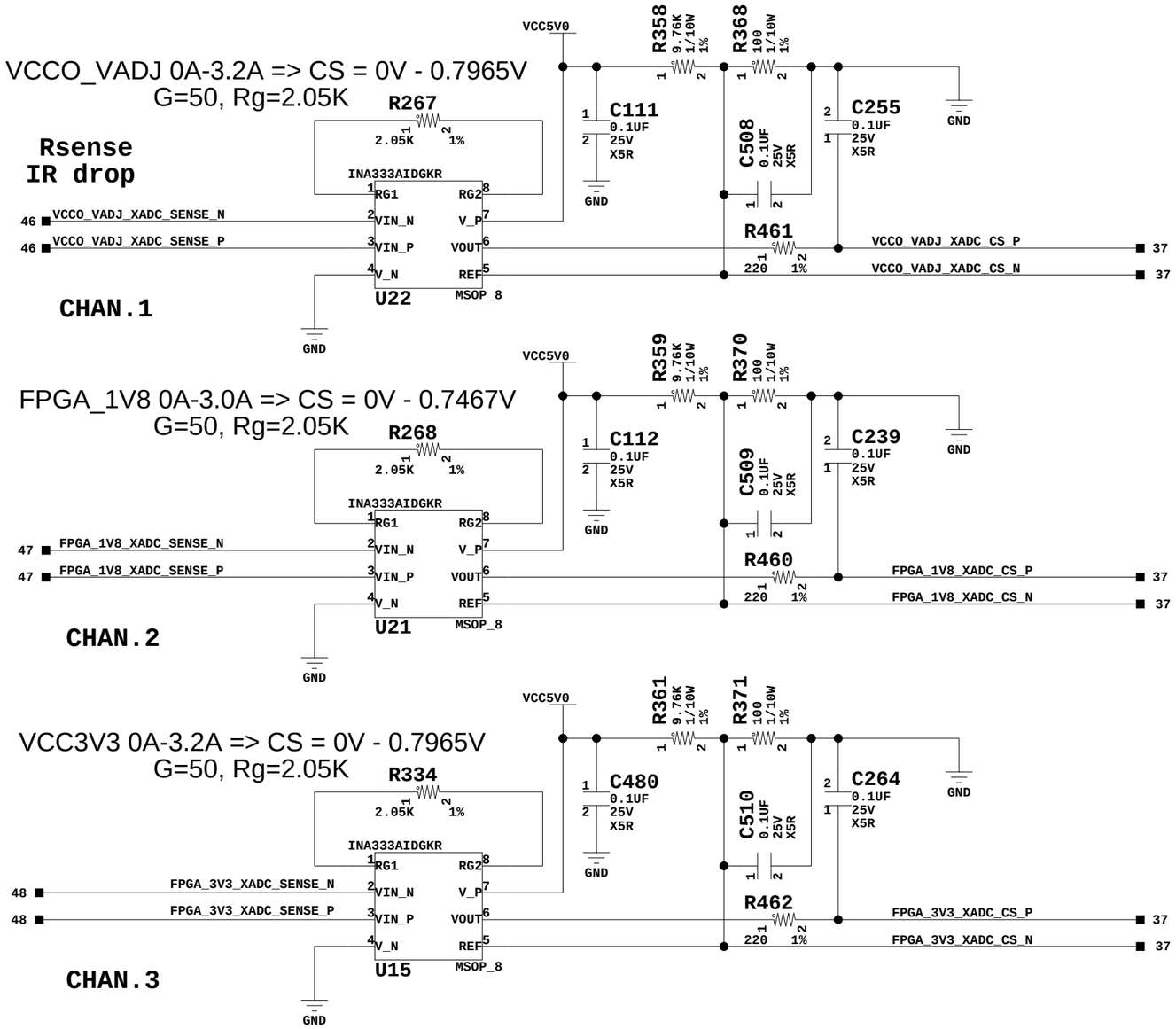
3.3V IMMEDIATE ON FIXED SUPPLY



XILINX	ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502		
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. OP AMPS		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	34 of 51	Drawn By	DN

XADC I/F MONITORING CIRCUIT PAGE 2

CONTROLLER #2



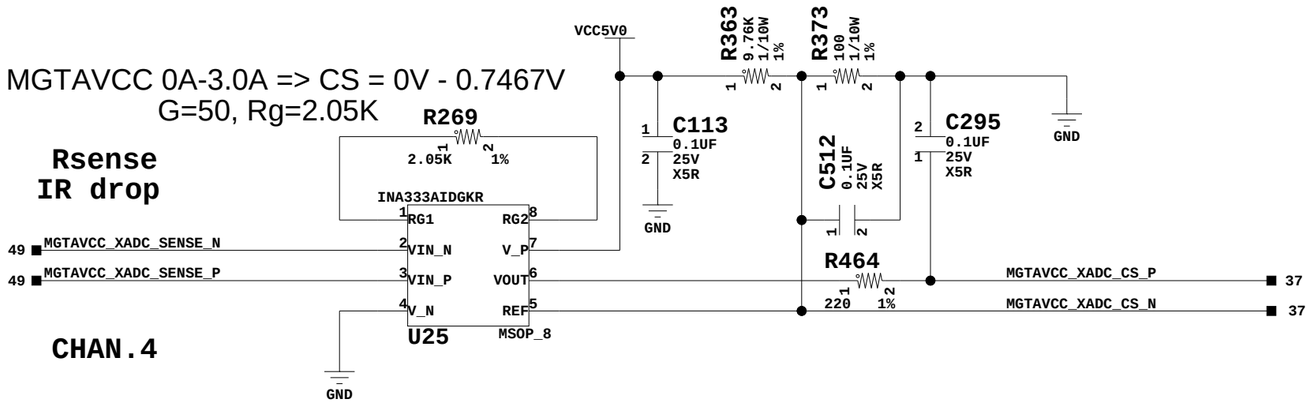
XILINX

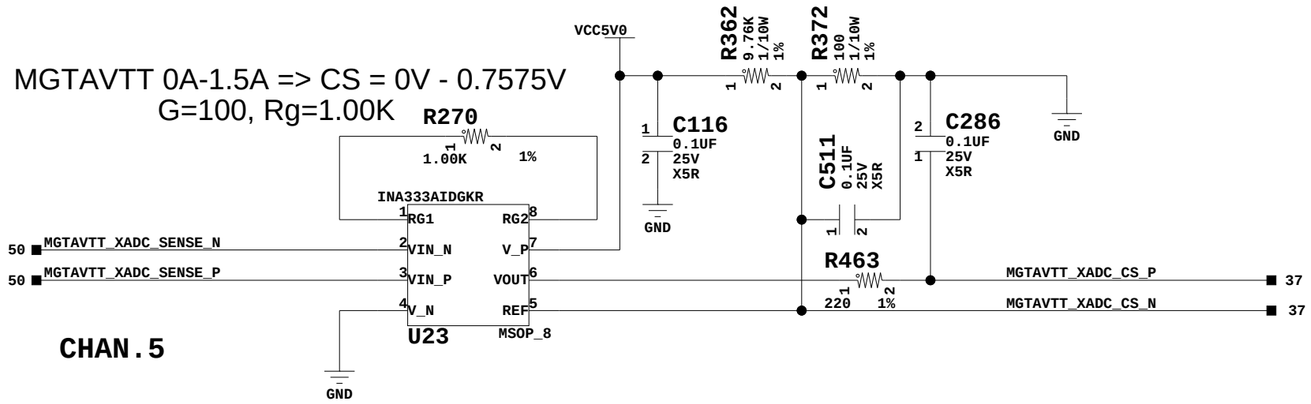
ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. OP AMPS		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	35 of 51	Drawn By	DN

XADC I/F MONITORING CIRCUIT PAGE 3

CONTROLLER #2



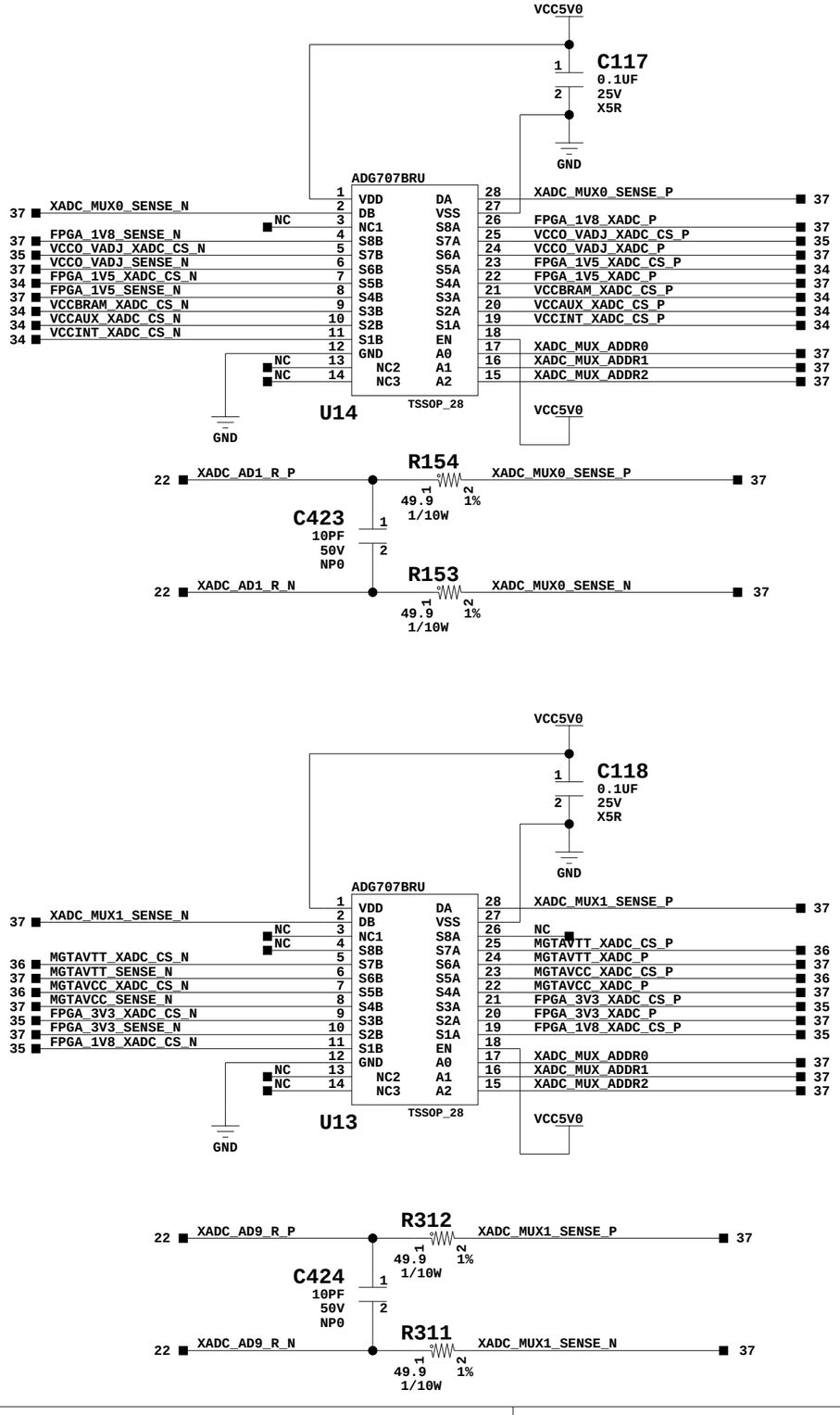


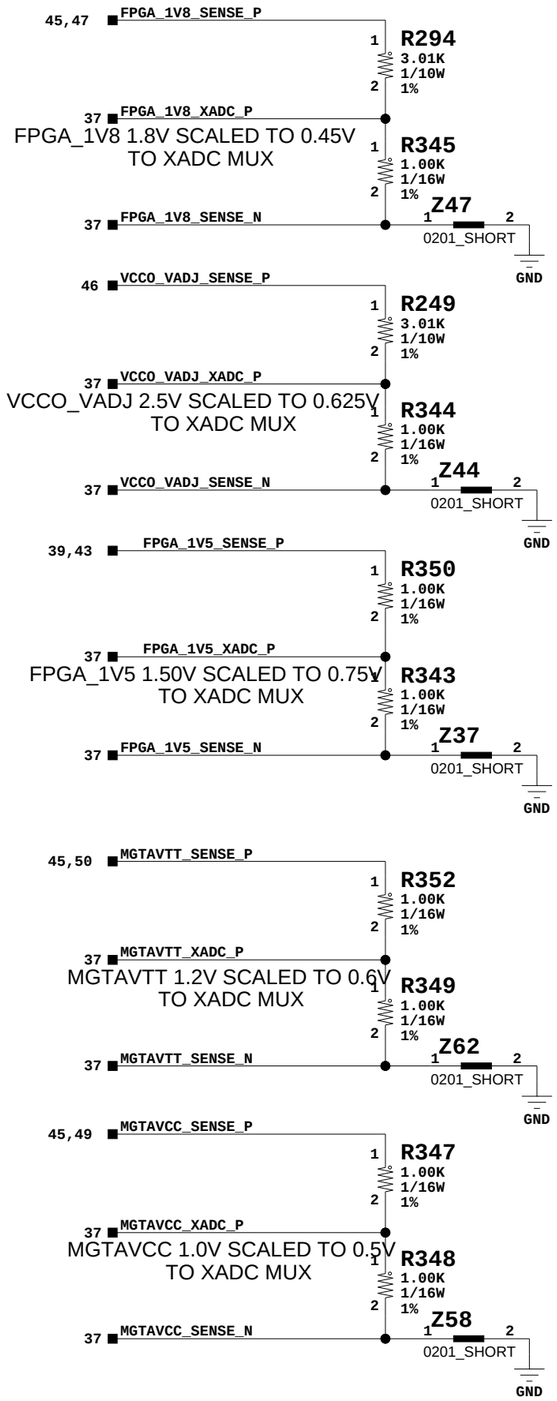
XILINX

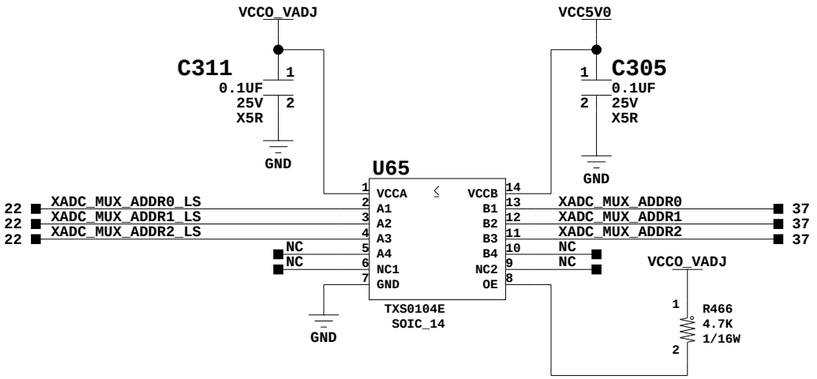
ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

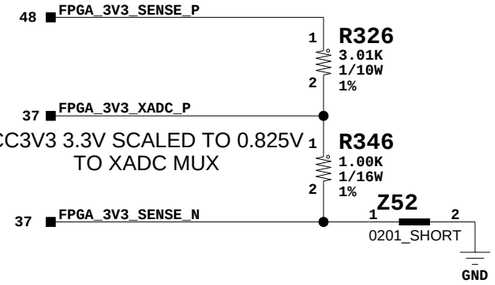
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. OP AMPS		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	36 of 51	Drawn By	DN

XADC I/F MONITORING CIRCUIT PAGE 4



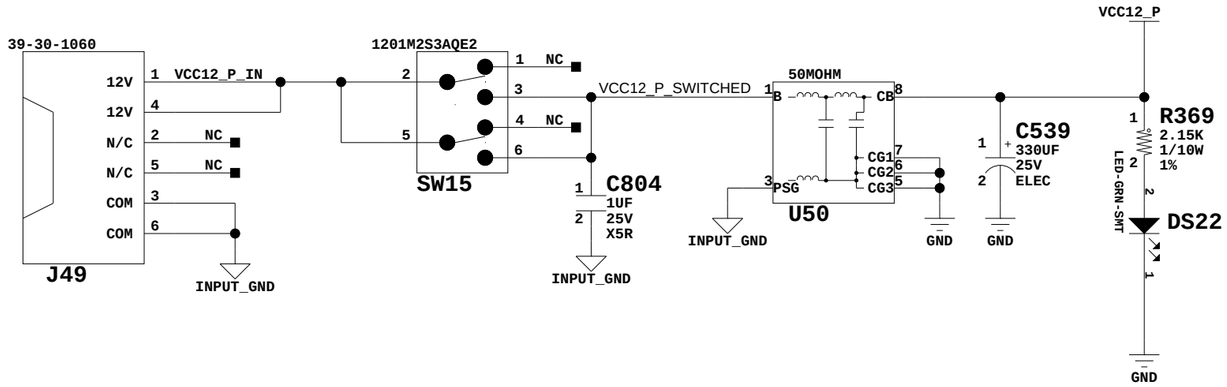






XILINX		ASSY P/N: 0431747 PCB P/N: 1280669 SCH P/N: 0381502	
Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD XADC MON. 2X MUX		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	37 of 51	Drawn By	DN

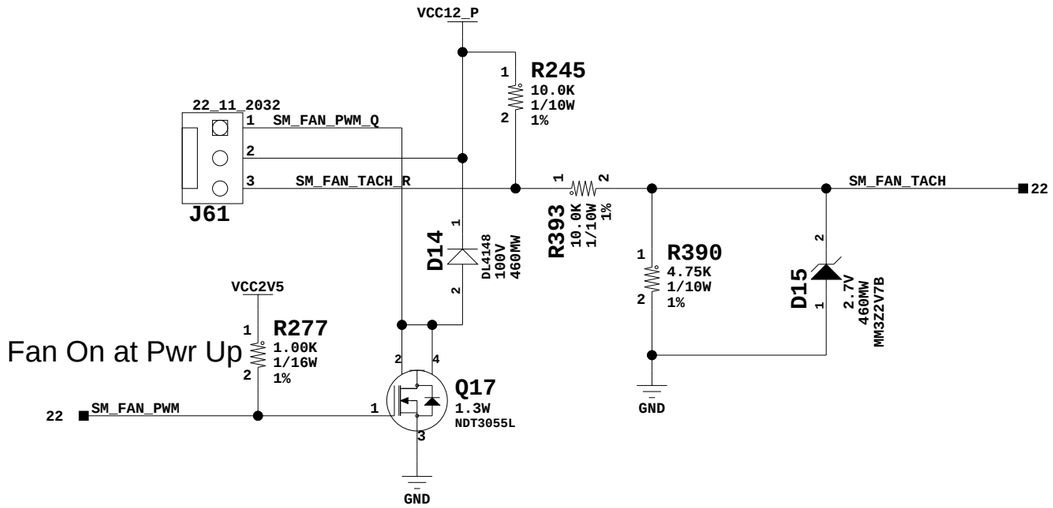
POWER SYSTEM SCHEMATIC STARTS HERE



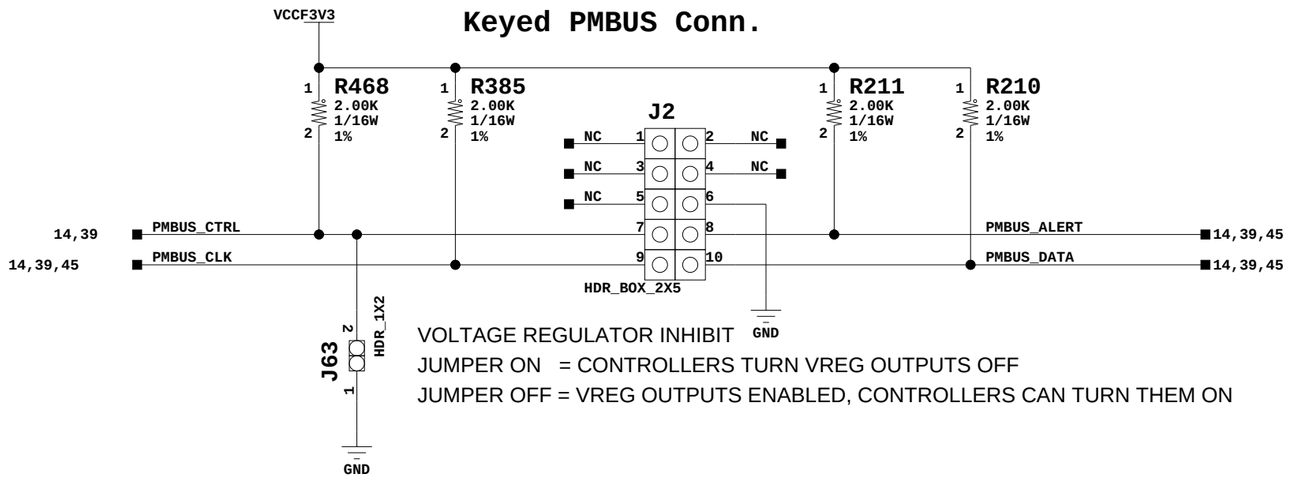
AC701 POWER SYSTEM CONFIGURATION

CTLR REF	PAGE	PMBUS ADDR/RAIL	NET NAME	VOLTAGE	VREG-TYPE	MAX I
#1 U8	PG 39	101 UCD90120A	4 RAILS:			
	PG 40	101 1	VCCINT	1.0V	LMZ12010 U49	10A
	PG 41	101 2	VCCAUX	1.8V	TPS84621 U53	6A
	PG 42	101 3	VCCBRAM	1.0V	TPS84320 U54	3A
	PG 43	101 4	FPGA_1V5	1.5V	TPS84621 U55	6A
#2 U9	PG 45	102 UCD90120A	5 RAILS:			
	PG 46	102 1	VCCO_VADJ	2.5V	TPS84621 U56	6A
	PG 47	102 2	FPGA_1V8	1.8V	TPS84320 U57	3A
	PG 48	102 3	FPGA_3V3	3.3V	TPS84621 U58	6A
	PG 49	102 4	MGTAVCC	1.0V	TPS84320 U59	3A
	PG 49	102 5	MGTAVTT	1.2V	TPS84320 U60	3A

Keyed Fan Header



Keyed PMBUS Conn.



VOLTAGE REGULATOR INHIBIT
JUMPER ON = CONTROLLERS TURN VREG OUTPUTS OFF
JUMPER OFF = VREG OUTPUTS ENABLED, CONTROLLERS CAN TURN THEM ON

Power Connector and switch, PMBus Header

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
POWER CONN.,SWITCH,PMBUS HEADER,FAN CONTROL

Date:	12-3-2012_12:58	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	38 of 51	Drawn By	DN

CORE,VCCO/DDR3 DIMM POWER

VOLTAGE SENSE FILTERS

39,40 VCCINT_SENSE_P
39,41 VCCAUX_SENSE_P
39,42 VCCBRAM_SENSE_P
37,39,43 FPGA_1V5_SENSE_P

Tap into GND close to the SENSE_P pin

C536 0.01UF, C540 0.01UF, C538 0.01UF, C537 0.01UF → GND

VOLTAGE SENSE

39,40 VCCINT_SENSE_P → MON1
39,41 VCCAUX_SENSE_P → MON2
39,42 VCCBRAM_SENSE_P → MON3
37,39,43 FPGA_1V5_SENSE_P → MON4
39 CTRL1_SHUTDOWN_B → MON5
NC → MON6
V33D_CTL1 → V33DIO1
DVSS1
RESET_B
NC → TRCK
40 VCCINT_EN → GPIO1
42 VCCBRAM_EN → GPIO2
41 VCCAUX_EN → GPIO3
43 FPGA_1V5_EN → GPIO4
14,38,45 PMBUS_CLK → PMBUS_CLK
14,38,45 PMBUS_DATA → PMBUS_DATA

RAIL ENABLES

R379 10.0K, R380 10.0K, R377 10.0K, R376 10.0K → GND

C516 0.1UF 25V X5R → GND

V33D_CTL2 → R375 10.0K 1/10W 1% → C553 1000PF 50V X7R → GND

VCCBRAM_CS_R, VCCAUX_CS_R, VCCINT_CS_R, FPGA_1V5_CS_R

R328 60.6K 1/10W 1%, R351 41.2K 1/10W 1% → GND

C535 0.01UF, C534 0.01UF, C532 0.01UF, C533 0.01UF → GND

R472 1.00K VCCBRAM_CS_P → 42
R473 1.00K VCCAUX_CS_P → 41
R474 1.00K VCCINT_CS_P → 40
R475 1.00K FPGA_1V5_CS_P → 43

CURRENT SENSE

CURRENT SENSE FILTERS

Tap into GND close to the SENSE_P pin

U61 TPS79433DCQ SOT223_6 3.3V 250MA
GNDTAB, EN, VIN, GND, VOUT, NR

VCC5V0 → C514 1UF 25V X5R → GND
V33D_CTL1 → C518 0.01UF 25V X7R, C152 4.7UF 6.3V X5R
NR_CTL1

AGND

U8

THERM_PAD 65, AVSS3 64, MON9 63, MON8 62, PMBUS_ADDR0 61, PMBUS_ADDR1 60, MON7 59, V33FB 58, NC4 57, MON13 56, NC3 55, MON12 54, NC2 53, MON11 52, NC1 51, MON10 50, AVSS1 49

AVSS2 48, BPCAP 47, V33A 46, V33D 45, V33DIO2 44, DVSS3 43
PWM3_GPI3 42 NC, PWM4_GPI4 41 NC, TRST_B 40, TMS_GPIO19 39 NC, TDI_GPIO19 38 NC, TDO_GPIO19 37 NC, TCK_GPIO19 36 NC
GPIO18 35 CTRL1_PWRGOOD
GPIO17 34 LOW_PWR_SEL → 40
GPIO16 33 NC

FPWM1_GPIO5 17, FPWM2_GPIO6 18, FPWM3_GPIO7 19, FPWM4_GPIO8 20, FPWM5_GPIO9 21, FPWM6_GPIO10 22, FPWM7_GPIO11 23, FPWM8_GPIO12 24, GPIO13 25, DVSS2 26, PMBUSALERT_B 27, PMBUS_CTRL 28, GPIO14 29, GPIO15 30, PWM1_GPI1 31, PWM2_GPI2 32

PMBus Addr 101

UCD90120ARGC
VQFN_64

C325 0.01UF 25V X7R, C123 0.1UF 25V X5R → AGND

V33A_CTL1

PLACE CLOSE TO Ux PINS44,45

C122 0.1UF 25V X5R, C120 0.1UF 25V X5R, C380 4.7UF 6.3V X5R, C121 0.1UF 25V X5R, C381 4.7UF 6.3V X5R → AGND

L21 FERRITE-220 2A
V33D_CTL1 → C119 0.1UF 25V X5R → AGND

VCC3V3 → R419 261 1/10W → LED-GRN-SMT DS6 → GND

R374 10.0K 1/10W 1% → GND

R413 4.7K 1/16W → GND

Q21 NDS331N

R471 1.00K 1/16W 1% → GND
CTRL2_SHUTDOWN_B
R470 1.00K 1/16W 1%
CTRL2_SEQUENCE_ON → 45
CTRL2_PWRGOOD → 14,24,45

VCCF3V3 → R482 10.0K 1/10W
R481 10.0K 1/10W 1% → GND

EN_CTLR1_SHUTDOWN → 45

39 CTRL1_SHUTDOWN_B

U68 NC7SZ66 SC70_5
VCC, A, B, OE, GND

R483 4.7K 1/16W

CTLR1 SHUTDOWN ENABLE
HI = CLOSE SWITCH, ENABLE S/D
LO = OPEN SWITCH, INHIBIT S/D

N.O. SWITCH
RON=5 OHMS

MARGIN TRIM

MARGIN R4's

40 VCCINT_TRIM → R395 4.64K 1%
41 VCCAUX_TRIM → R397 1.58K 1%
42 VCCBRAM_TRIM → R399 3.74K 1%
43 FPGA_1V5_TRIM → R398 1.96K 1%

C489 2200PF 25V X7R, C493 1000PF 50V X7R, C483 1000PF 50V X7R, C154 1000PF 50V X7R → AGND

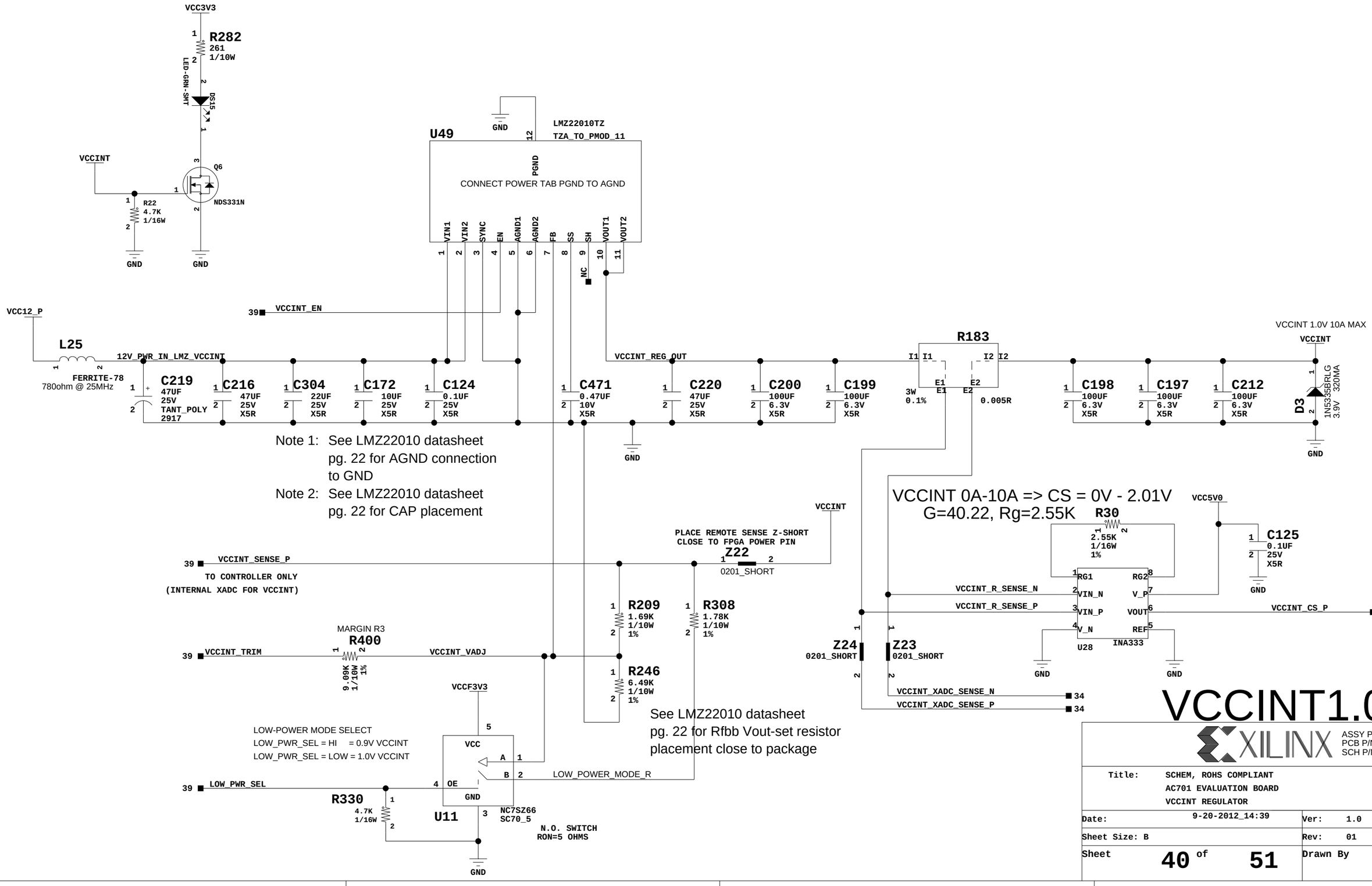
MARGIN C1's

14,38
14,38,45

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD UCD90120A CTLR #1 ADDR 101		
Date:	10-24-2012_11:45	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	39 of 51	Drawn By	DN

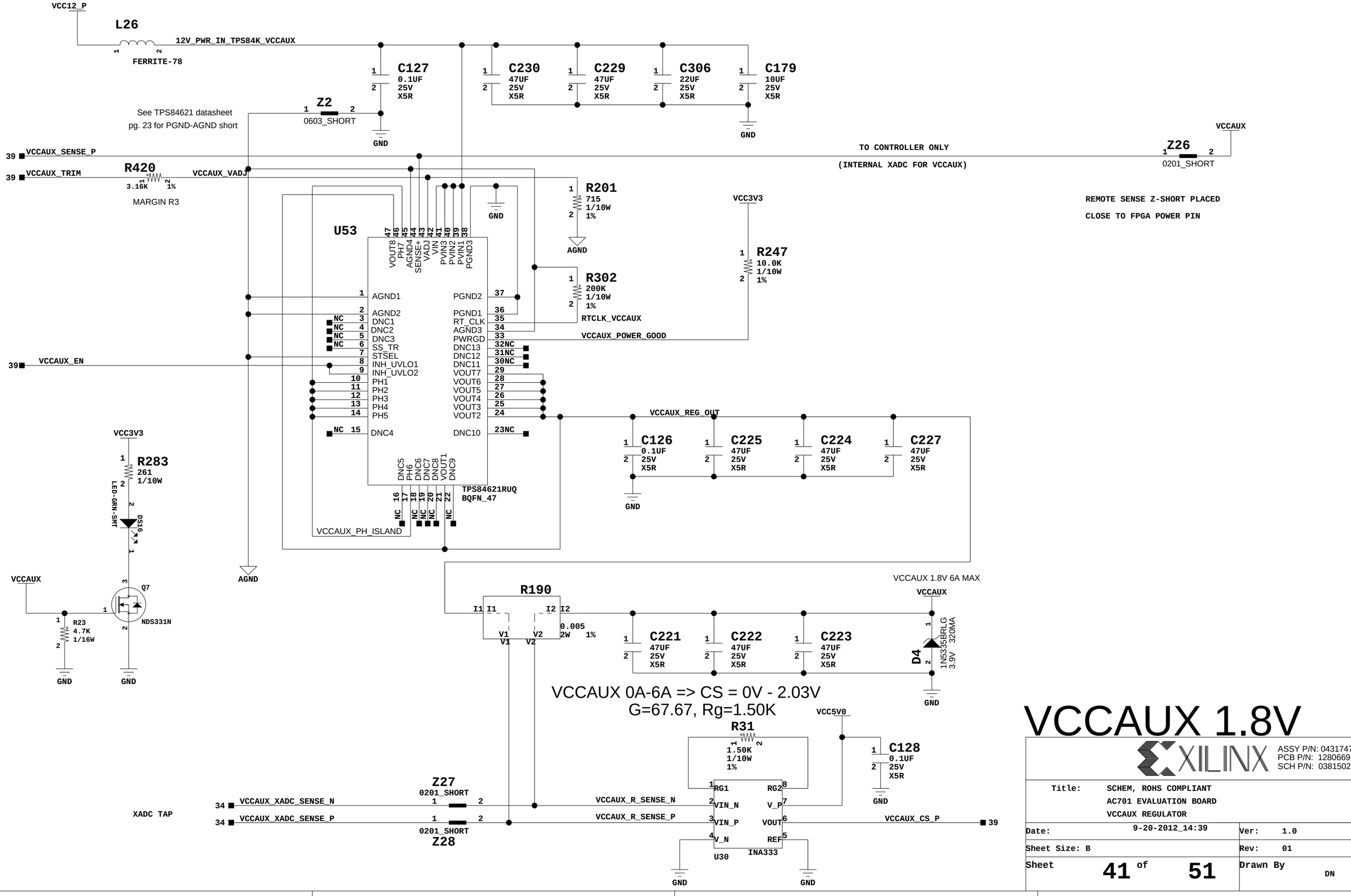


VCCINT1.0V

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCINT REGULATOR		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	40 of 51	Drawn By	DN

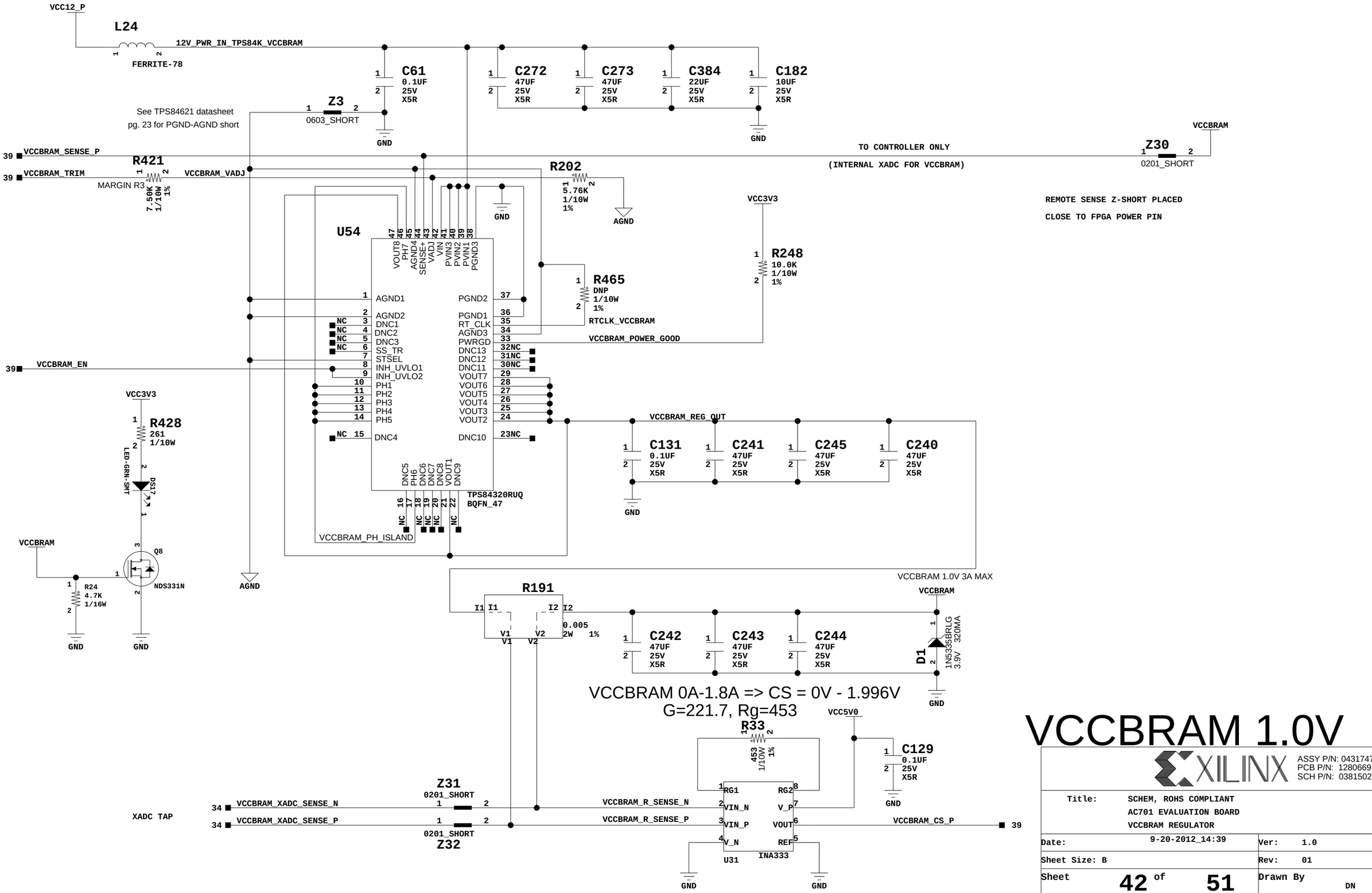


VCCAUX 1.8V

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCAUX REGULATOR		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	41 of 51	Drawn By	DN

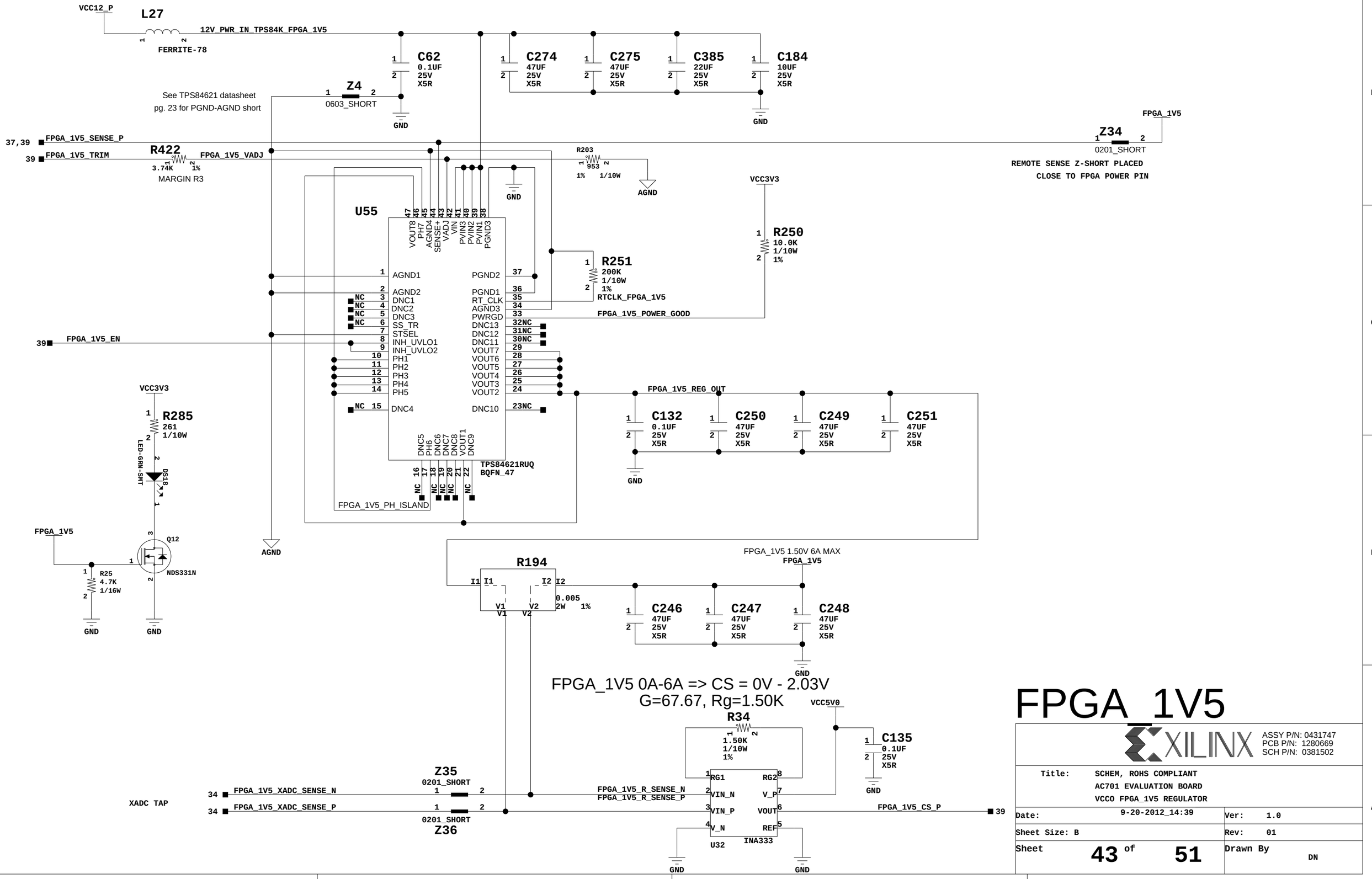


VCCBRAM 1.0V

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCBRAM REGULATOR		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	42 of 51	Drawn By	DN



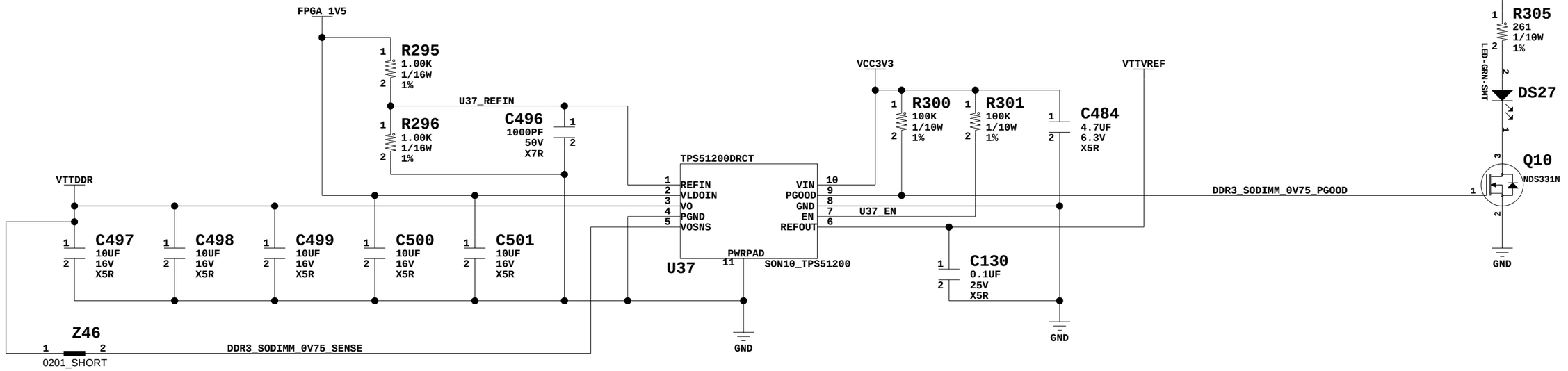
FPGA_1V5

XILINX

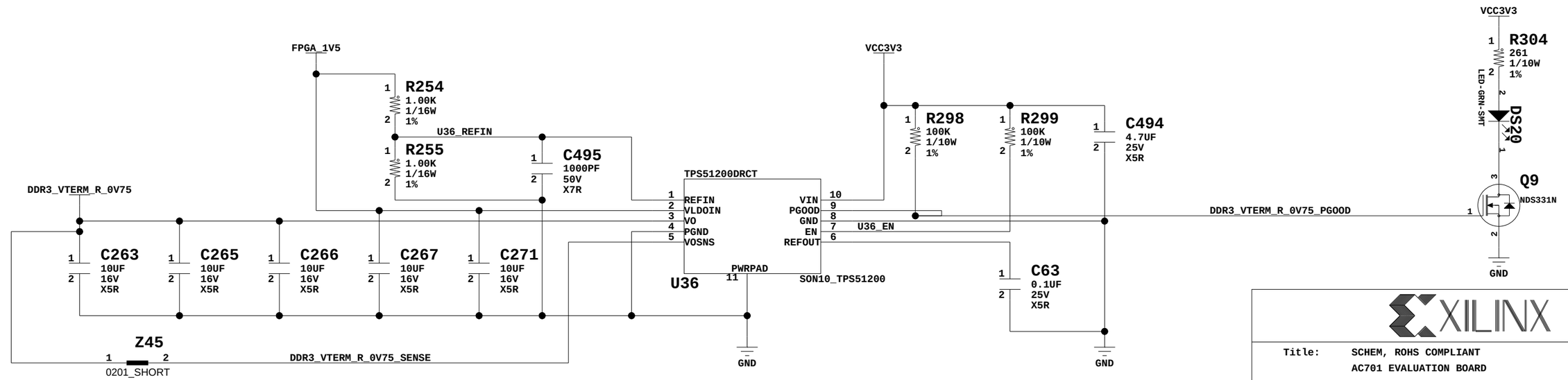
ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD VCCO FPGA_1V5 REGULATOR		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	43 of 51	Drawn By	DN

DDR3 SODIMM TERM. REGULATOR, 0.75v @ 3A



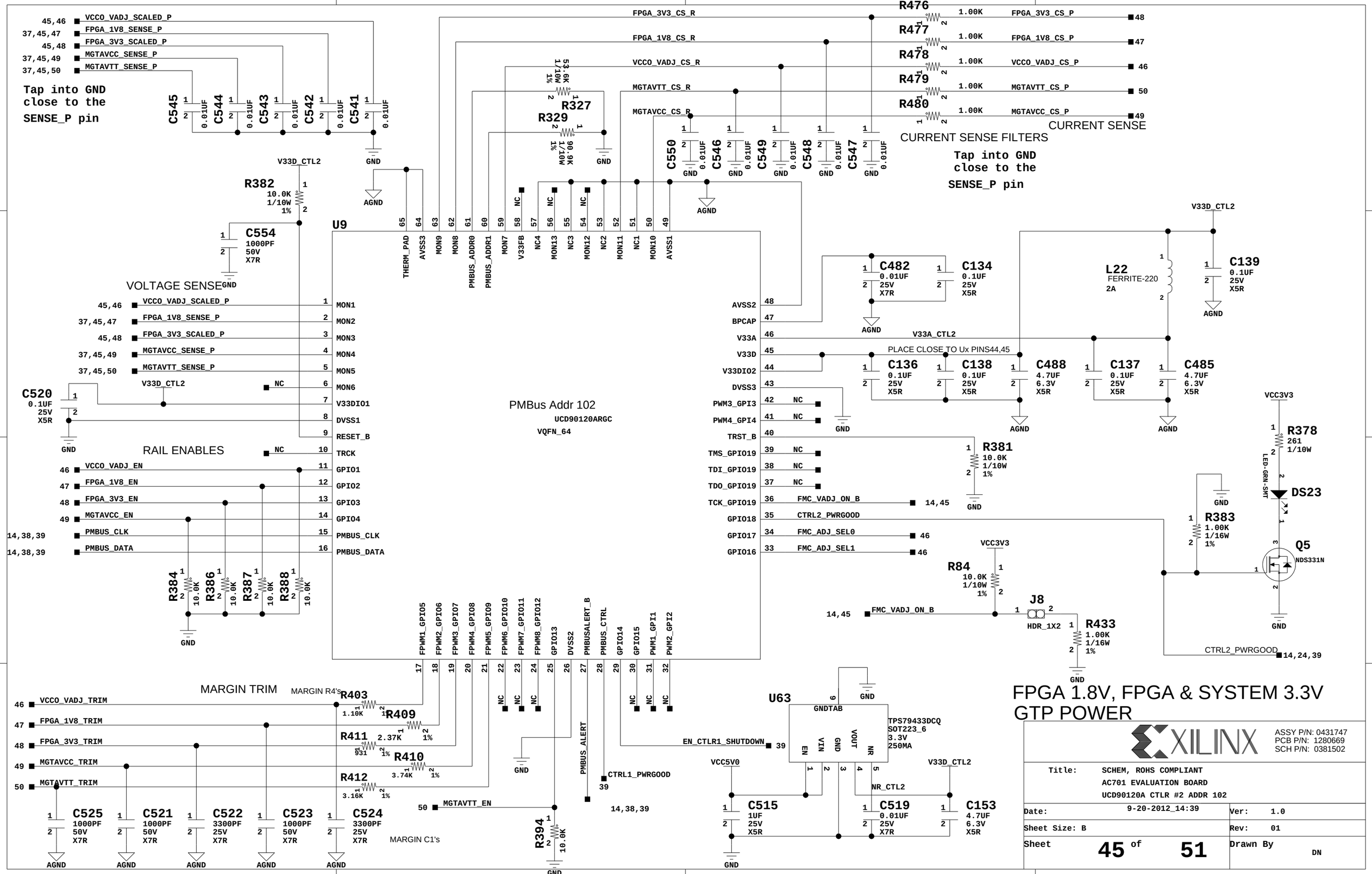
DDR3 SODIMM MEM. TERM. RESISTOR REGULATOR, 0.75v @ 3A

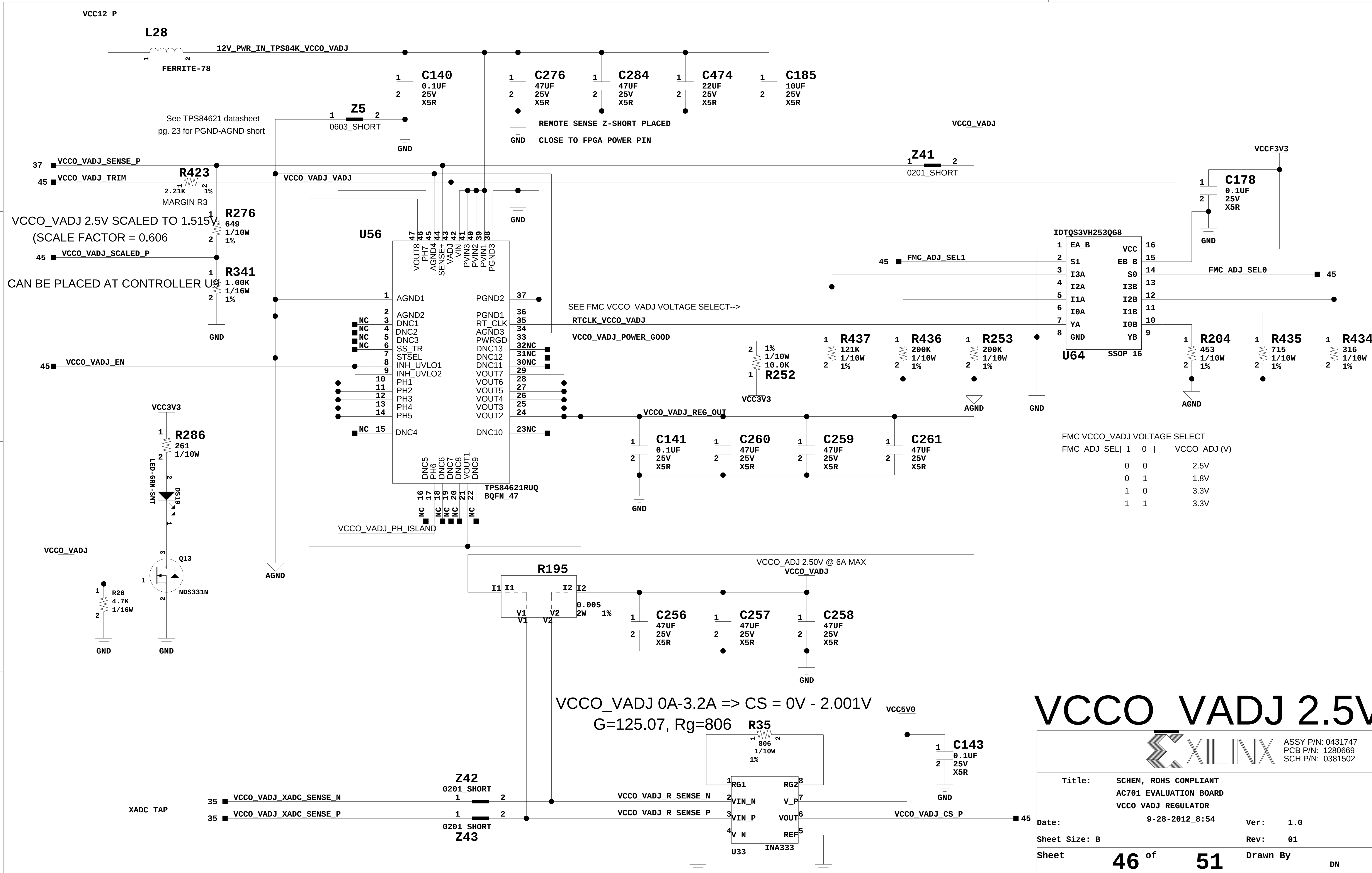


XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD DDR3 MEMORY TERM. REGULATOR		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	44 of 51	Drawn By	DN


45,46 VCCO_VADJ_SCALED_P
37,45,47 FPGA_1V8_SENSE_P
45,48 FPGA_3V3_SCALED_P
37,45,49 MGTAVCC_SENSE_P
37,45,50 MGTAVTT_SENSE_P
Tap into GND close to the SENSE_P pin
C545 C544 C543 C542 C541 0.01UF
GND
V33D_CTL2
R382 10.0K 1/10W 1%
C554 1000PF 50V X7R
VOLTAGE SENSE
AGND
U9
THERM_PAD AVSS3 MON9 MON8 PMBUS_ADDR0 PMBUS_ADDR1 MON7 V33FB NC4 MON13 NC3 MON12 NC2 MON11 NC1 MON10 AVSS1
45,46 VCCO_VADJ_SCALED_P
37,45,47 FPGA_1V8_SENSE_P
45,48 FPGA_3V3_SCALED_P
37,45,49 MGTAVCC_SENSE_P
37,45,50 MGTAVTT_SENSE_P
MON1 MON2 MON3 MON4 MON5 MON6
V33DIO1 DVSS1 RESET_B TRCK GPIO1 GPIO2 GPIO3 GPIO4 PMBUS_CLK PMBUS_DATA
C520 0.1UF 25V X5R
V33D_CTL2
NC
RAIL ENABLES
46 VCCO_VADJ_EN
47 FPGA_1V8_EN
48 FPGA_3V3_EN
49 MGTAVCC_EN
14,38,39 PMBUS_CLK
14,38,39 PMBUS_DATA
R384 R386 R387 R388 10.0K
PMBus Addr 102
UCD90120ARGC
VQFN_64
FPWM1_GPIO5 FPWM2_GPIO6 FPWM3_GPIO7 FPWM4_GPIO8 FPWM5_GPIO9 FPWM6_GPIO10 FPWM7_GPIO11 FPWM8_GPIO12 GPIO13 DVSS2 PMBUSALERT_B PMBUS_CTRL GPIO14 GPIO15 PWM1_GPI1 PWM2_GPI2
MARGIN TRIM
MARGIN R4's
46 VCCO_VADJ_TRIM
47 FPGA_1V8_TRIM
48 FPGA_3V3_TRIM
49 MGTAVCC_TRIM
50 MGTAVTT_TRIM
R403 1.10K
R409 2.37K
R411 931
R410 3.74K
R412 3.16K
1%
C525 1000PF 50V X7R
C521 1000PF 50V X7R
C522 3300PF 25V X7R
C523 1000PF 50V X7R
C524 3300PF 25V X7R
MARGIN C1's
AGND
50 MGTAVTT_EN
R394 10.0K
GND
NC
CTRL1_PWRGOOD
39
14,38,39
FPGA_3V3_CS_R
FPGA_1V8_CS_R
VCCO_VADJ_CS_R
MGTAVTT_CS_R
MGTAVCC_CS_R
R476 R477 R478 R479 R480 1.00K
FPGA_3V3_CS_P 48
FPGA_1V8_CS_P 47
VCCO_VADJ_CS_P 46
MGTAVTT_CS_P 50
MGTAVCC_CS_P 49
CURRENT SENSE
CURRENT SENSE FILTERS
53.6K 1/10W 1%
R327
R329 90.9K 1/10W 1%
C550 C546 C549 C548 C547 0.01UF
Tap into GND close to the SENSE_P pin
AVSS2 BPCAP V33A V33D V33DIO2 DVSS3 PWM3_GPI3 PWM4_GPI4 TRST_B TMS_GPIO19 TDI_GPIO19 TDO_GPIO19 TCK_GPIO19 GPIO18 GPIO17 GPIO16
48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
C482 0.01UF 25V X7R
C134 0.1UF 25V X5R
V33A_CTL2
PLACE CLOSE TO Ux PINS44,45
C136 C138 0.1UF 25V X5R
C488 4.7UF 6.3V X5R
C137 0.1UF 25V X5R
C485 4.7UF 6.3V X5R
L22 FERRITE-220 2A
C139 0.1UF 25V X5R
R381 10.0K 1/10W 1%
FMC_VADJ_ON_B 14,45
FMC_ADJ_SEL0 46
FMC_ADJ_SEL1 46
CTRL2_PWRGOOD 14,24,39
R84 10.0K 1/10W 1%
J8 HDR_1X2
R433 1.00K 1/16W 1%
R378 261 1/10W
LED-GRN-SMT
DS23
R383 1.00K 1/16W 1%
Q5 NDS331N
U63 GNDTAB
TPS79433DCQ SOT223_6 3.3V 250MA
EN VIN GND VOUT NR
EN_CTLR1_SHUTDOWN 39
NR_CTL2
VCC5V0
C515 1UF 25V X5R
C519 0.01UF 25V X7R
C153 4.7UF 6.3V X5R
VCC3V3
FPGA 1.8V, FPGA & SYSTEM 3.3V GTP POWER
XILINX
ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
UCD90120A CTLR #2 ADDR 102
Date: 9-20-2012_14:39
Ver: 1.0
Sheet Size: B
Rev: 01
Sheet 45 of 51
Drawn By DN


VCC12_P
L28
FERRITE-78
12V_PWR_IN_TPS84K_VCCO_VADJ
C140 0.1UF 25V X5R
C276 47UF 25V X5R
C284 47UF 25V X5R
C474 22UF 25V X5R
C185 10UF 25V X5R
See TPS84621 datasheet
pg. 23 for PGND-AGND short
Z5
0603_SHORT
GND
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN
VCCO_VADJ
Z41
0201_SHORT
VCCF3V3
C178 0.1UF 25V X5R
37 VCCO_VADJ_SENSE_P
45 VCCO_VADJ_TRIM
R423
2.21K 1%
MARGIN R3
VCCO_VADJ_VADJ
R276 649 1/10W 1%
VCCO_VADJ 2.5V SCALED TO 1.515V
(SCALE FACTOR = 0.606
45 VCCO_VADJ_SCALED_P
R341 1.00K 1/16W 1%
CAN BE PLACED AT CONTROLLER U9
U56
TPS84621RUQ
BQFN_47
AGND1 AGND2 DNC1 DNC2 DNC3 SS_TR STSEL INH_UVLO1 INH_UVLO2 PH1 PH2 PH3 PH4 PH5 DNC4
PGND2 PGND1 RT_CLK AGND3 PWRGD DNC13 DNC12 DNC11 VOUT7 VOUT6 VOUT5 VOUT4 VOUT3 VOUT2 DNC10
VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3
DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9
VCCO_VADJ_PH_ISLAND
45 VCCO_VADJ_EN
SEE FMC VCCO_VADJ VOLTAGE SELECT-->
RTCLK_VCCO_VADJ
VCCO_VADJ_POWER_GOOD
R252 1% 1/10W 10.0K
VCC3V3
VCCO_VADJ_REG_OUT
C141 0.1UF 25V X5R
C260 47UF 25V X5R
C259 47UF 25V X5R
C261 47UF 25V X5R
IDTQS3VH253QG8
U64
SSOP_16
EA_B S1 I3A I2A I1A I0A YA GND
VCC EB_B S0 I3B I2B I1B I0B YB
45 FMC_ADJ_SEL1
FMC_ADJ_SEL0 45
R437 121K 1/10W 1%
R436 200K 1/10W 1%
R253 200K 1/10W 1%
R204 453 1/10W 1%
R435 715 1/10W 1%
R434 316 1/10W 1%
AGND
VCC3V3
R286 261 1/10W
LED-GRN-SMT
DS19
VCCO_VADJ
Q13
NDS331N
R26 4.7K 1/16W
R195
I1 I2 V1 V2
0.005 2W 1%
VCCO_ADJ 2.50V @ 6A MAX
VCCO_VADJ
C256 47UF 25V X5R
C257 47UF 25V X5R
C258 47UF 25V X5R
VCCO_VADJ 0A-3.2A => CS = 0V - 2.001V
G=125.07, Rg=806
R35 806 1/10W 1%
VCC5V0
C143 0.1UF 25V X5R
XADC TAP
35 VCCO_VADJ_XADC_SENSE_N
35 VCCO_VADJ_XADC_SENSE_P
Z42 0201_SHORT
Z43 0201_SHORT
VCCO_VADJ_R_SENSE_N
VCCO_VADJ_R_SENSE_P
RG1 VIN_N VIN_P V_N RG2 V_P VOUT REF
U33 INA333
VCCO_VADJ_CS_P 45

FMC VCCO_VADJ VOLTAGE SELECT

FMC_ADJ_SEL[1	0]	VCCO_ADJ (V)
0	0	2.5V
0	1	1.8V
1	0	3.3V
1	1	3.3V

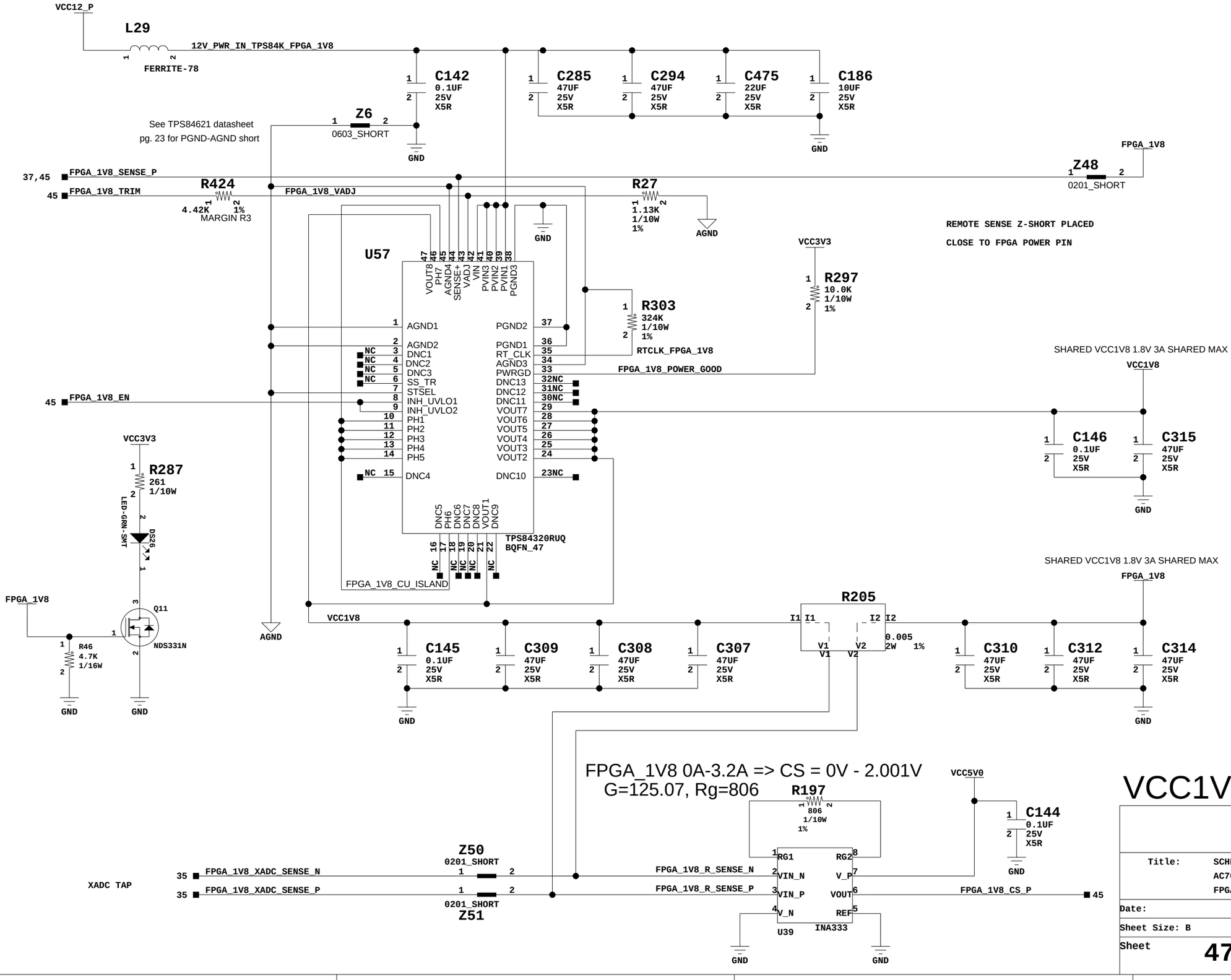
VCCO_VADJ 2.5V

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
VCCO_VADJ REGULATOR

Date: 9-28-2012_8:54 | Ver: 1.0
Sheet Size: B | Rev: 01
Sheet 46 of 51 | Drawn By DN

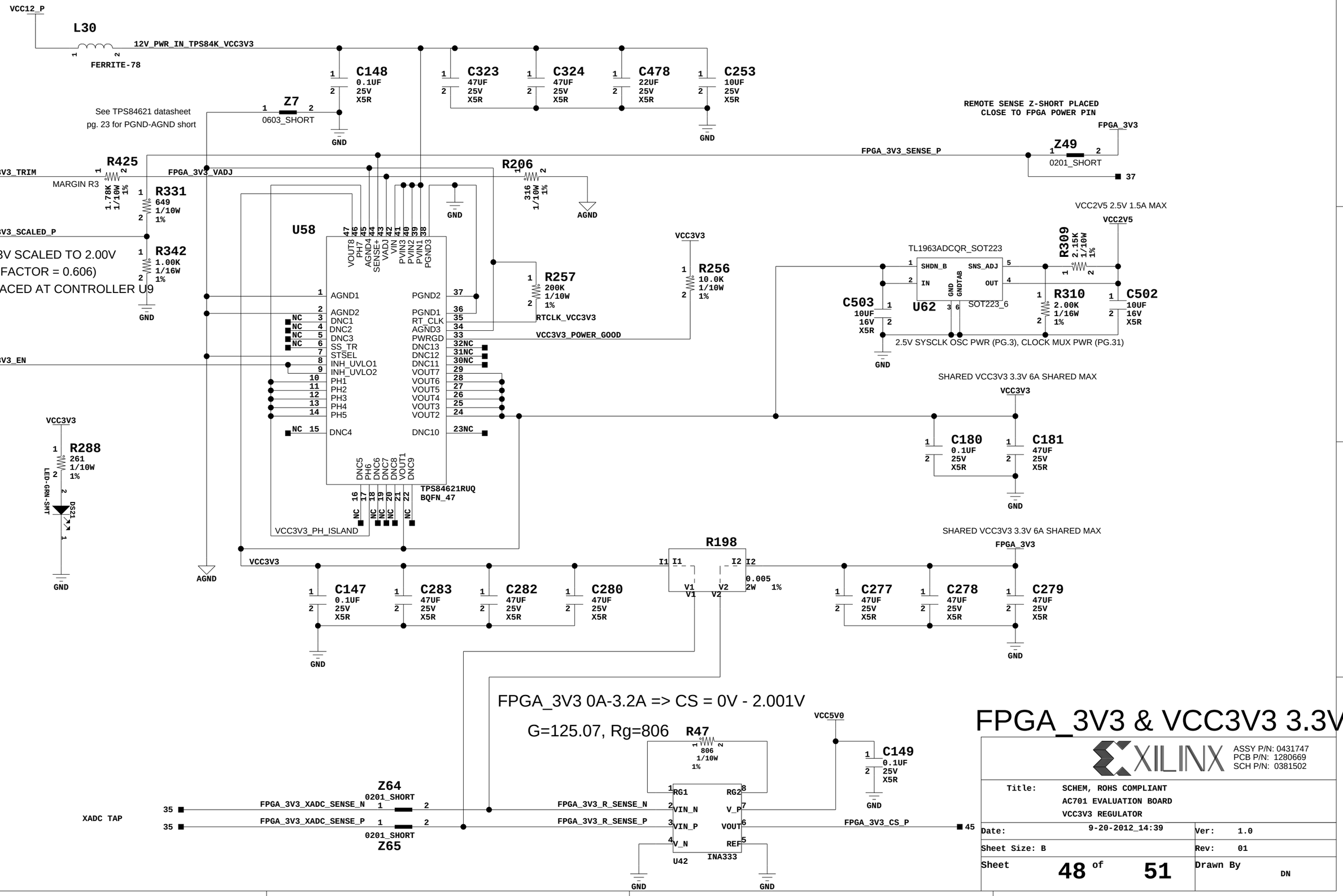


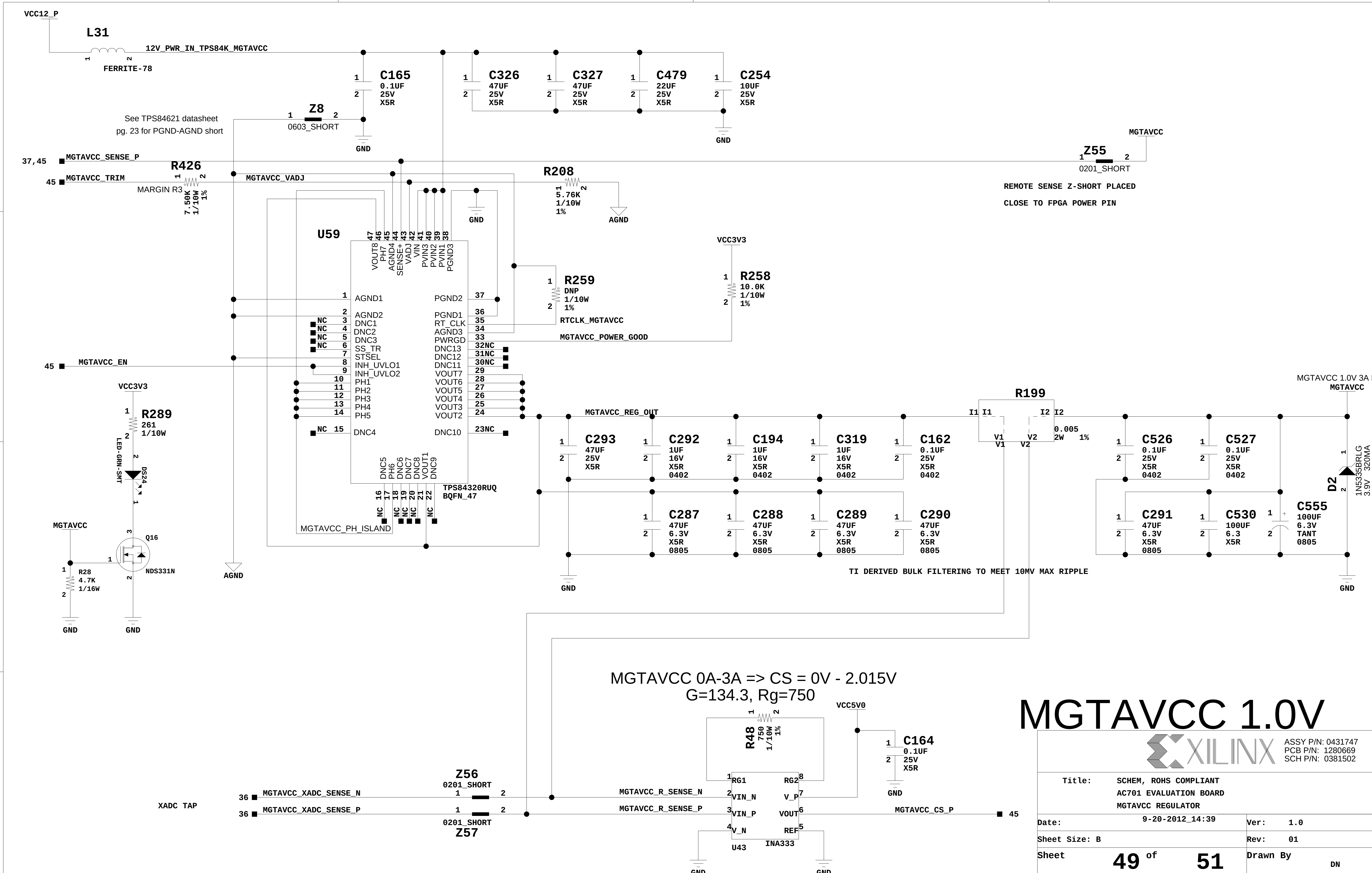
VCC1V8 & FPGA_1V8

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title:	SCHEM, ROHS COMPLIANT AC701 EVALUATION BOARD FPGA_1V8 REGULATOR		
Date:	9-20-2012_14:39	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	47 of 51	Drawn By	DN


VCC12_P
L30
12V_PWR_IN_TPS84K_VCC3V3
FERRITE-78
C148 0.1UF 25V X5R
C323 47UF 25V X5R
C324 47UF 25V X5R
C478 22UF 25V X5R
C253 10UF 25V X5R
GND
See TPS84621 datasheet
pg. 23 for PGND-AGND short
Z7
0603_SHORT
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN
FPGA_3V3
Z49
0201_SHORT
FPGA_3V3_SENSE_P
45 FPGA_3V3_TRIM
MARGIN R3
R425 1.78K 1/10W 1%
R331 649 1/10W 1%
R206 316 1/10W 1%
AGND
FPGA_3V3_VADJ
45 FPGA_3V3_SCALED_P
VCC3V3 3.3V SCALED TO 2.00V
(SCALE FACTOR = 0.606)
CAN BE PLACED AT CONTROLLER U9
R342 1.00K 1/16W 1%
U58
VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3
AGND1 AGND2 DNC1 DNC2 DNC3 SS_TR STSEL INH_UVLO1 INH_UVLO2 PH1 PH2 PH3 PH4 PH5 DNC4
PGND2 PGND1 RT_CLK AGND3 PWRGD DNC13 DNC12 DNC11 VOUT7 VOUT6 VOUT5 VOUT4 VOUT3 VOUT2 DNC10
DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9
TPS84621RUQ
BQFN_47
VCC3V3_PH_ISLAND
R257 200K 1/10W 1%
RTCLK_VCC3V3
VCC3V3_POWER_GOOD
R256 10.0K 1/10W 1%
45 FPGA_3V3_EN
VCC2V5 2.5V 1.5A MAX
VCC2V5
TL1963ADCQR_SOT223
SHDN_B IN GND GNDTAB SNS_ADJ OUT
U62
SOT223_6
R309 2.15K 1/10W 1%
R310 2.00K 1/16W 1%
C503 10UF 16V X5R
C502 10UF 16V X5R
2.5V SYSCLK OSC PWR (PG.3), CLOCK MUX PWR (PG.31)
SHARED VCC3V3 3.3V 6A SHARED MAX
VCC3V3
C180 0.1UF 25V X5R
C181 47UF 25V X5R
R288 261 1/10W 1%
LED-GRN-SMT
DS21
SHARED VCC3V3 3.3V 6A SHARED MAX
FPGA_3V3
R198 0.005 2W 1%
I1 I1 I2 I2 V1 V1 V2 V2
C147 0.1UF 25V X5R
C283 47UF 25V X5R
C282 47UF 25V X5R
C280 47UF 25V X5R
C277 47UF 25V X5R
C278 47UF 25V X5R
C279 47UF 25V X5R
FPGA_3V3 0A-3.2A => CS = 0V - 2.001V
G=125.07, Rg=806
R47 806 1/10W 1%
VCC5V0
C149 0.1UF 25V X5R
XADC TAP
Z64
0201_SHORT
FPGA_3V3_XADC_SENSE_N
Z65
0201_SHORT
FPGA_3V3_XADC_SENSE_P
FPGA_3V3_R_SENSE_N
FPGA_3V3_R_SENSE_P
RG1 RG2 VIN_N V_P VIN_P VOUT V_N REF
U42
INA333
FPGA_3V3_CS_P
45
FPGA_3V3 & VCC3V3 3.3V
XILINX
ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502
Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
VCC3V3 REGULATOR
Date: 9-20-2012_14:39
Ver: 1.0
Sheet Size: B
Rev: 01
Sheet 48 of 51
Drawn By DN


VCC12_P
L31
FERRITE-78
12V_PWR_IN_TPS84K_MGTAVCC
C165 0.1UF 25V X5R
C326 47UF 25V X5R
C327 47UF 25V X5R
C479 22UF 25V X5R
C254 10UF 25V X5R
See TPS84621 datasheet
pg. 23 for PGND-AGND short
Z8 0603_SHORT
GND
37,45 MGTAVCC_SENSE_P
45 MGTAVCC_TRIM
R426 MARGIN R3 7.50K 1/10W 1%
MGTAVCC_VADJ
R208 5.76K 1/10W 1%
AGND
Z55 0201_SHORT
MGTAVCC
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN
U59
VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3
AGND1 AGND2 DNC1 DNC2 DNC3 SS_TR STSEL INH_UVLO1 INH_UVLO2 PH1 PH2 PH3 PH4 PH5 DNC4
PGND2 PGND1 RT_CLK AGND3 PWRGD DNC13 DNC12 DNC11 VOUT7 VOUT6 VOUT5 VOUT4 VOUT3 VOUT2 DNC10
DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9
TPS84320RUQ
BQFN_47
MGTAVCC_PH_ISLAND
VCC3V3
R259 DNP 1/10W 1%
RTCLK_MGTAVCC
R258 10.0K 1/10W 1%
MGTAVCC_POWER_GOOD
45 MGTAVCC_EN
R289 261 1/10W
LED-GRN-SMT
DS24
Q16 NDS331N
R28 4.7K 1/16W
MGTAVCC_REG_OUT
R199 0.005 2W 1%
MGTAVCC 1.0V 3A MAX
C293 47UF 25V X5R
C292 1UF 16V X5R 0402
C194 1UF 16V X5R 0402
C319 1UF 16V X5R 0402
C162 0.1UF 25V X5R 0402
C287 47UF 6.3V X5R 0805
C288 47UF 6.3V X5R 0805
C289 47UF 6.3V X5R 0805
C290 47UF 6.3V X5R 0805
C526 0.1UF 25V X5R 0402
C527 0.1UF 25V X5R 0402
C291 47UF 6.3V X5R 0805
C530 100UF 6.3 X5R
C555 100UF 6.3V TANT 0805
D2 1N5335BRLG 3.9V 320MA
TI DERIVED BULK FILTERING TO MEET 10MV MAX RIPPLE
MGTAVCC 0A-3A => CS = 0V - 2.015V
G=134.3, Rg=750
VCC5V0
R48 750 1/10W 1%
C164 0.1UF 25V X5R
U43 INA333
RG1 RG2 VIN_N V_P VIN_P VOUT V_N REF
XADC TAP
36 MGTAVCC_XADC_SENSE_N
36 MGTAVCC_XADC_SENSE_P
Z56 0201_SHORT
Z57 0201_SHORT
MGTAVCC_R_SENSE_N
MGTAVCC_R_SENSE_P
MGTAVCC_CS_P 45

MGTAVCC 1.0V

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
MGTAVCC REGULATOR

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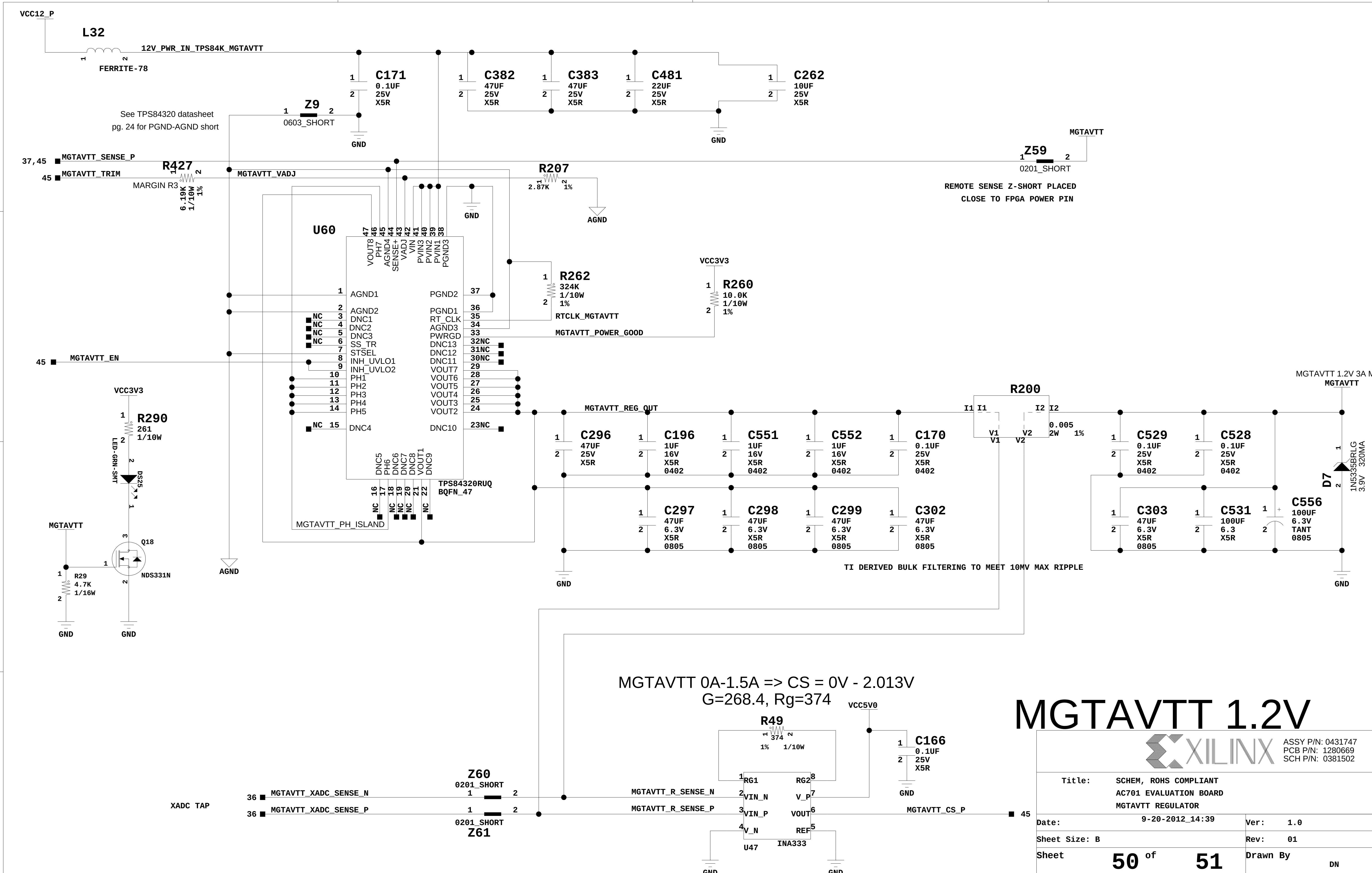
 | Drawn By DN


VCC12_P
L32
FERRITE-78
12V_PWR_IN_TPS84K_MGTAVTT
C171 0.1UF 25V X5R
C382 47UF 25V X5R
C383 47UF 25V X5R
C481 22UF 25V X5R
C262 10UF 25V X5R
See TPS84320 datasheet
pg. 24 for PGND-AGND short
Z9 0603_SHORT
GND
MGTAVTT
Z59 0201_SHORT
37,45 MGTAVTT_SENSE_P
45 MGTAVTT_TRIM
R427 MARGIN R3 6.19K 1/10W 1%
MGTAVTT_VADJ
R207 2.87K 1%
AGND
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN
U60
VOUT8 PH7 AGND4 SENSE+ VADJ VIN PVIN3 PVIN2 PVIN1 PGND3
AGND1 AGND2 DNC1 DNC2 DNC3 SS_TR STSEL INH_UVLO1 INH_UVLO2 PH1 PH2 PH3 PH4 PH5 DNC4
PGND2 PGND1 RT_CLK AGND3 PWRGD DNC13 DNC12 DNC11 VOUT7 VOUT6 VOUT5 VOUT4 VOUT3 VOUT2 DNC10
DNC5 PH6 DNC6 DNC7 DNC8 VOUT1 DNC9
TPS84320RUQ
BQFN_47
MGTAVTT_PH_ISLAND
R262 324K 1/10W 1%
RTCLK_MGTAVTT
VCC3V3
R260 10.0K 1/10W 1%
MGTAVTT_POWER_GOOD
45 MGTAVTT_EN
VCC3V3
R290 261 1/10W
LED-GRN-SMT DS25
MGTAVTT
Q18 NDS331N
R29 4.7K 1/16W
MGTAVTT_REG_OUT
R200 0.005 2W 1%
MGTAVTT 1.2V 3A MAX
MGTAVTT
C296 47UF 25V X5R
C196 1UF 16V X5R 0402
C551 1UF 16V X5R 0402
C552 1UF 16V X5R 0402
C170 0.1UF 25V X5R 0402
C529 0.1UF 25V X5R 0402
C528 0.1UF 25V X5R 0402
D7 1N5335BRLG 3.9V 320MA
C297 47UF 6.3V X5R 0805
C298 47UF 6.3V X5R 0805
C299 47UF 6.3V X5R 0805
C302 47UF 6.3V X5R 0805
C303 47UF 6.3V X5R 0805
C531 100UF 6.3 X5R
C556 100UF 6.3V TANT 0805
TI DERIVED BULK FILTERING TO MEET 10MV MAX RIPPLE
MGTAVTT 0A-1.5A => CS = 0V - 2.013V
G=268.4, Rg=374
VCC5V0
R49 374 1% 1/10W
C166 0.1UF 25V X5R
Z60 0201_SHORT
Z61 0201_SHORT
XADC TAP
36 MGTAVTT_XADC_SENSE_N
36 MGTAVTT_XADC_SENSE_P
MGTAVTT_R_SENSE_N
MGTAVTT_R_SENSE_P
RG1 VIN_N VIN_P V_N RG2 V_P VOUT REF
U47 INA333
MGTAVTT_CS_P 45

MGTAVTT 1.2V

XILINX

ASSY P/N: 0431747
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Title: SCHEM, ROHS COMPLIANT
AC701 EVALUATION BOARD
MGTAVTT REGULATOR

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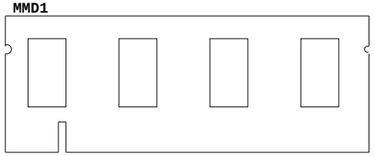
MMD1



DDR3_SODIMM

CBL1

4-Pin ATX Power — 6-Pin Molex Mini-fit Jr.

PCIe Adapter Cable

PCIE_ADAPTER_CABLE

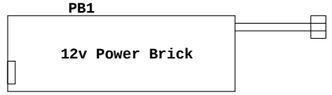
CBL2

110V Prong — IEC320-C13

Power Cord

PC_POWER_CABLE

PB1



PWR_BRICK_12V

CBL3

USB A — USB Mini-B

USB Mini-B Cable

USB_MINIB_CABLE

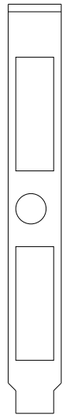
CBL4

USB A — USB Mini-B

USB Micro-B Cable

USB_MICRO_CABLE

PL1



AC701_PCIE_PLATE

MANF=PURCELL
MANF_P/N=P1155-0003

MSTK1

PCIE_POWER_STICKER

MJB1 JUMPER_BLOCK_2-PIN
MJB2 JUMPER_BLOCK_2-PIN
MJB3 JUMPER_BLOCK_2-PIN
MJB4 JUMPER_BLOCK_2-PIN
MJB5 JUMPER_BLOCK_2-PIN
MJB6 JUMPER_BLOCK_2-PIN
MJB7 JUMPER_BLOCK_2-PIN
MJB8 JUMPER_BLOCK_2-PIN
MJB9 JUMPER_BLOCK_2-PIN
MJB10 JUMPER_BLOCK_2-PIN
MJB11 JUMPER_BLOCK_2-PIN
MJB12 JUMPER_BLOCK_2-PIN
MJB13 JUMPER_BLOCK_2-PIN
MJB14 JUMPER_BLOCK_2-PIN
MJB15 JUMPER_BLOCK_2-PIN

MS1 MACHINE_SCREW_4-40
MS01 STANDOFF_0P375
MRB1 RUBBER_BUMPER
MS13 MACHINE_SCREW_4-40
MH_125_250 — MH1 — GND

MS2 MACHINE_SCREW_4-40
MS02 STANDOFF_0P375
MRB2 RUBBER_BUMPER
MS14 MACHINE_SCREW_4-40
MH_125_250 — MH2 — GND

MS3 MACHINE_SCREW_4-40
MS03 STANDOFF_0P375
MRB3 RUBBER_BUMPER
MS15 MACHINE_SCREW_4-40
MH_125_250 — MH3 — GND

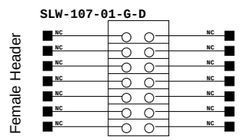
MS4 MACHINE_SCREW_4-40
MS04 STANDOFF_0P375
MRB4 RUBBER_BUMPER
MS16 MACHINE_SCREW_4-40
MH_125_250 — MH4 — GND

MS5 MACHINE_SCREW_4-40
MS05 STANDOFF_0P375
MRB5 RUBBER_BUMPER
MS17 MACHINE_SCREW_4-40
MH_125_250 — MH5 — GND

MS6 MACHINE_SCREW_4-40
MS06 STANDOFF_0P375
MRB6 RUBBER_BUMPER
MS18 MACHINE_SCREW_4-40
MH_125_250 — MH6 — GND

LCD Display Assembly

SLW-107-01-G-D — Female Header — LCD1_J11



LCD Display — LCD_DISPLAY_16X2 — LCD1

LCD Mounting HW

STANDOFF_10MM — MS09
MACHINE_SCREW_M2_5 — MS12
MACHINE_SCREW_M2_5 — MS9
MH_110_135 — MH9 — GND

STANDOFF_10MM — MS07
MACHINE_SCREW_M2_5 — MS7
MACHINE_SCREW_M2_5 — MS10
MH_110_135 — MH7 — GND

STANDOFF_10MM — MS08
MACHINE_SCREW_M2_5 — MS8
MACHINE_SCREW_M2_5 — MS11
MH_110_135 — MH8 — GND

Mechanical Components

XILINX

ASSY P/N: 0431747
PCB P/N: 1280669
SCH P/N: 0381502

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