# SP605 PCIe x1 Gen1 Design Creation

March 2012



XTP065

# Revision History

| Date | Version | Description |
|---|---|---|
| 03/16/12 | 13.4 | Recompiled under 13.4. |
| 10/26/11 | 13.3 | Recompiled under 13.3. |
| 07/06/11 | 13.2 | Recompiled under 13.2. |
| 03/01/11 | 13.1 | Recompiled under 13.1. |
| 12/21/10 | 12.4 | Recompiled under 12.4. |
| 10/05/10 | 12.3 | Recompiled under 12.3. |
| 07/23/10 | 12.2 | Recompiled under 12.2. |

# Overview

- Spartan-6 PCIe x1 Gen1 Capability
- Xilinx SP605 Board
- Software Requirements
- Generate PCIe Core
- Compile PCIe Core
- Program SPI Flash with PCIe Design
- SP605 Setup
- Running the PCIe x1 Gen1 Design
- References
  - IP Release Notes Guide XTP025

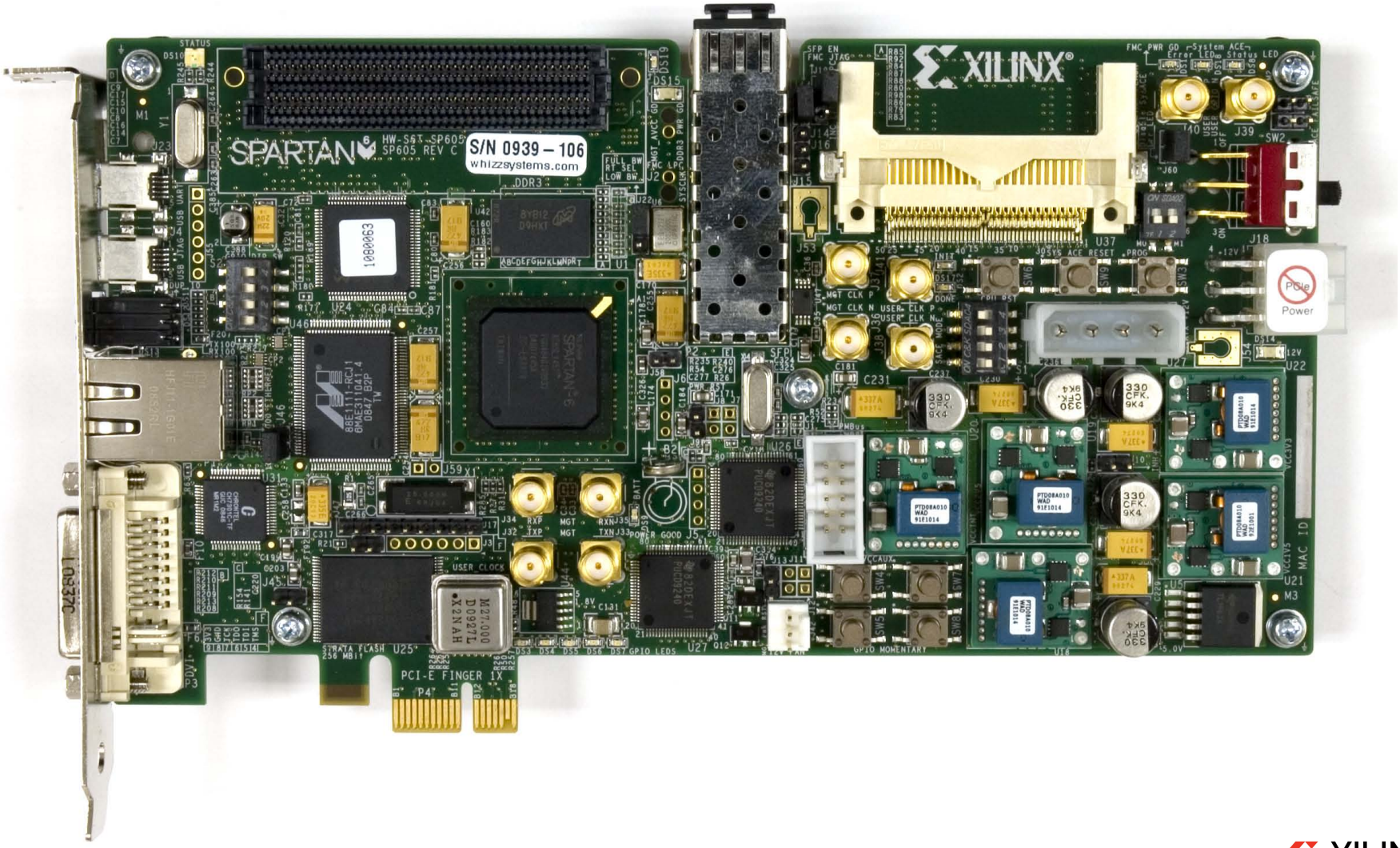
**Note:** This presentation applies to the SP605

# Spartan-6 PCIe x1 Gen1 Capability

- **Integrated Block for PCI Express**
  - PCI Express Base 1.1 Specification
- **Generation 1 (2.5 Gb/s) data rates**
  - x1 Gen1 lane width
- **Configurable for Endpoint**
  - SP605 configured for Endpoint Applications
- **GTP Transceivers implement a fully compliant PHY**
- **Large range of maximum payload size**
  - 128 / 256 / 512 bytes
- **Configurable BAR spaces**
  - Up to 6 x 32 bit, 3 x 64 bit, or a combination
  - Memory or IO
  - BAR and ID filtering

**Note:** Presentation applies to the SP605

# Xilinx SP605 Board




**Note:** Presentation applies to the SP605

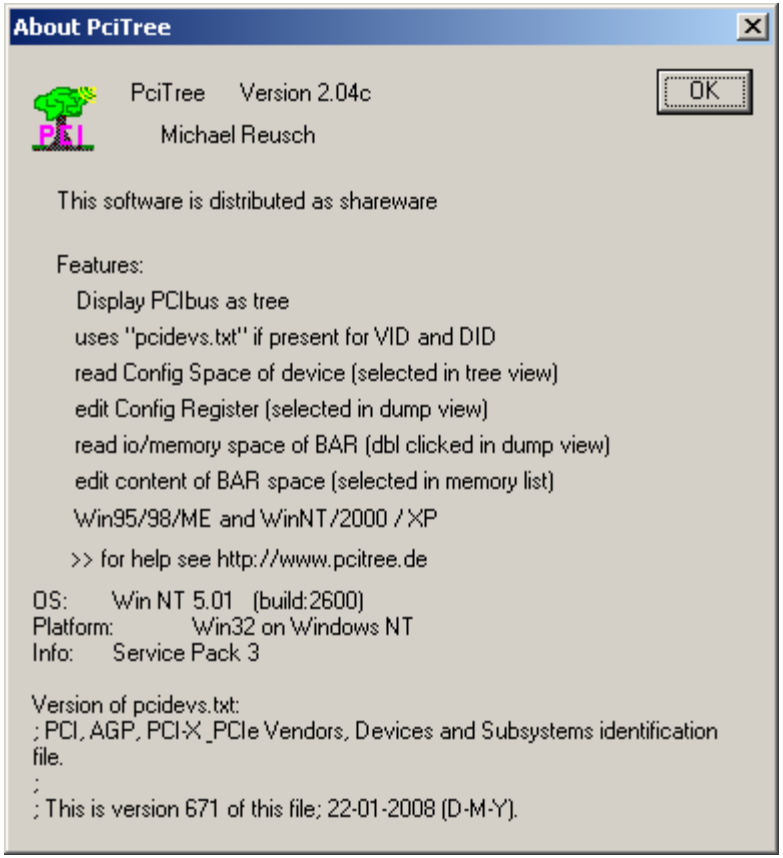
# ISE Software Requirement

- **Xilinx ISE 13.4 software**


**Note:** Presentation applies to the SP605

# PciTree Software Requirement

- **PciTree Bus Viewer**
  - Free download
  - HLP.SYS must be copied to C:\WINDOWS\system32\drivers directory



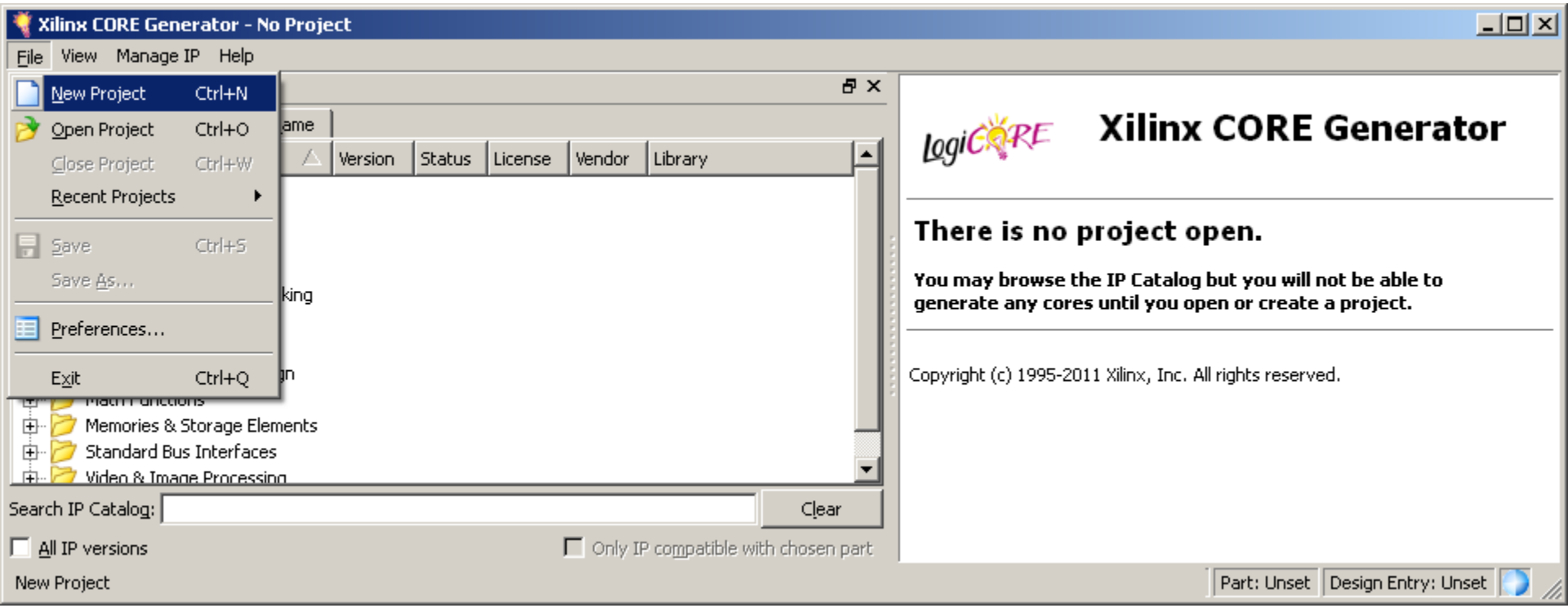

**Note:** Presentation applies to the SP605

# Generate PCIe Core

- **Open the CORE Generator**

  **Start → All Programs → Xilinx ISE Design Suite 13.4 → ISE Design Tools → Tools → CORE Generator**

- **Create a new project; select File → New Project**




**Note:** Presentation applies to the SP605

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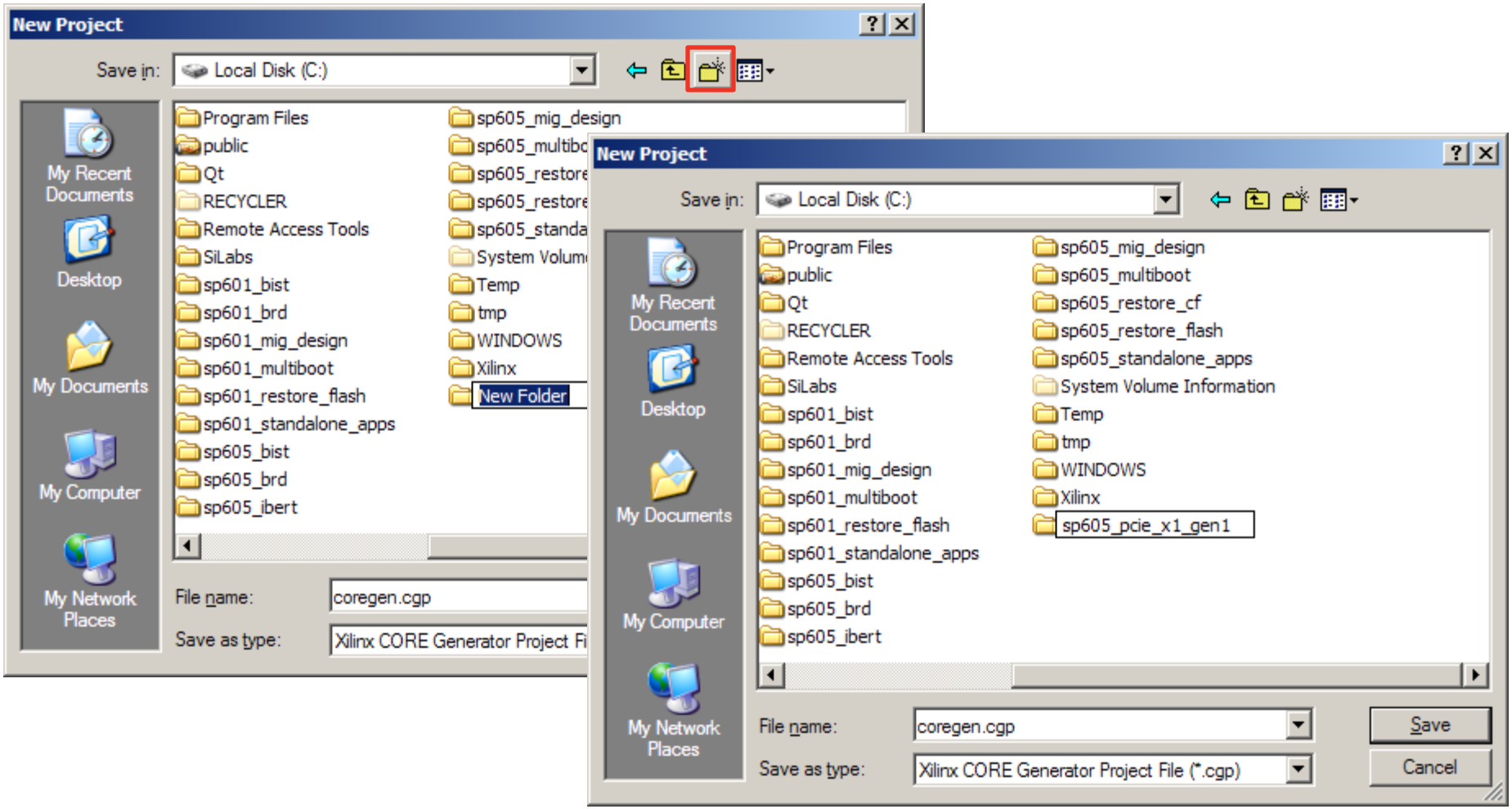
# Generate MIG Example Design

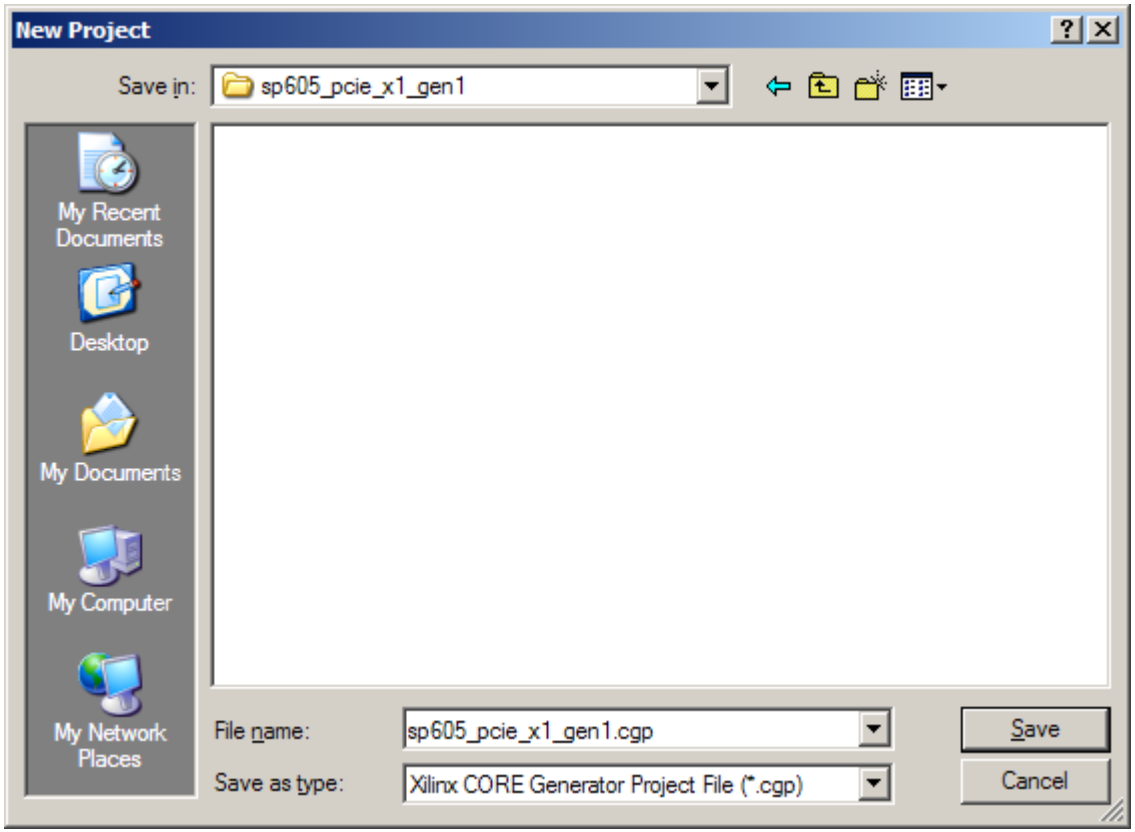
- **Create a project directory: sp605_pcie_x1_gen1**




**Note:** Presentation applies to the SP605

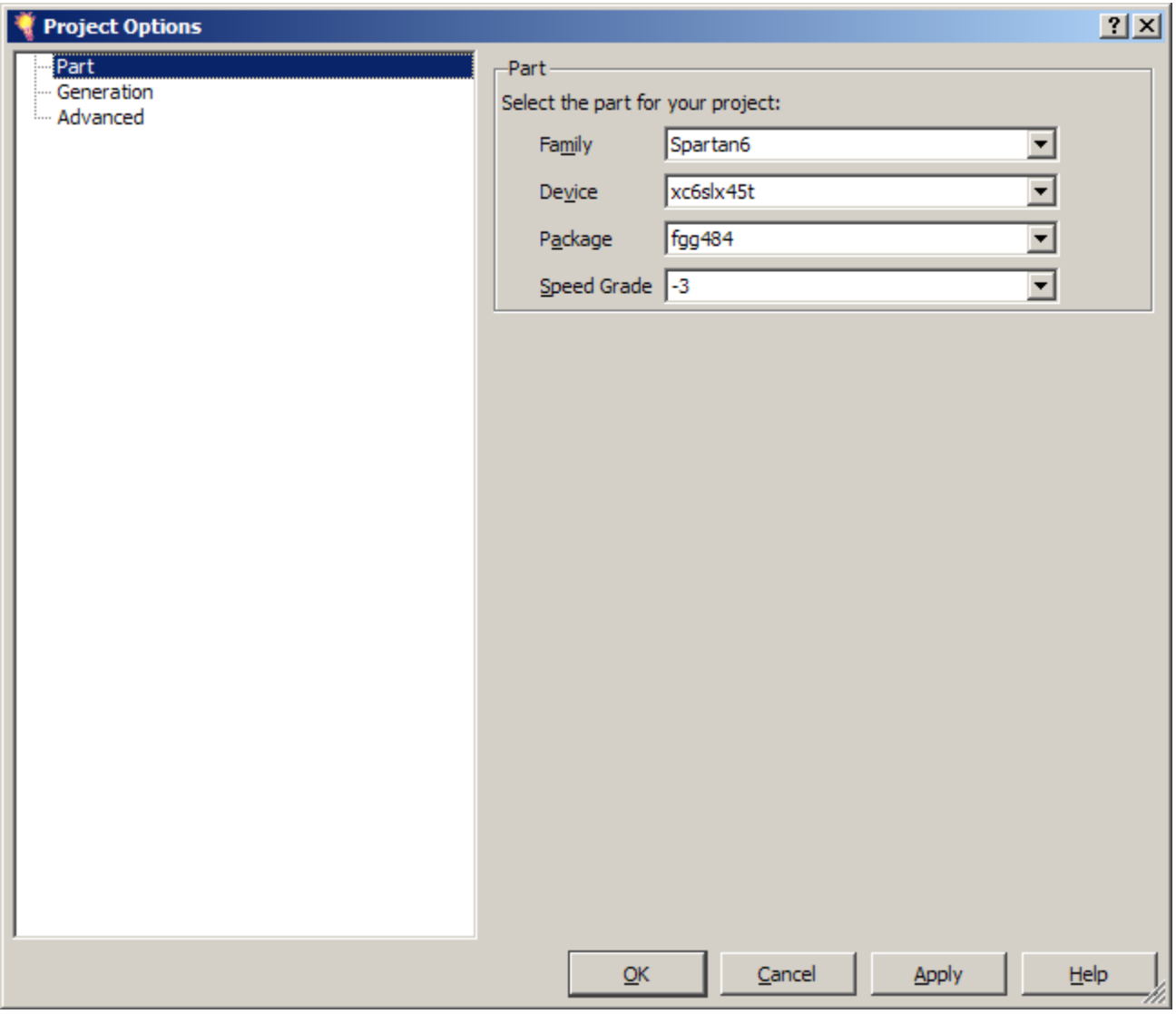
# Generate MIG Example Design

- **Name the project: sp605_pcie_x1_gen1.cgp**




**Note:** Presentation applies to the SP605

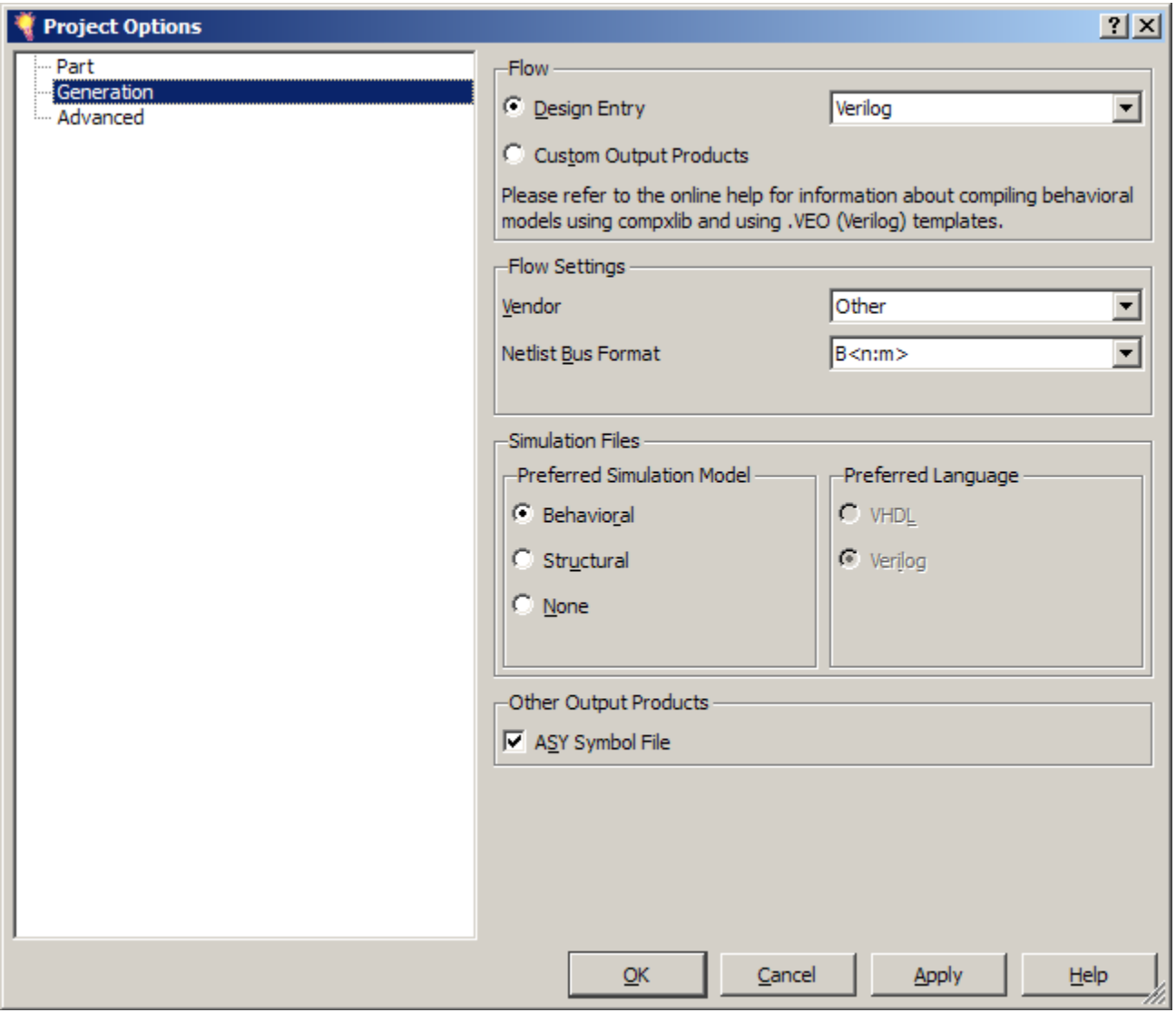
# Generate PCIe Core




- **The Project options will appear**
- **Set the Part (as seen here):**
  - Family: Spartan6
  - Device: xc6slx45t
  - Package: fgg484
  - Speed Grade: -3
- **Select Generation**

**Note:** Presentation applies to the SP605

# Generate PCIe Core

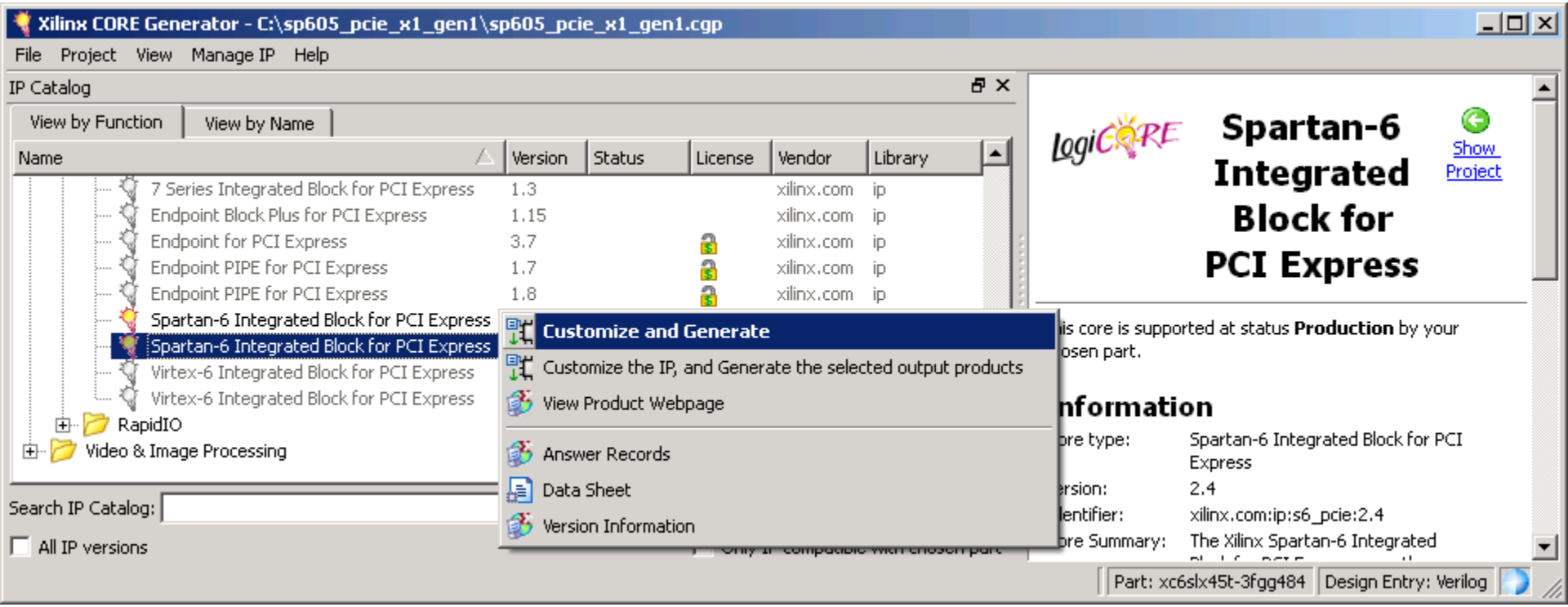



- **Under Generation**
  - Set the Design Entry to Verilog
- **Click OK**

**Note:** Presentation applies to the SP605

# Generate PCIe Core

- **Right click on the Spartan-6 Integrated Block for PCI Express, Version 2.4**
  - Select **Customize and Generate**




**Note:** Presentation applies to the SP605

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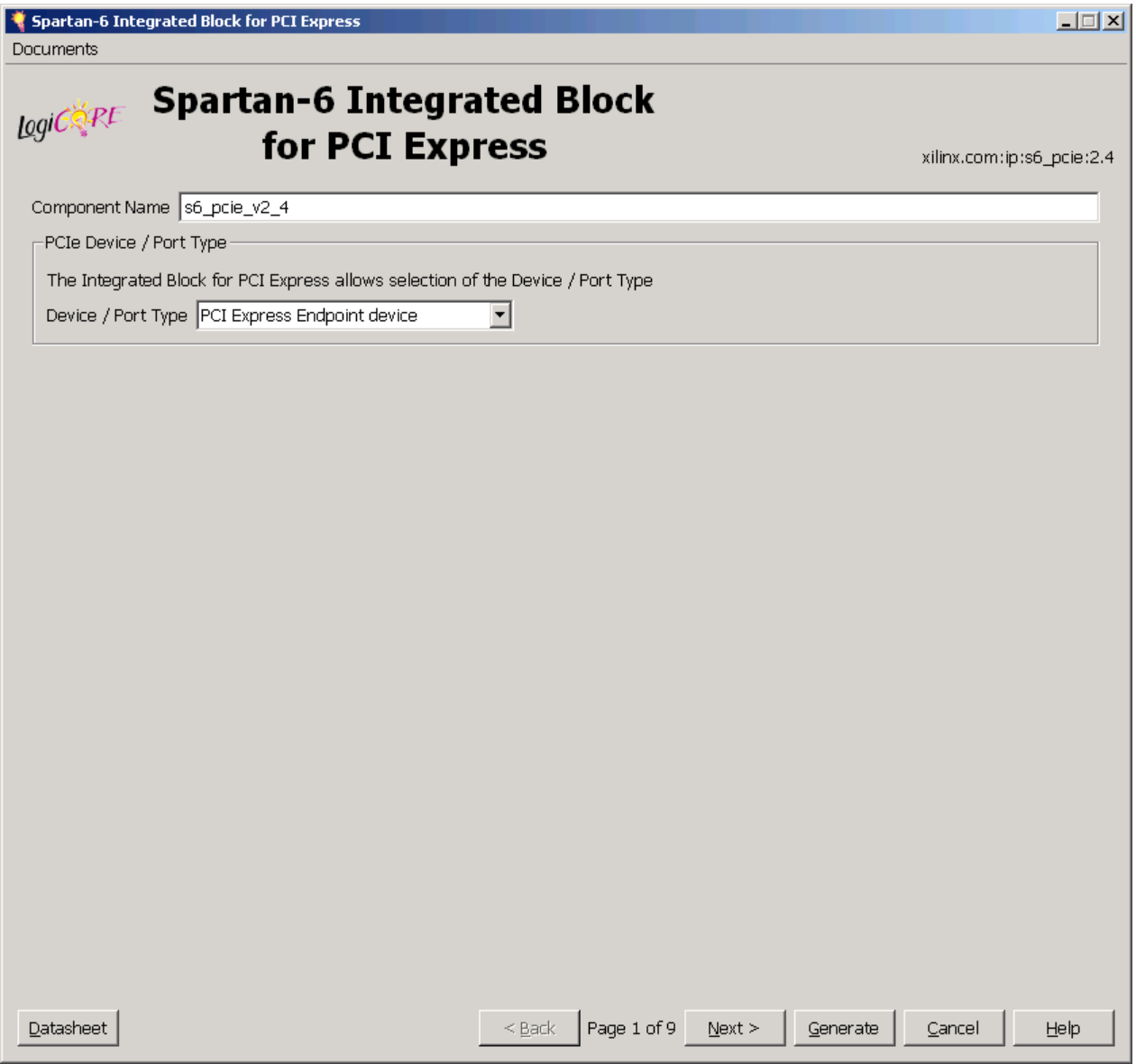
# Generate PCIe Core




- Click Next

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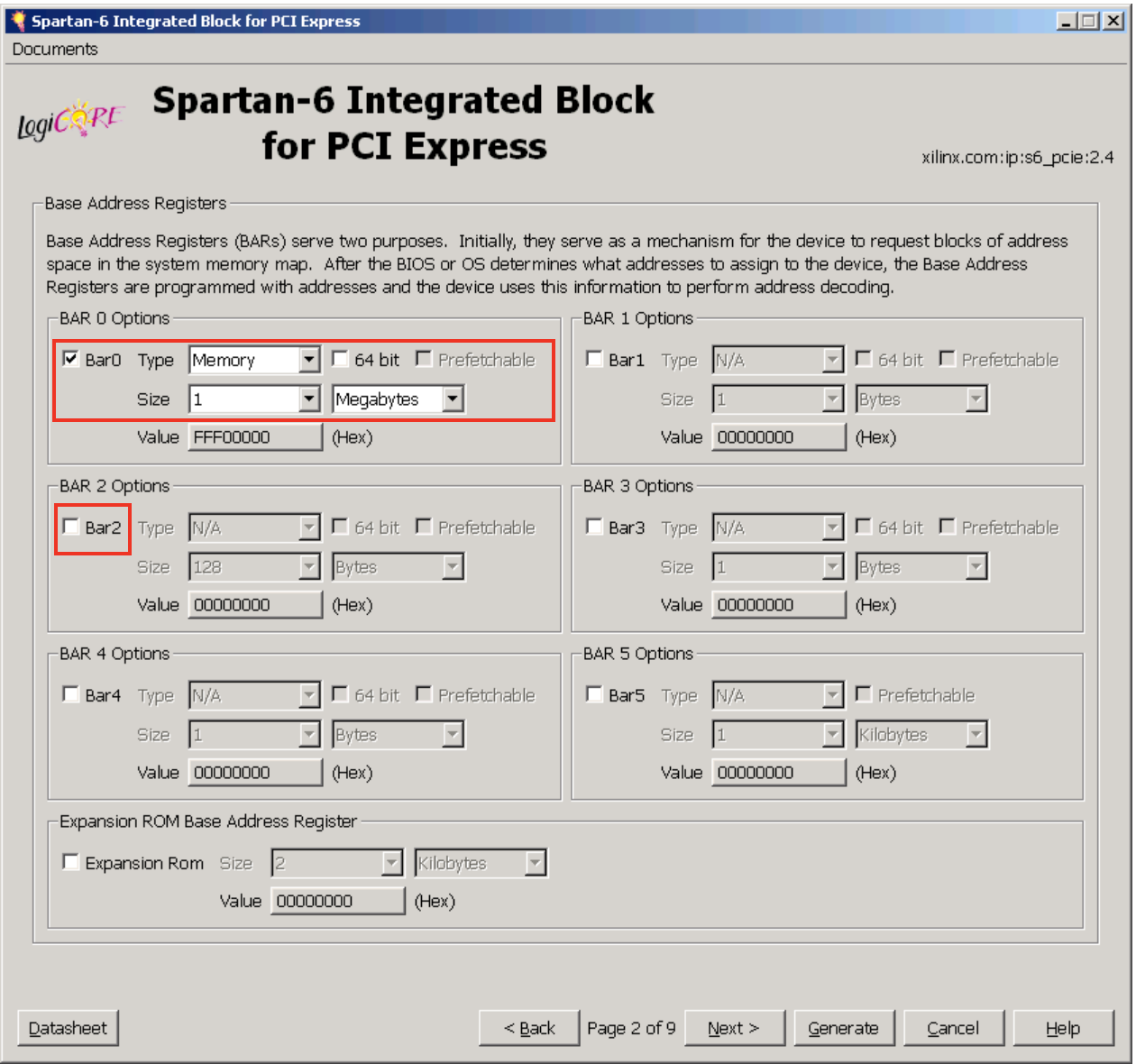
# Generate PCIe Core




- **BAR 0**
  - Set to 1 Megabytes
- **BAR 2**
  - Deselect BAR 2
- **Click Next**

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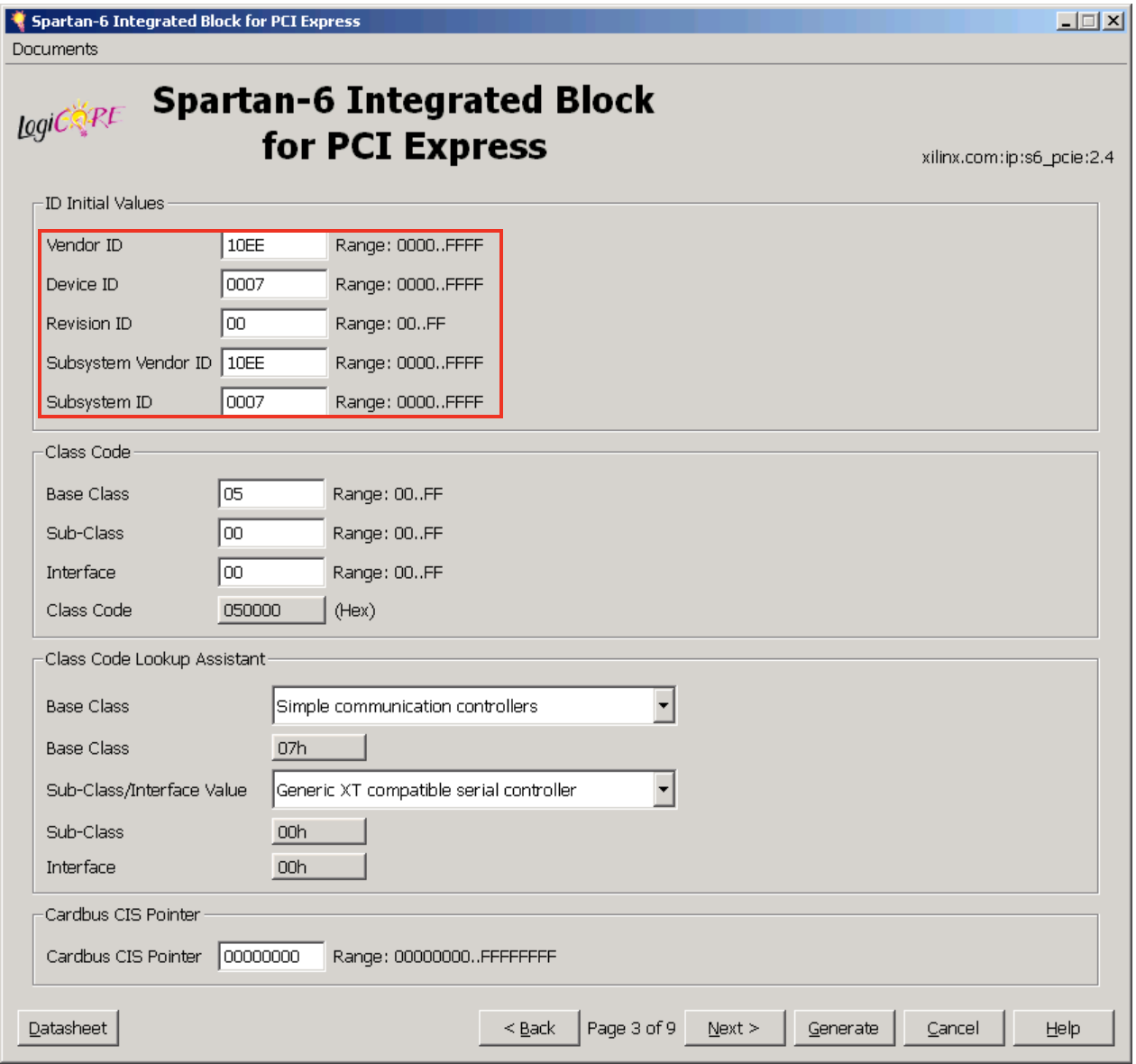
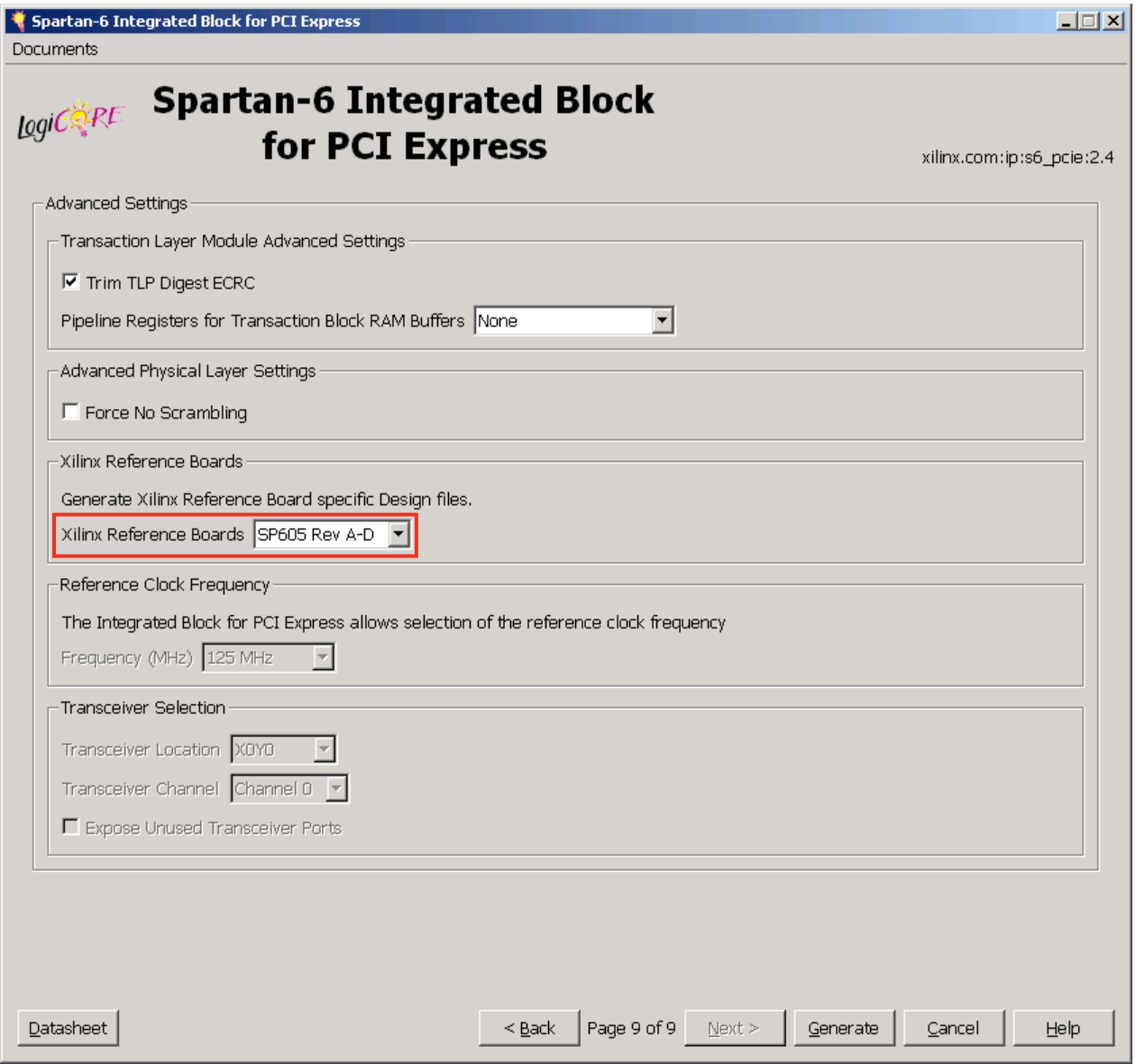
# Generate PCIe Core




- **Note ID Initial Values**
  - Vendor ID = **10EE**
  - Device ID = **0007**
  - Revision ID = **00**
  - Subsystem Vendor ID = **10EE**
  - Subsystem ID = **0007**
- **Click Next 6 times**

# Generate PCIe Core




- **On Page 9**
  - Select SP605
- **Click Generate**

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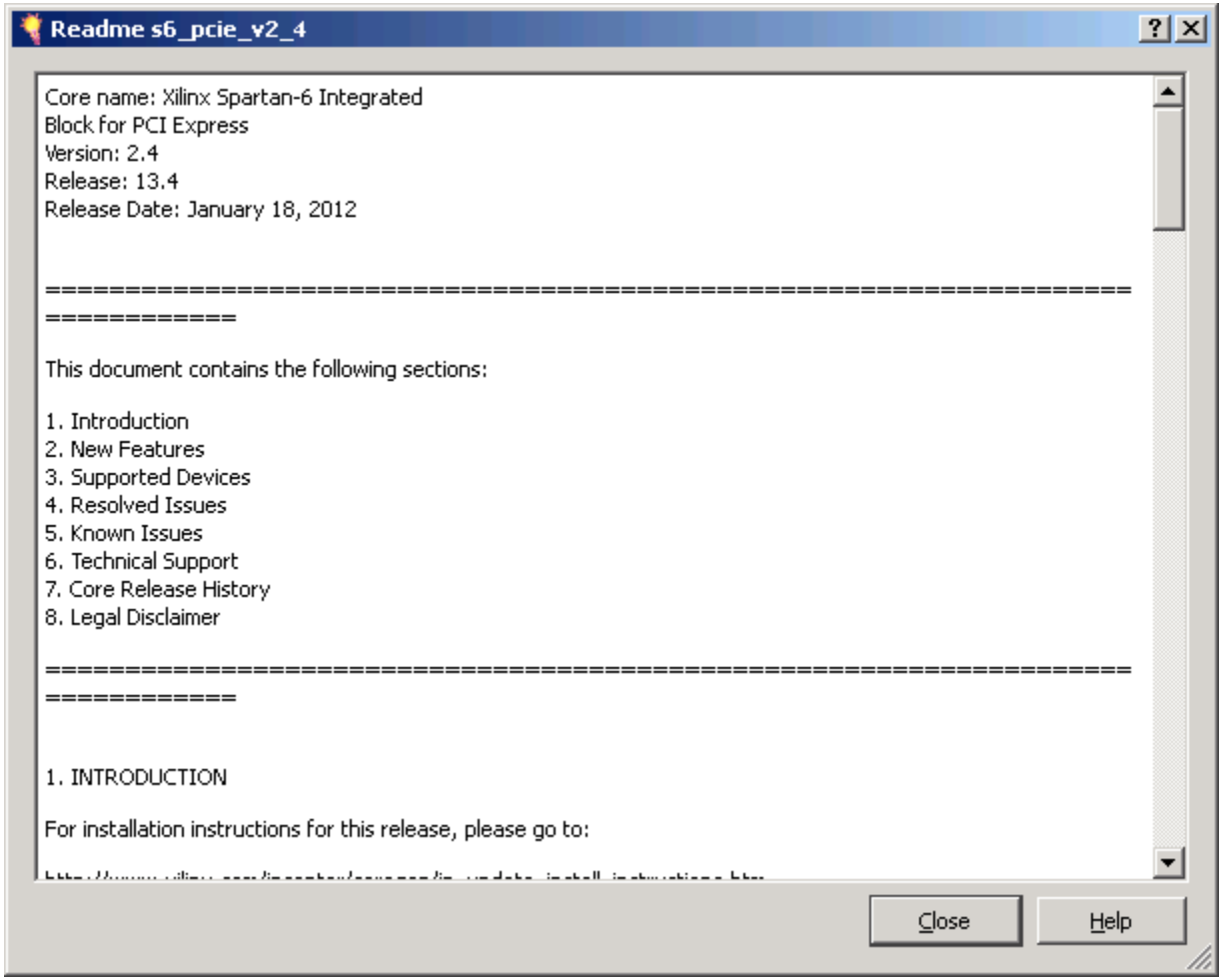
# Generate PCIe Core

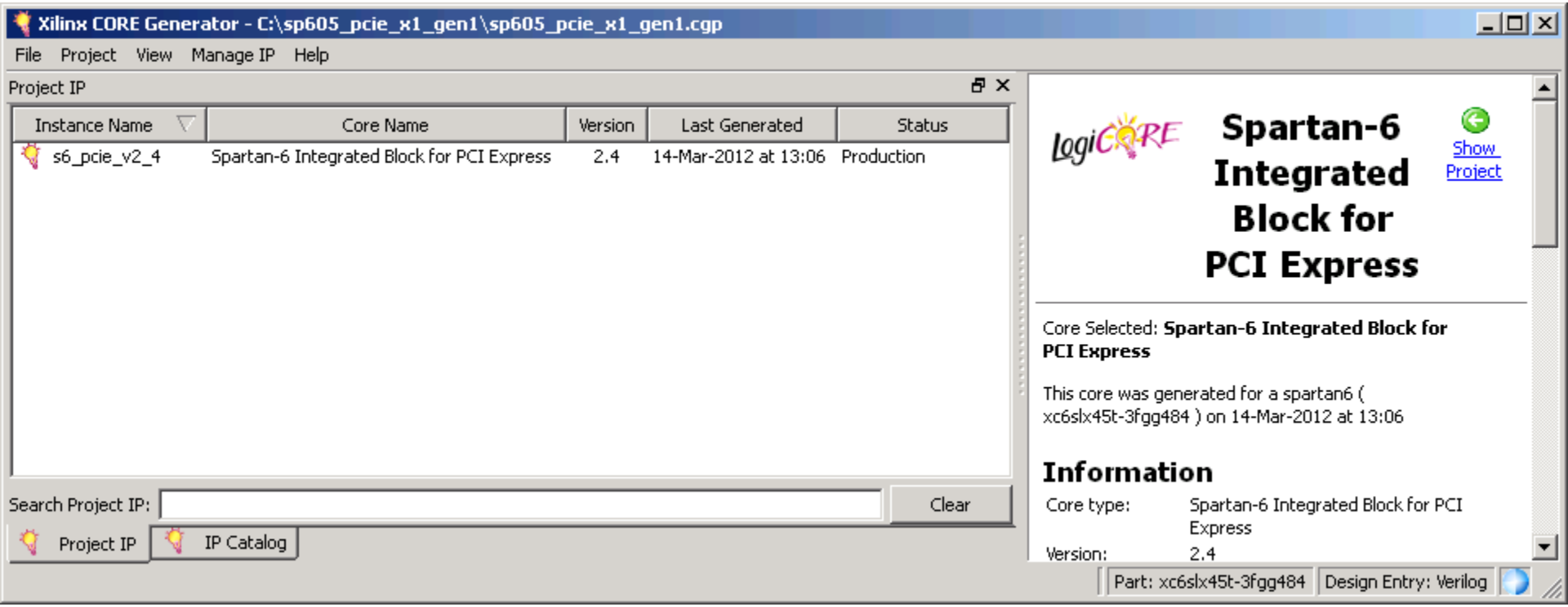
- After the PCIe core finishes generating, click OK on the Readme File window




**Note:** Presentation applies to the SP605

# Generate PCIe Core

- The s6_pcie_v2_4 IP appears under the Project IP tab



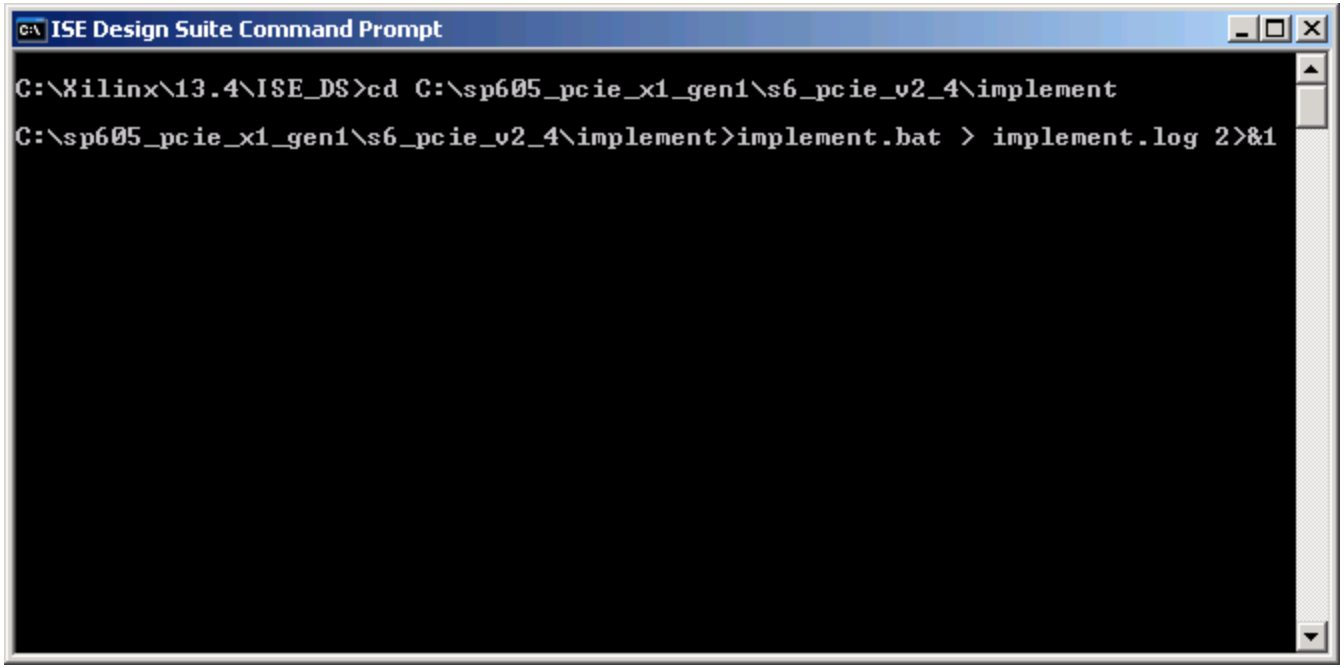

**Note:** Presentation applies to the SP605

# Compile PCIe Core

- **Type these commands in an ISE Design Suite Command Prompt:**

  **cd C:\sp605_pcie_x1_gen1\s6_pcie_v2_4\implement**

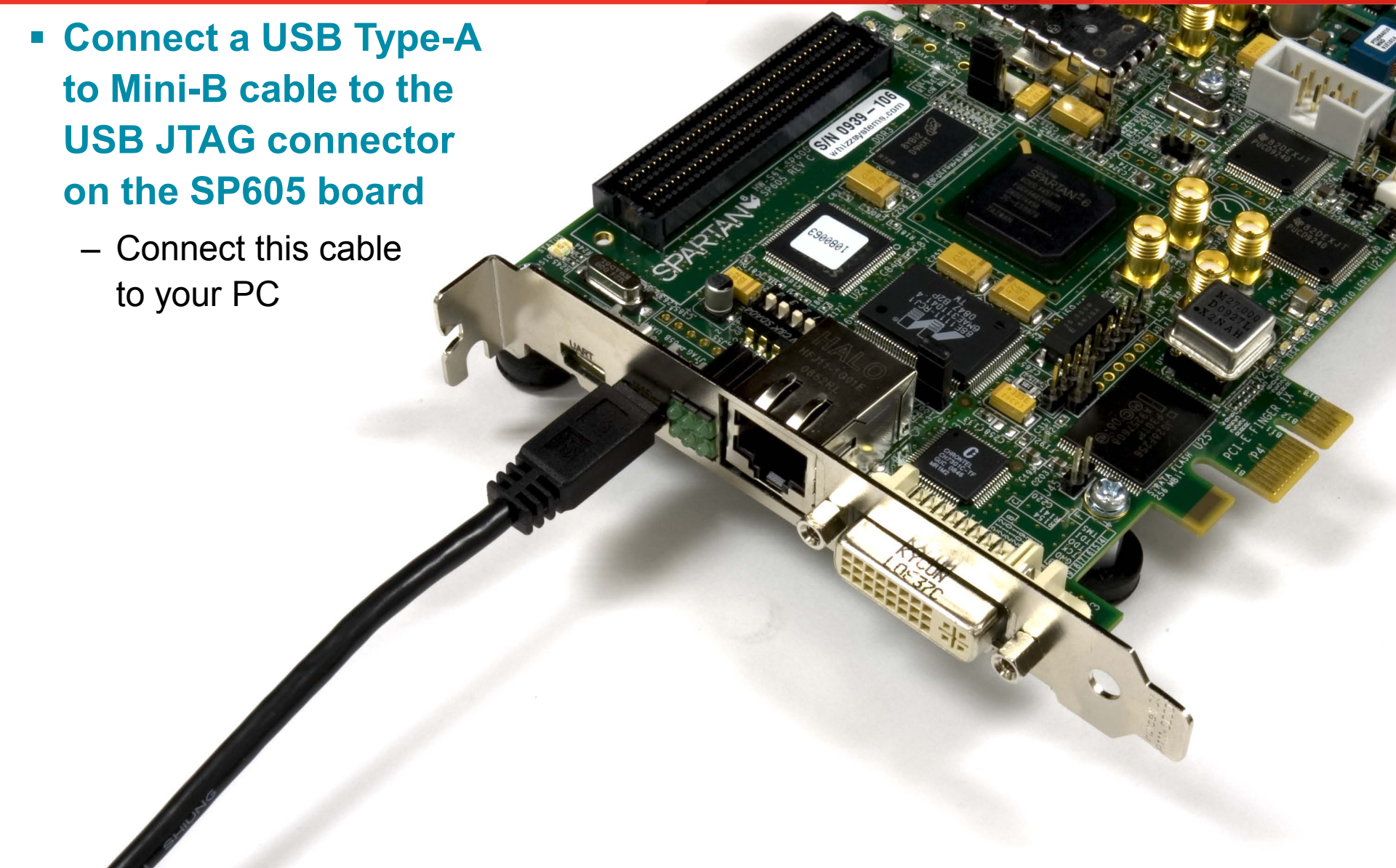
  **implement.bat > implement.log 2>&1**




**Note:** Presentation applies to the SP605

# Program SPI Flash with PCIe Design

- **Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the SP605 board**
  - Connect this cable to your PC



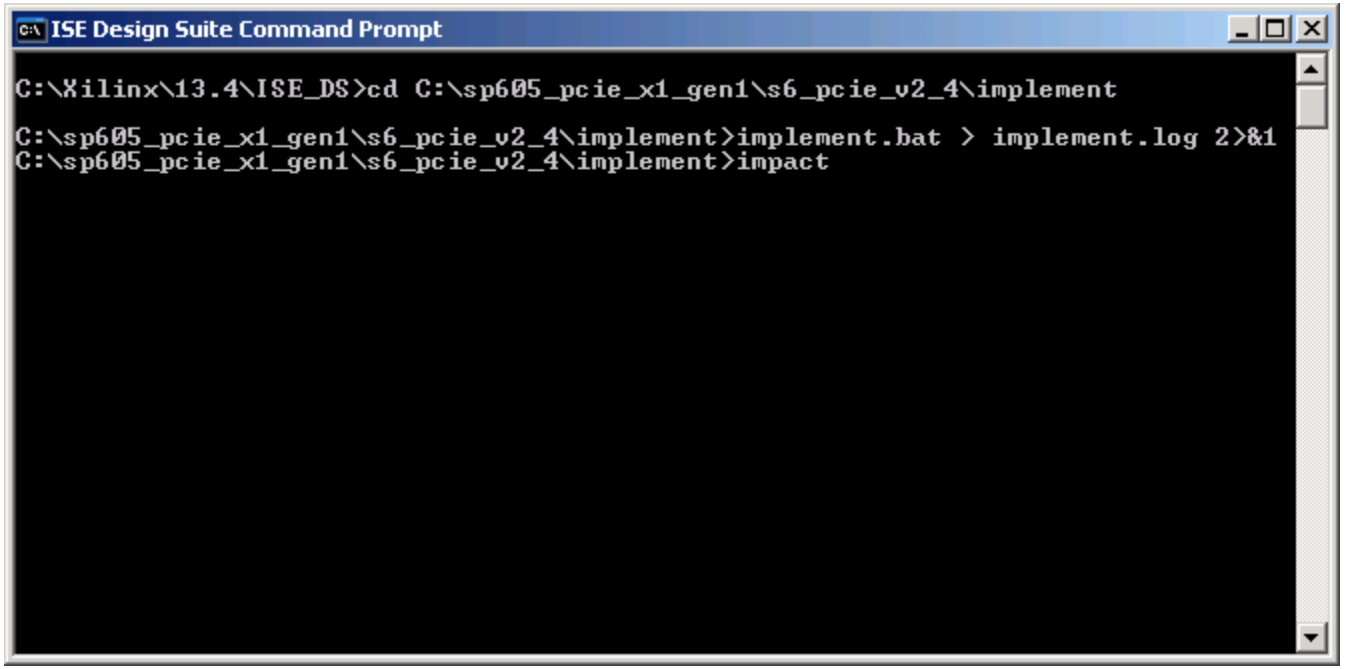
# Program SPI Flash with PCIe Design


- **Set the mode pins for SPI x4 Flash**
  - M0 = 1
  - M1 = 0
  - Set S1 to 0000

# Program SPI Flash with PCIe Design

- **Run iMPACT:**

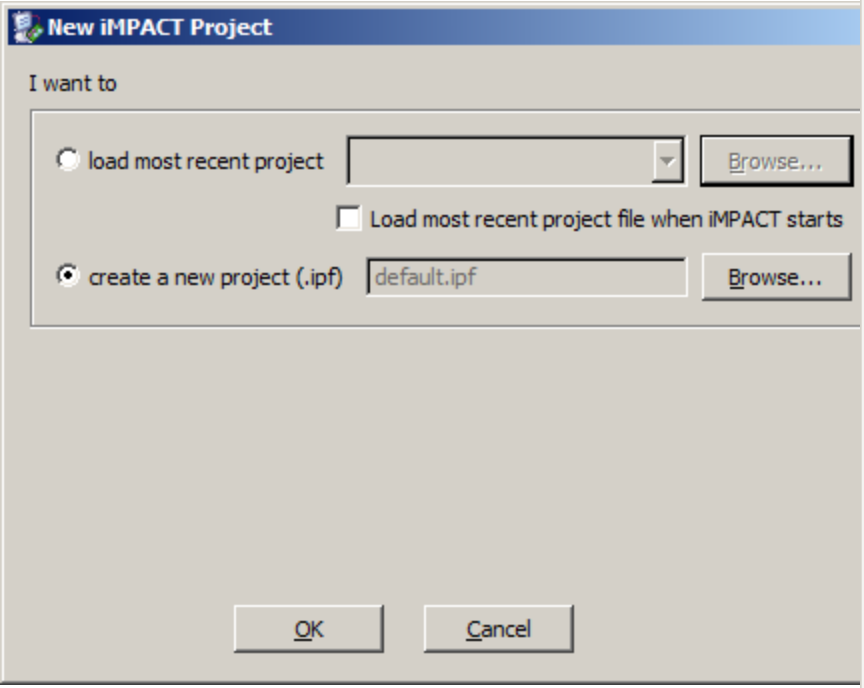
  **impact**

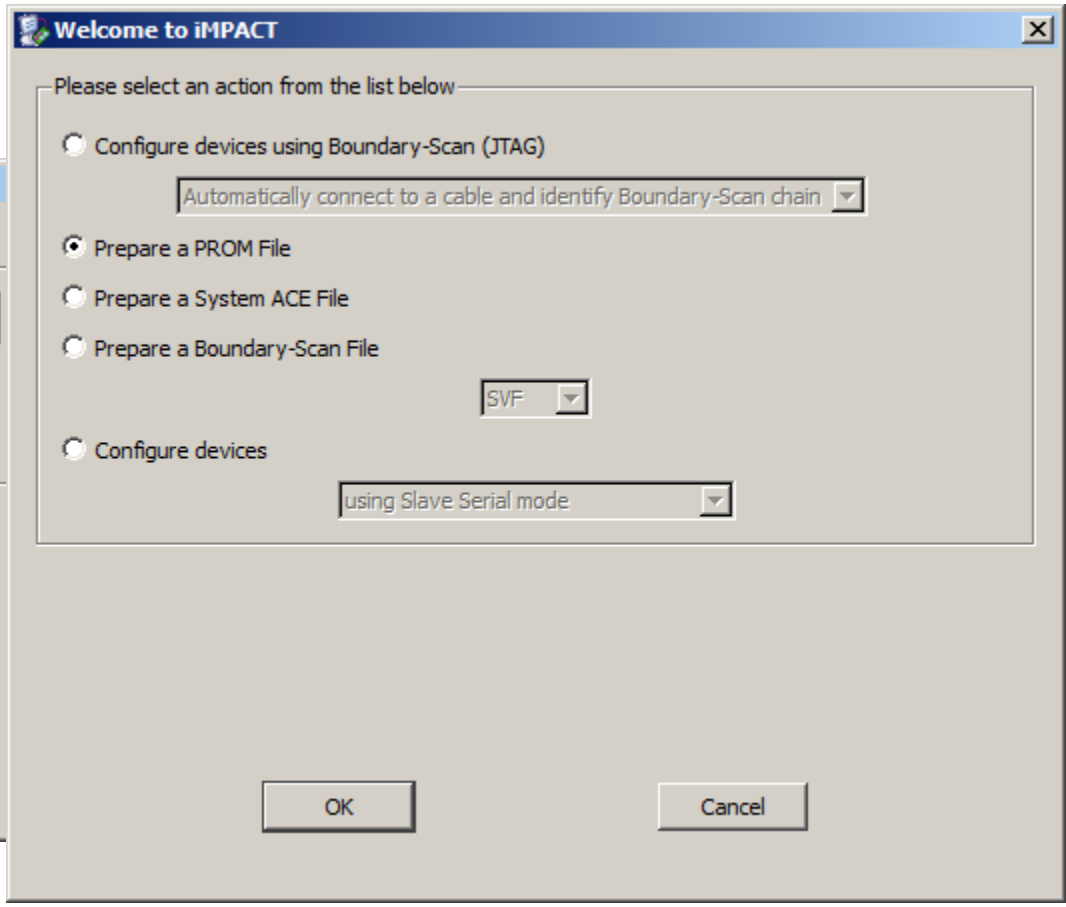



**Note:** Presentation applies to the SP605

# Program SPI Flash with PCIe Design

- **Select**
  - Create a new project
  - Prepare a PROM File

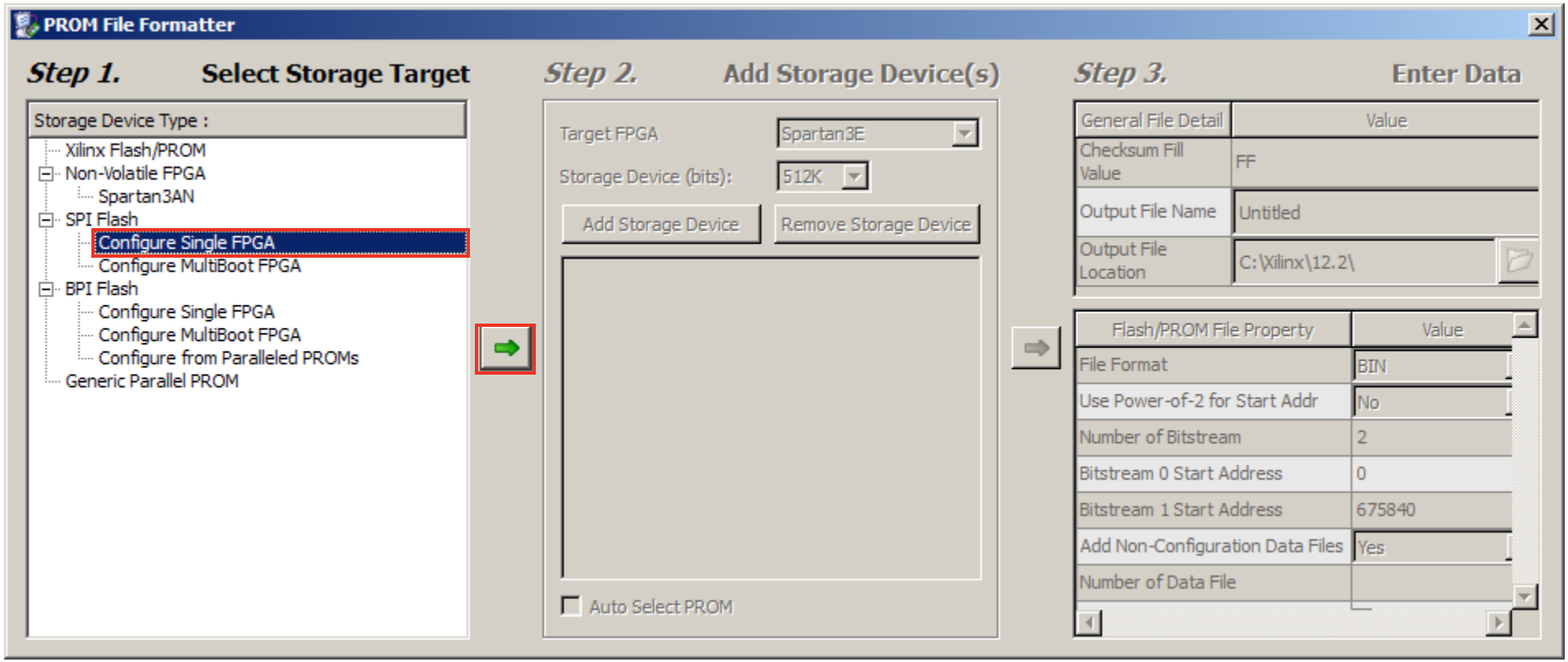



**Note:** Presentation applies to the SP605

# Program SPI Flash with PCIe Design

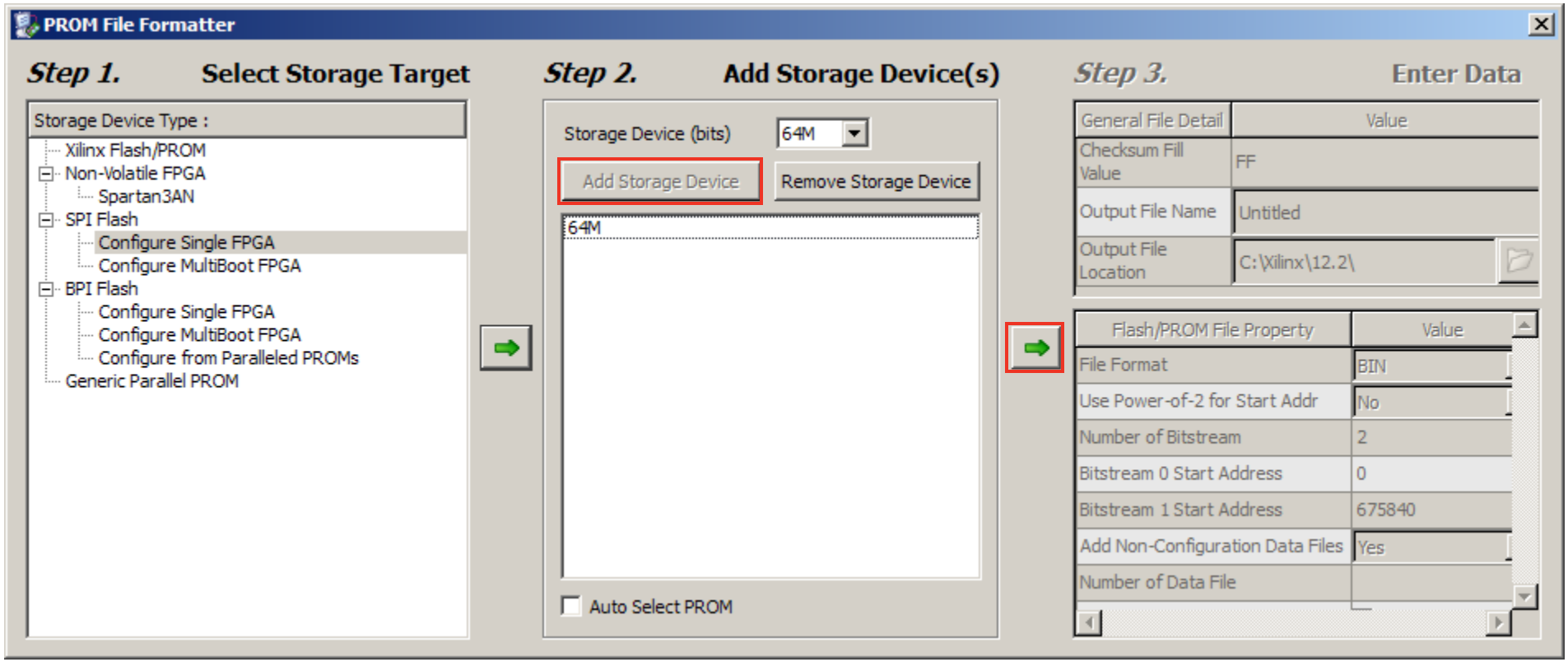
- **To generate a PROM file for the SPI Flash, select:**
  - SPI Flash – Configure Single FPGA




**Note:** Presentation applies to the SP605

# Program SPI Flash with PCIe Design

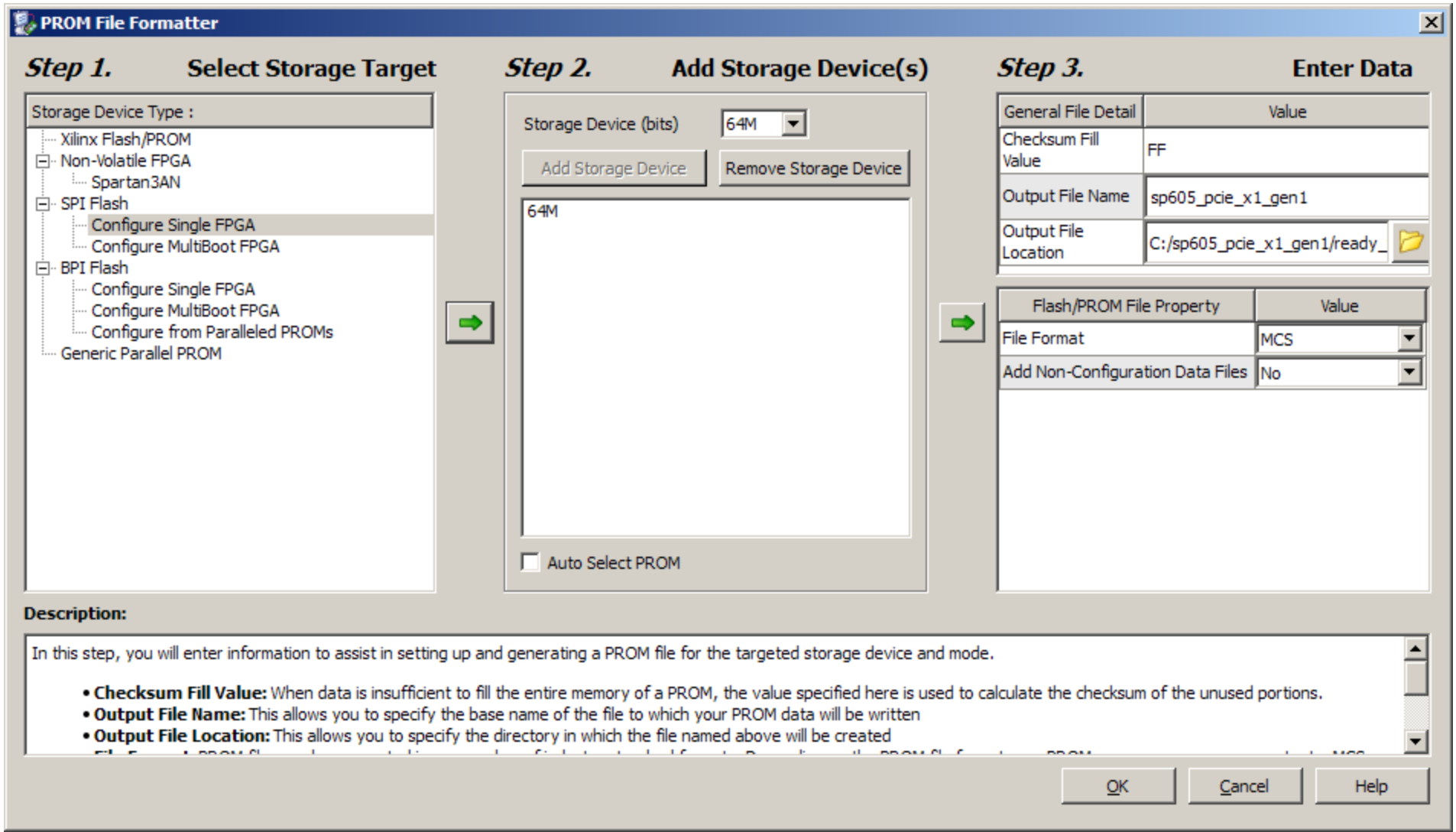
- Add 64M




**Note:** Presentation applies to the SP605

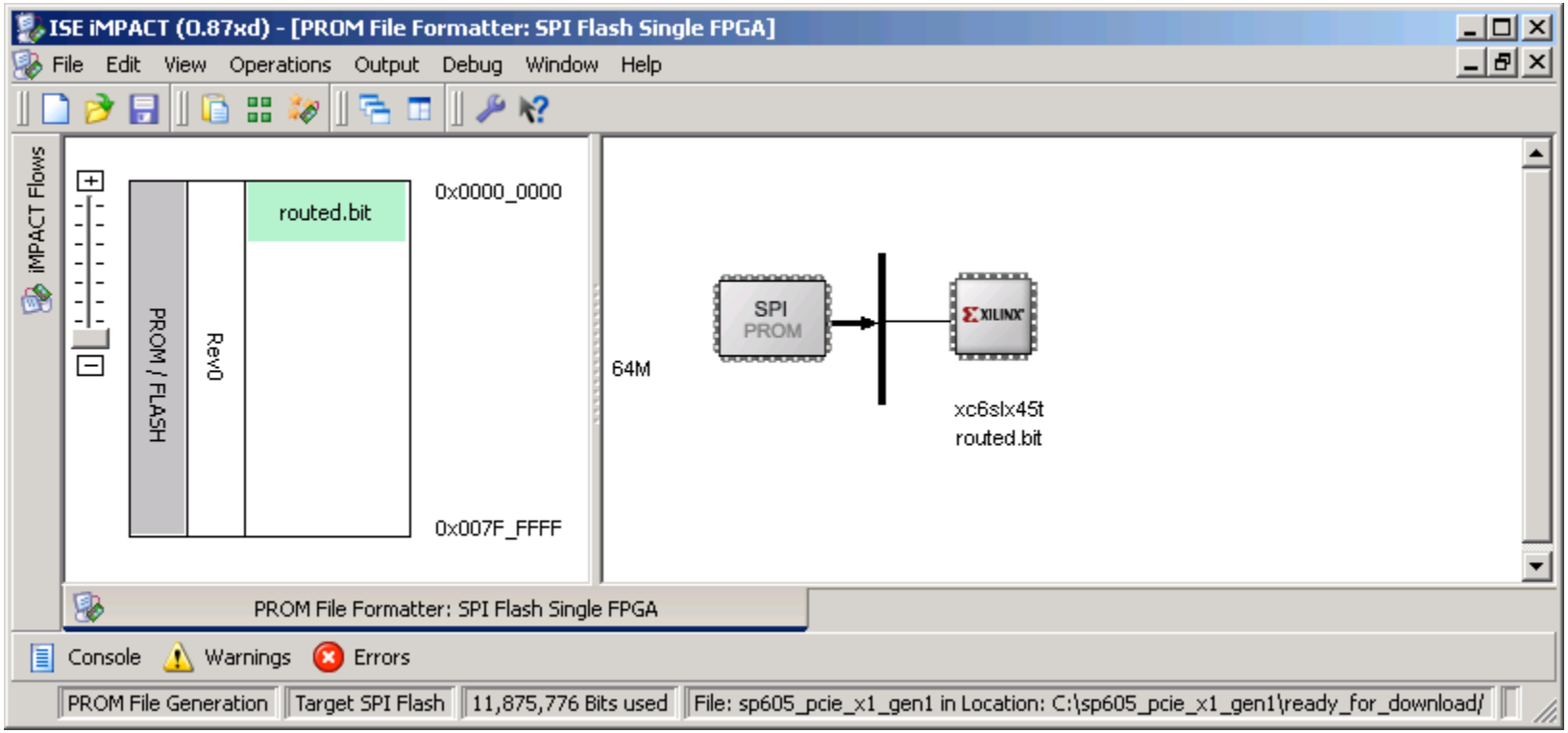
# Program SPI Flash with PCIe Design

- Set file name and save in <design path>\ready_for_download



# Program SPI Flash with PCIe Design

- Add routed.bit from the <design path> \s6_pcie_v2_4\implement\results




**Note:** Presentation applies to the SP605

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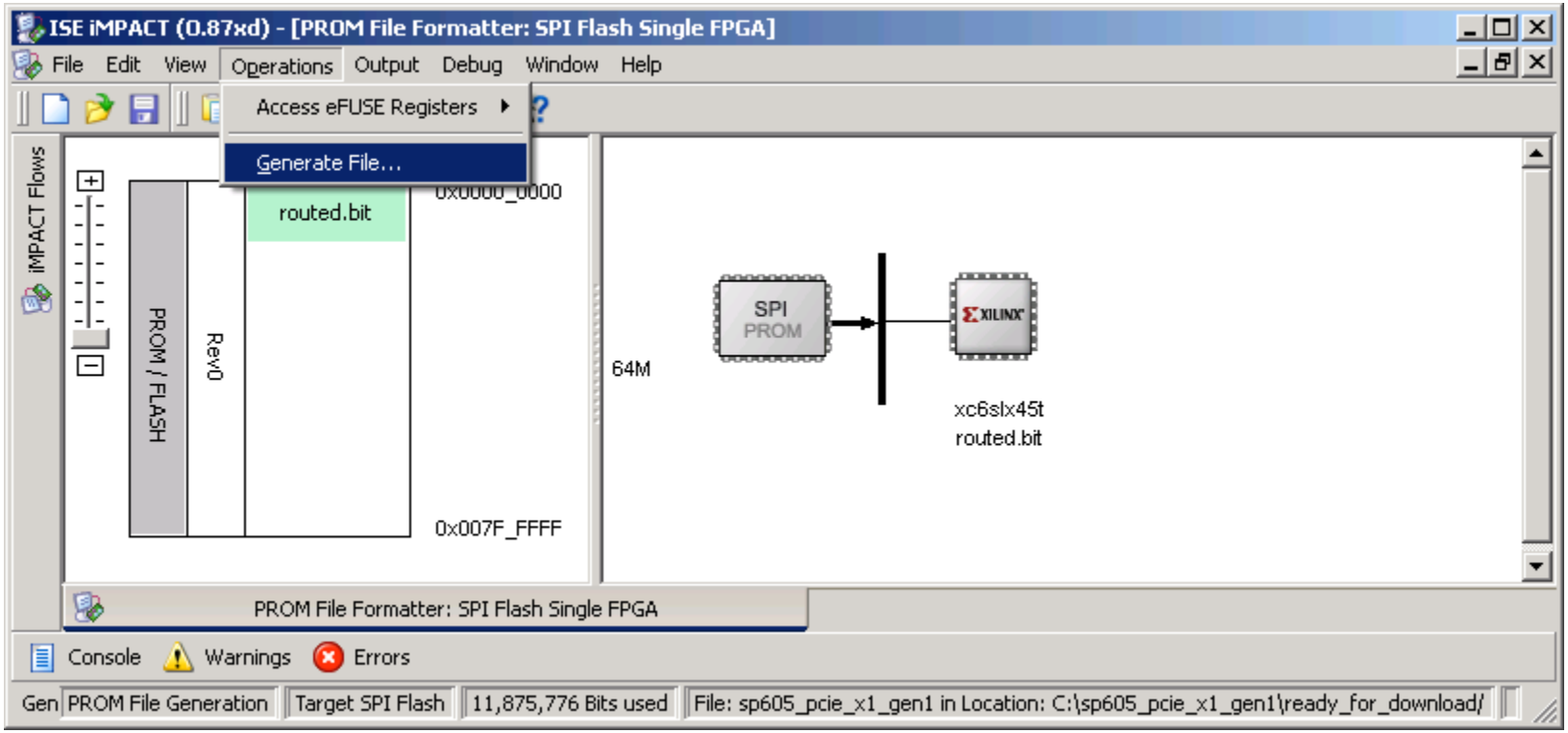
# Program SPI Flash with PCIe Design

- From the iMPACT menu, select

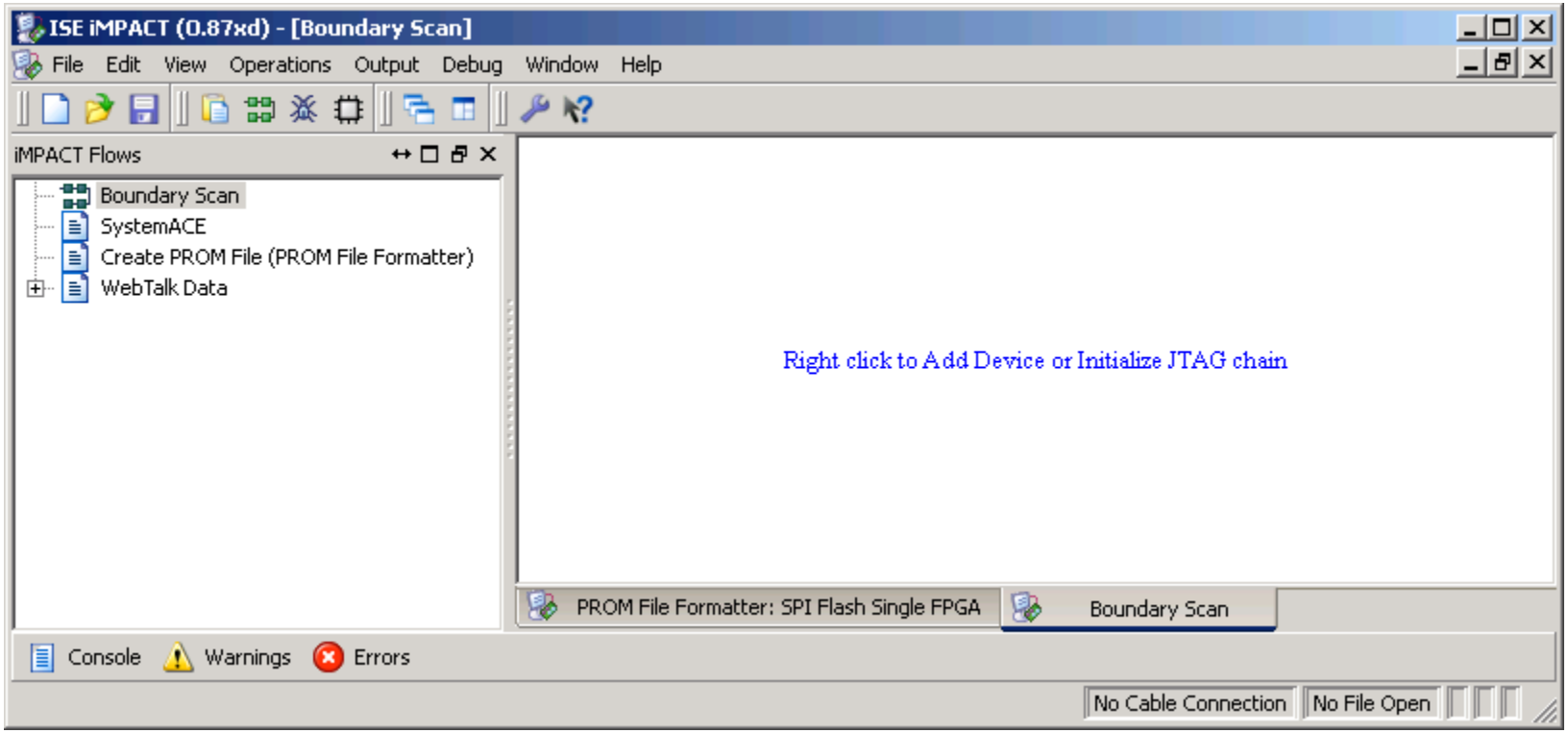
  **Operations → Generate File…**




**Note:** Presentation applies to the SP605

# Program SPI Flash with PCIe Design

- After generation completes, under the iMPACT Flows, double click on Boundary Scan

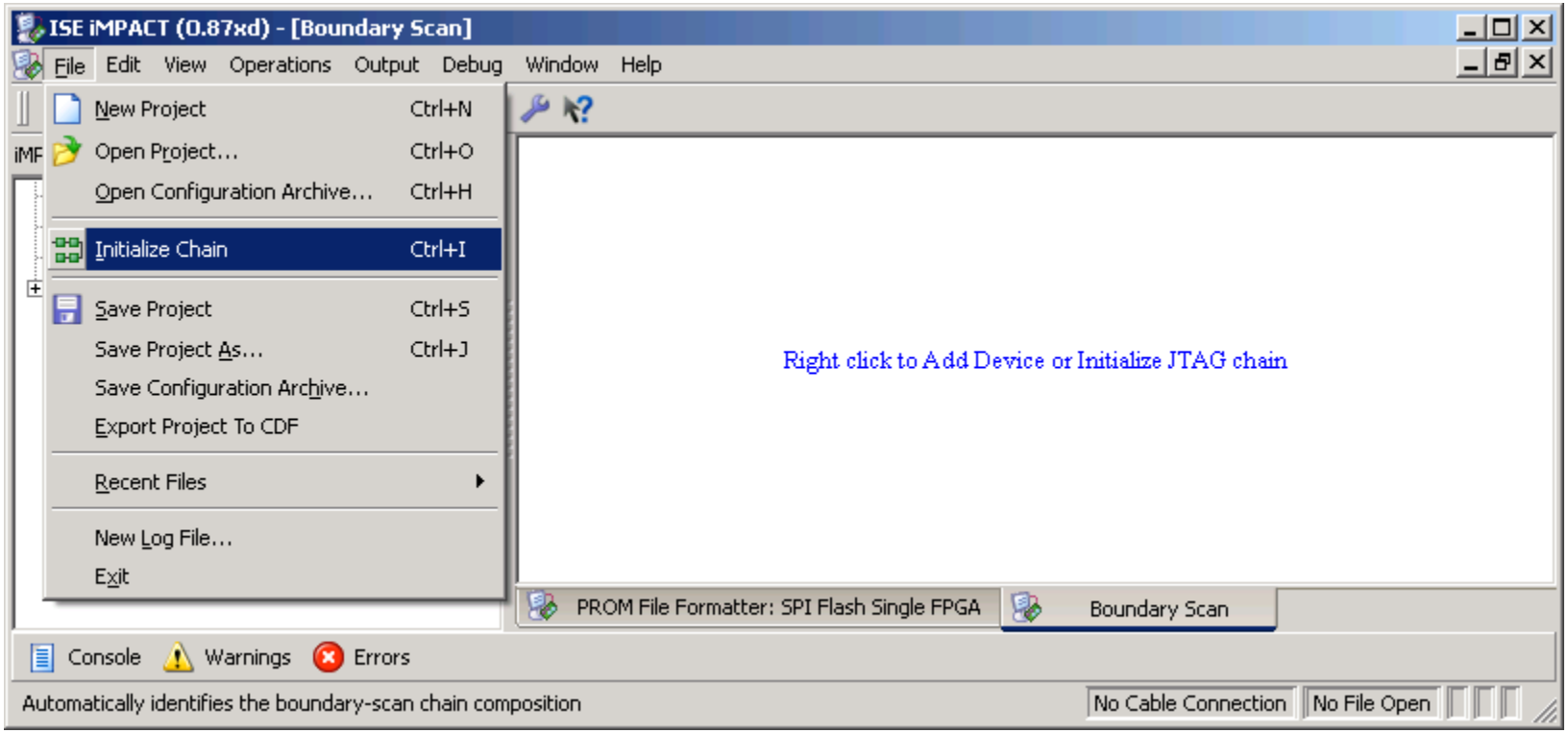



**Note:** Presentation applies to the SP605

# Program SPI Flash with PCIe Design

- **From the iMPACT menu, select**

  **File → Initialize Chain**




**Note:** Presentation applies to the SP605

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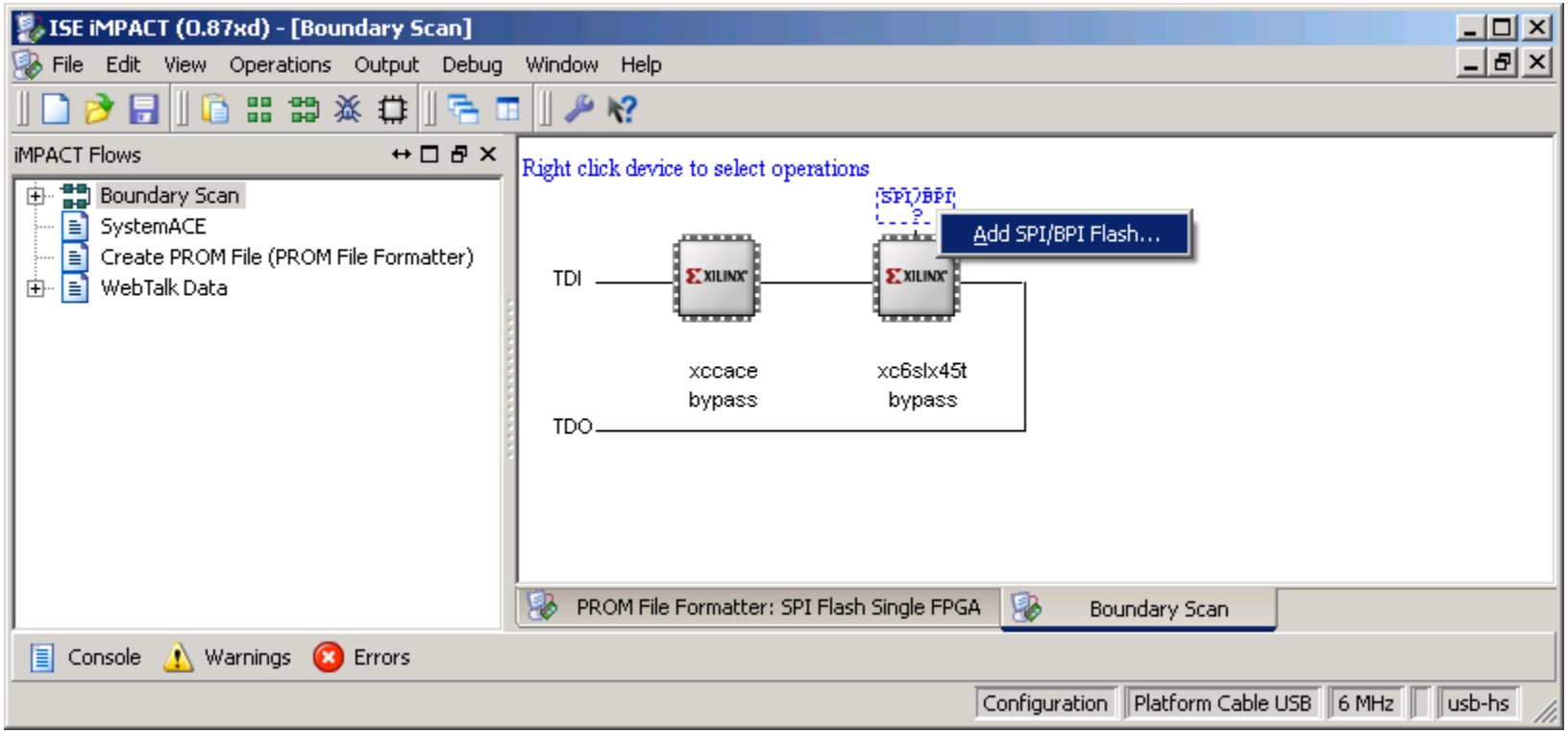
# Program SPI Flash with PCIe Design

- **Right click on the "SPI/BPI ?" box and select Add SPI/BPI Flash…**
  - Add <design path>\ready_for_download\sp605_pcie_x1_gen1.mcs




**Note:** Presentation applies to the SP605

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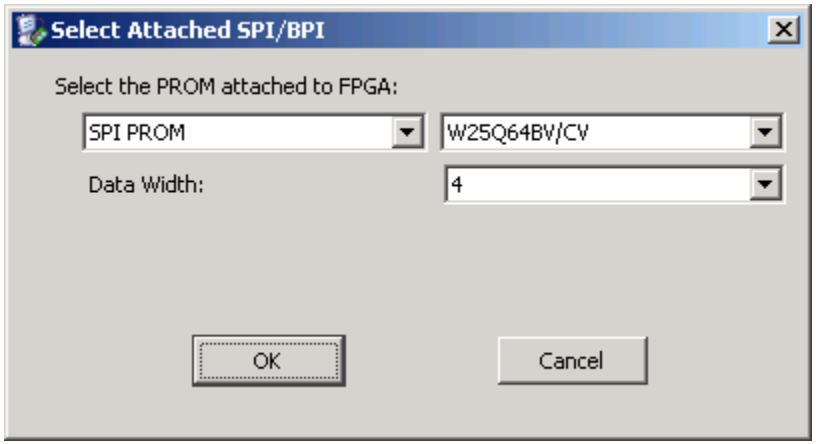
# Program SPI Flash with PCIe Design

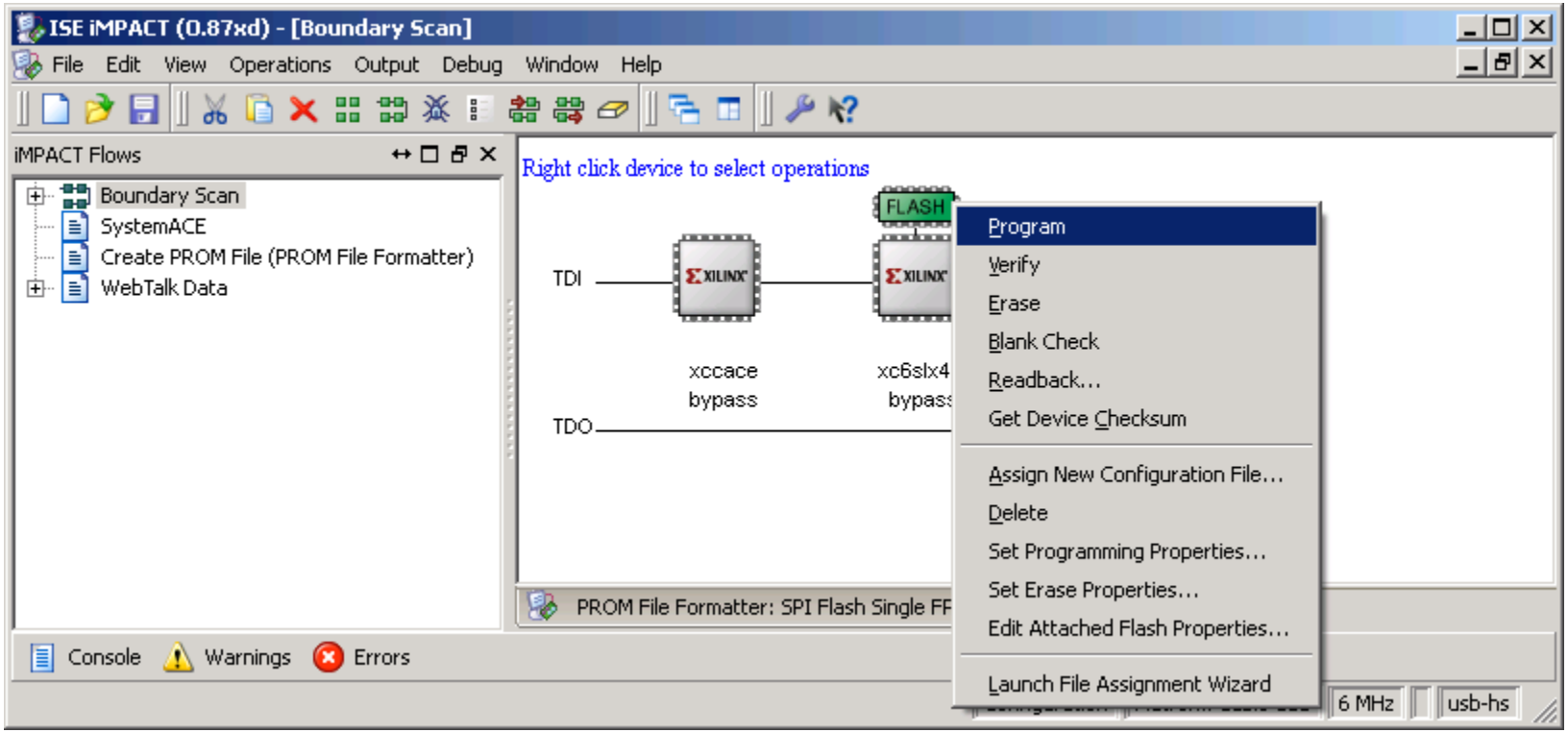
- **Select**
  - **SPI PROM**
  - **W25Q64BV/CV**
  - Data Width: **4**




**Note:** Presentation applies to the SP605

# Program SPI Flash with PCIe Design

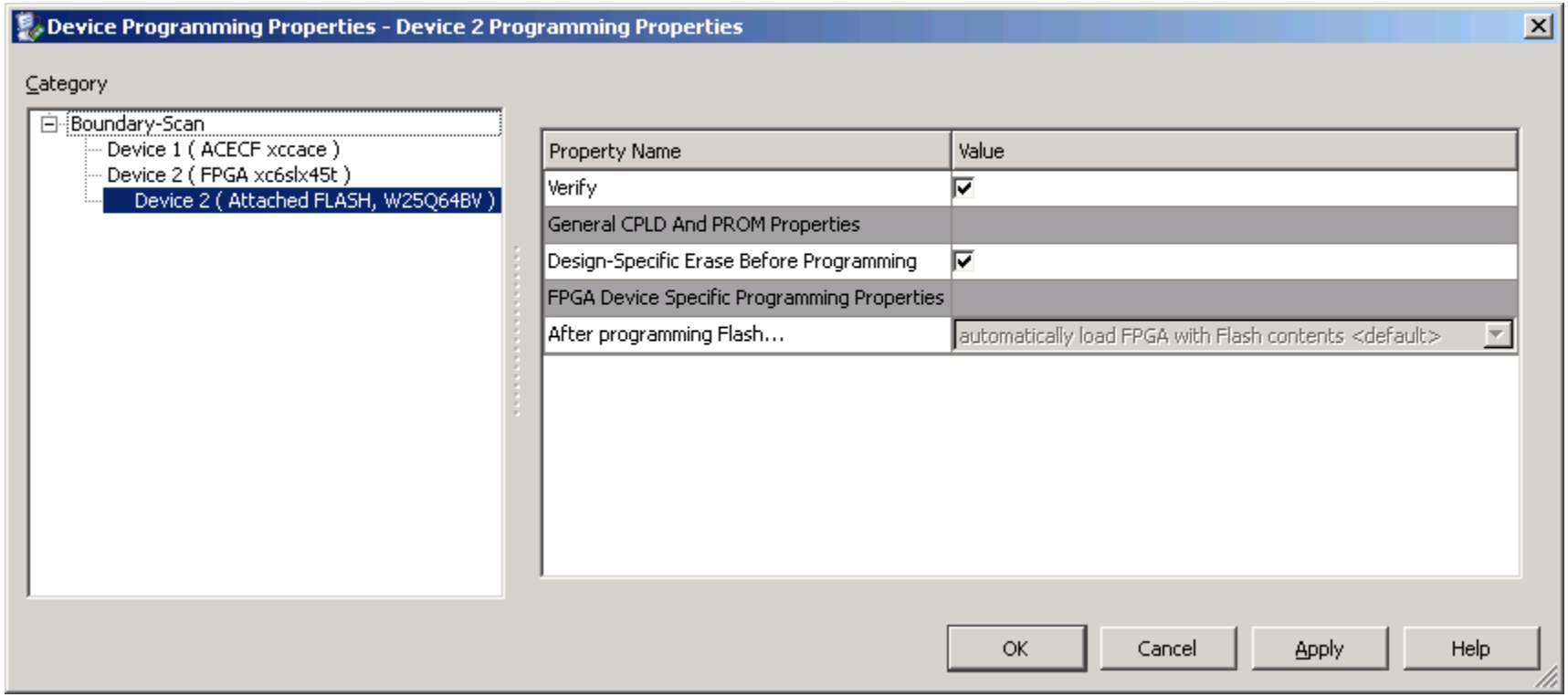
- **Right click on the Flash and select Program**
  - Use default settings to Erase and Verify device




**Note:** Programming takes about 5 minutes

# Program SPI Flash with PCIe Design

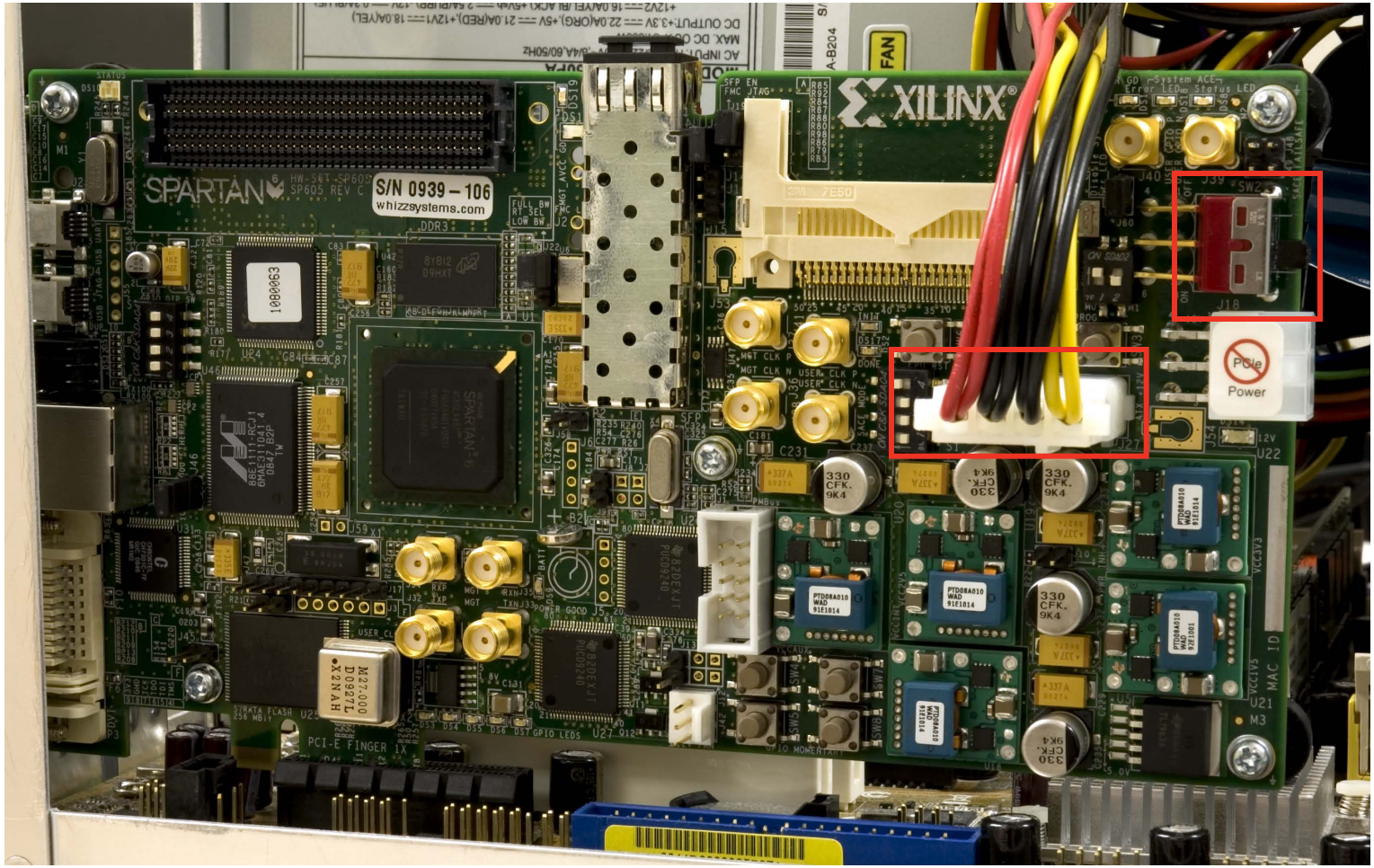
- **Erase Before Programming must be selected**




**Note:** Presentation applies to the SP605

# Hardware Setup

- **After programming completes, insert the SP605 Board into a PCIe slot**
  - Connect PC power to J27, turn on Power Switch

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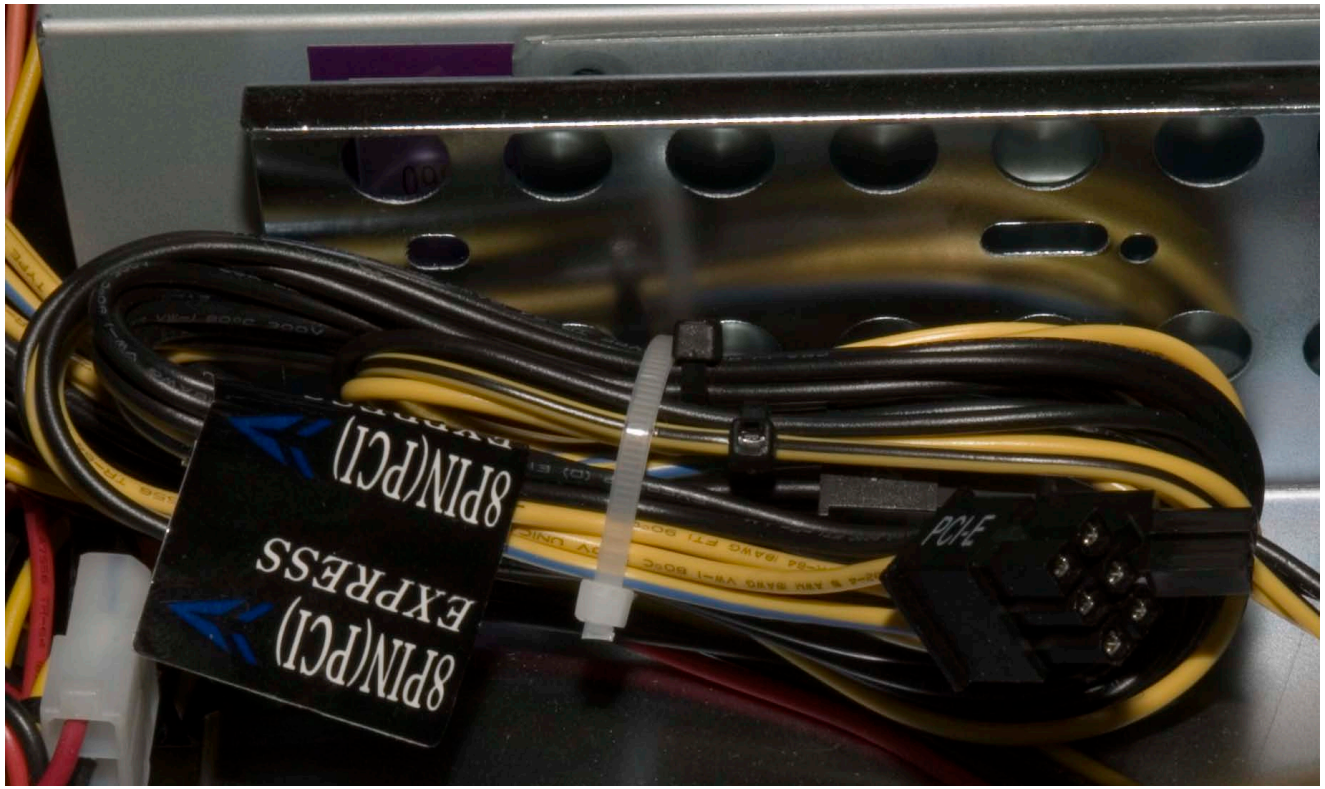
# Hardware Setup

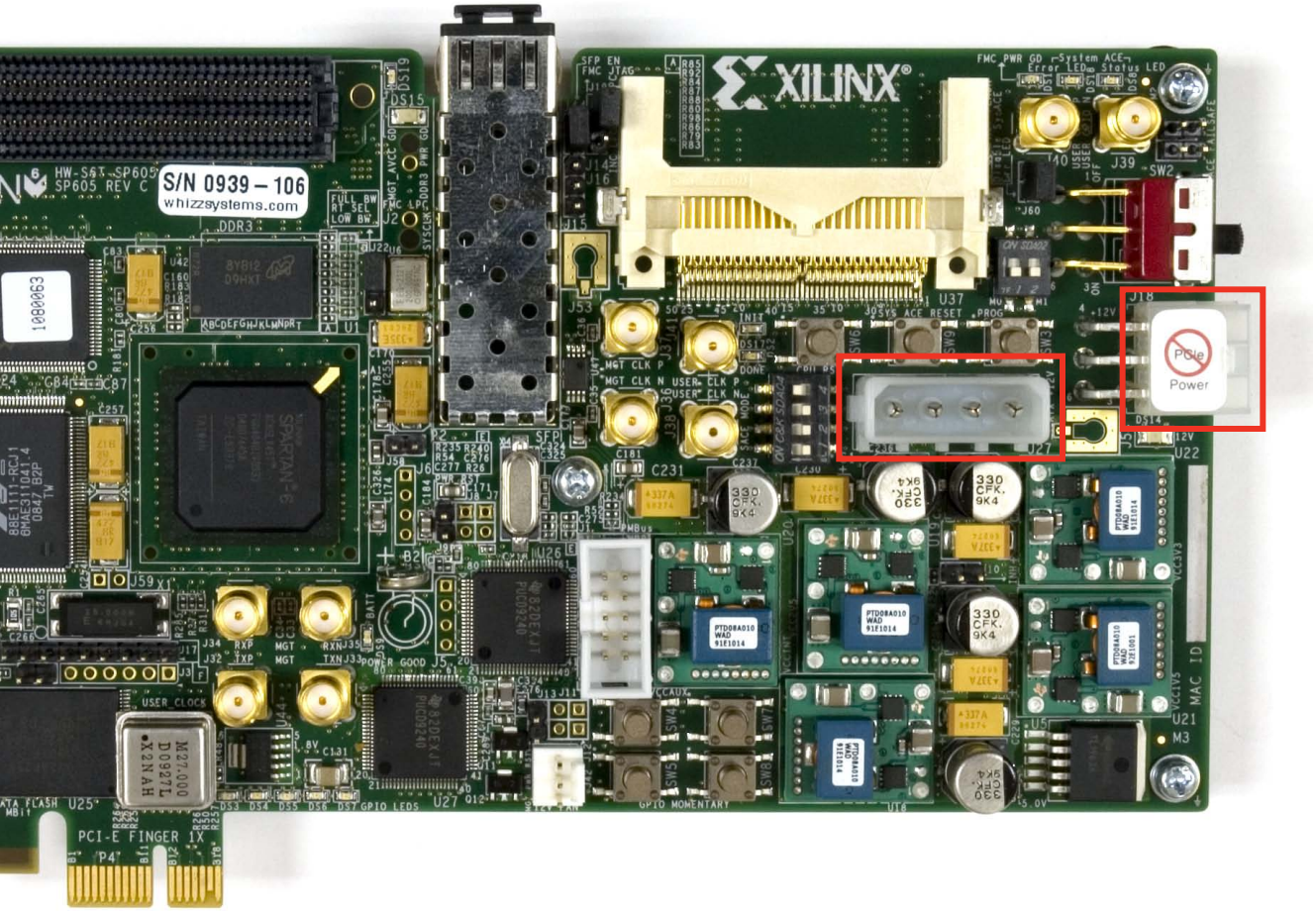
- Do *not* use the PCIe connector from the PC power supply

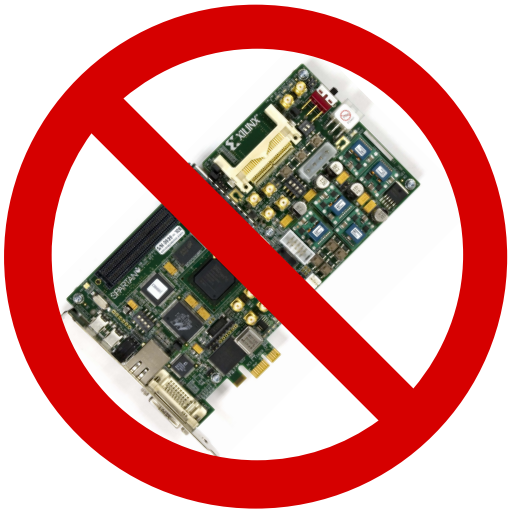



**Note:** Presentation applies to the SP605

# Hardware Setup

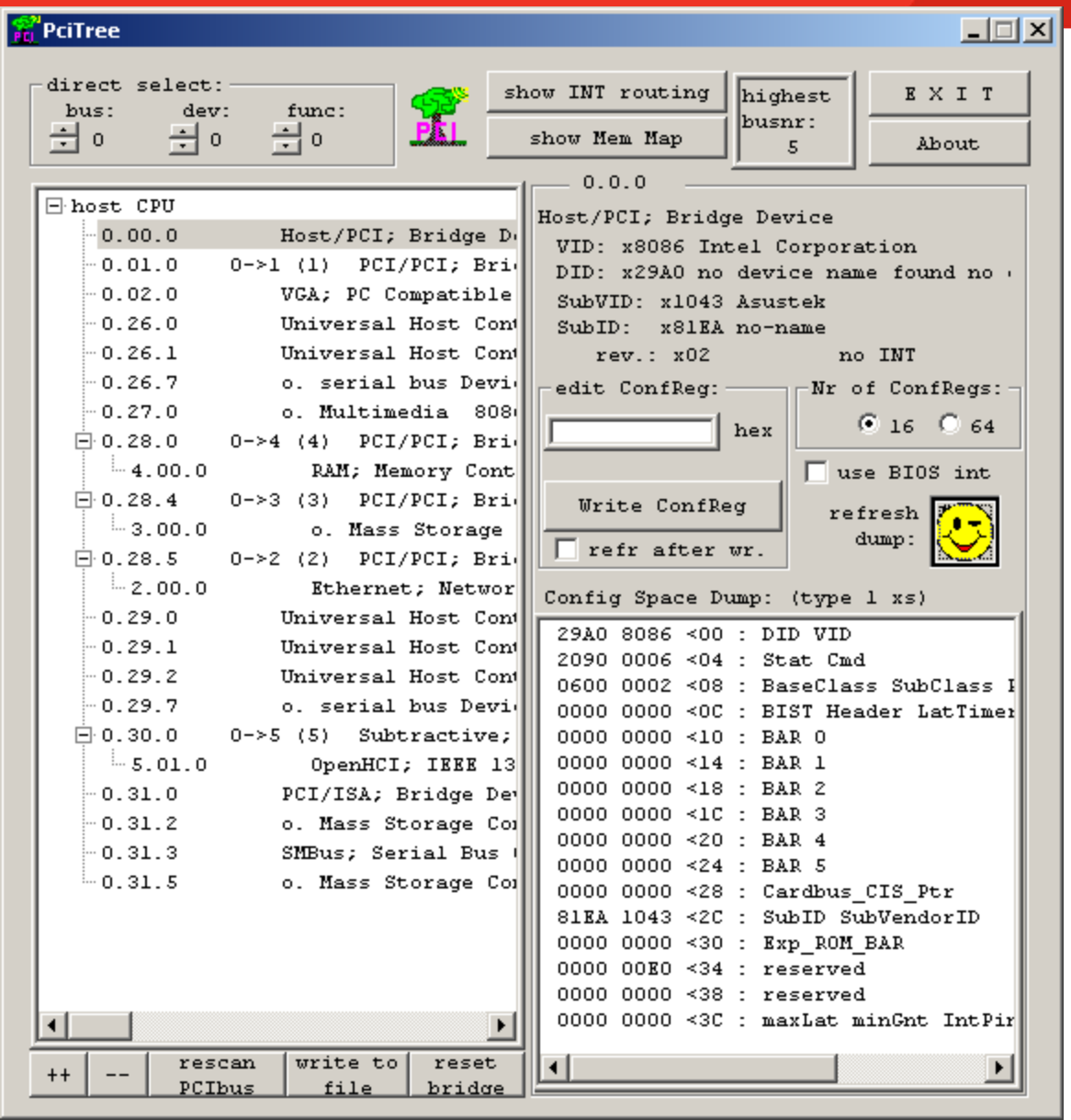
- Do not connect both the SP605 power brick connector (J60) and the four pin ATX power connector at the same time



**Note:** Presentation applies to the SP605

# Running the PCIe x1 Gen1 Design




- Power on the PC
- Start PciTree

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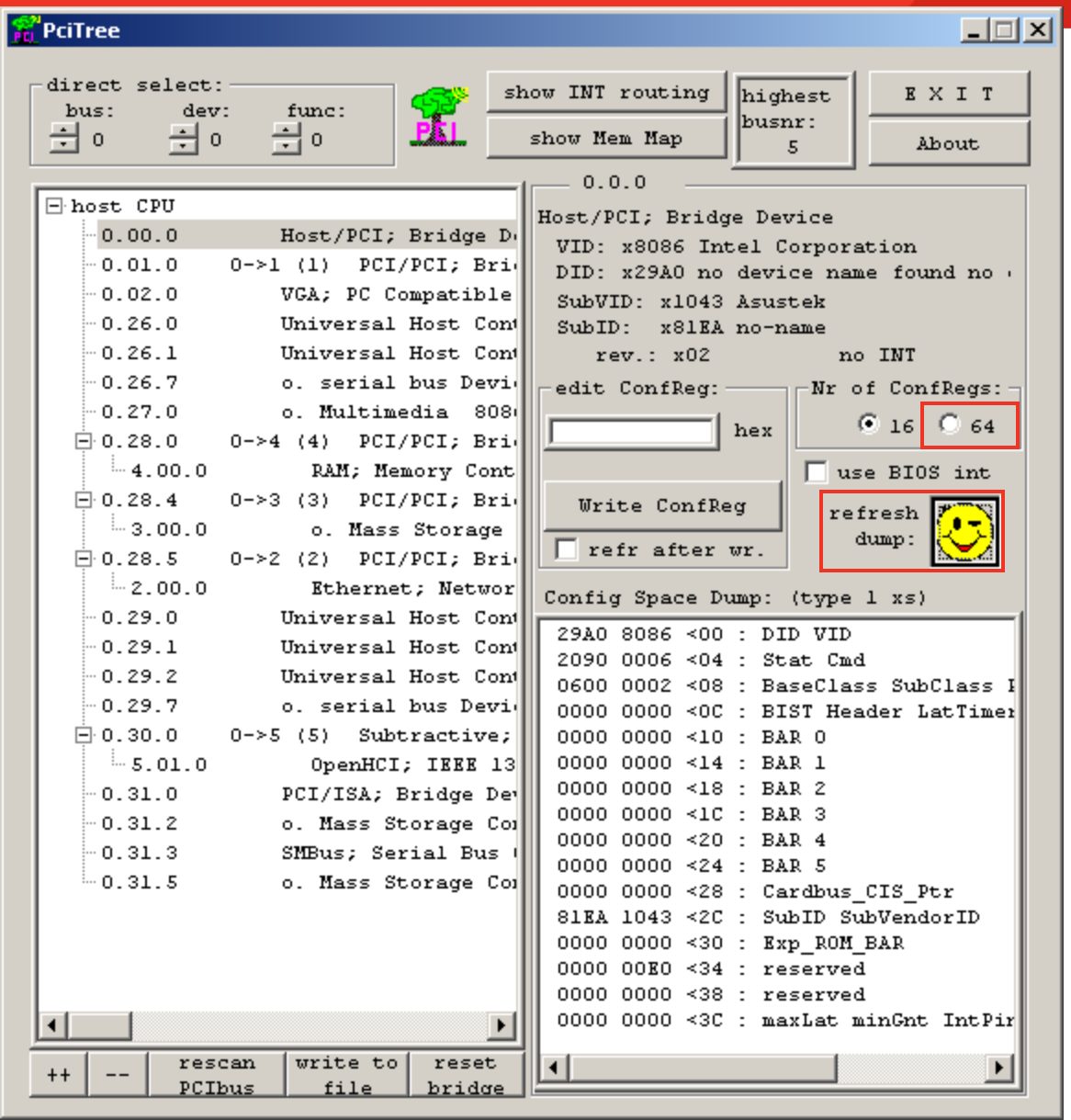
# Running the PCIe x1 Gen1 Design




- Set Number of Configuration Registers to 64
- Click on Refresh dump

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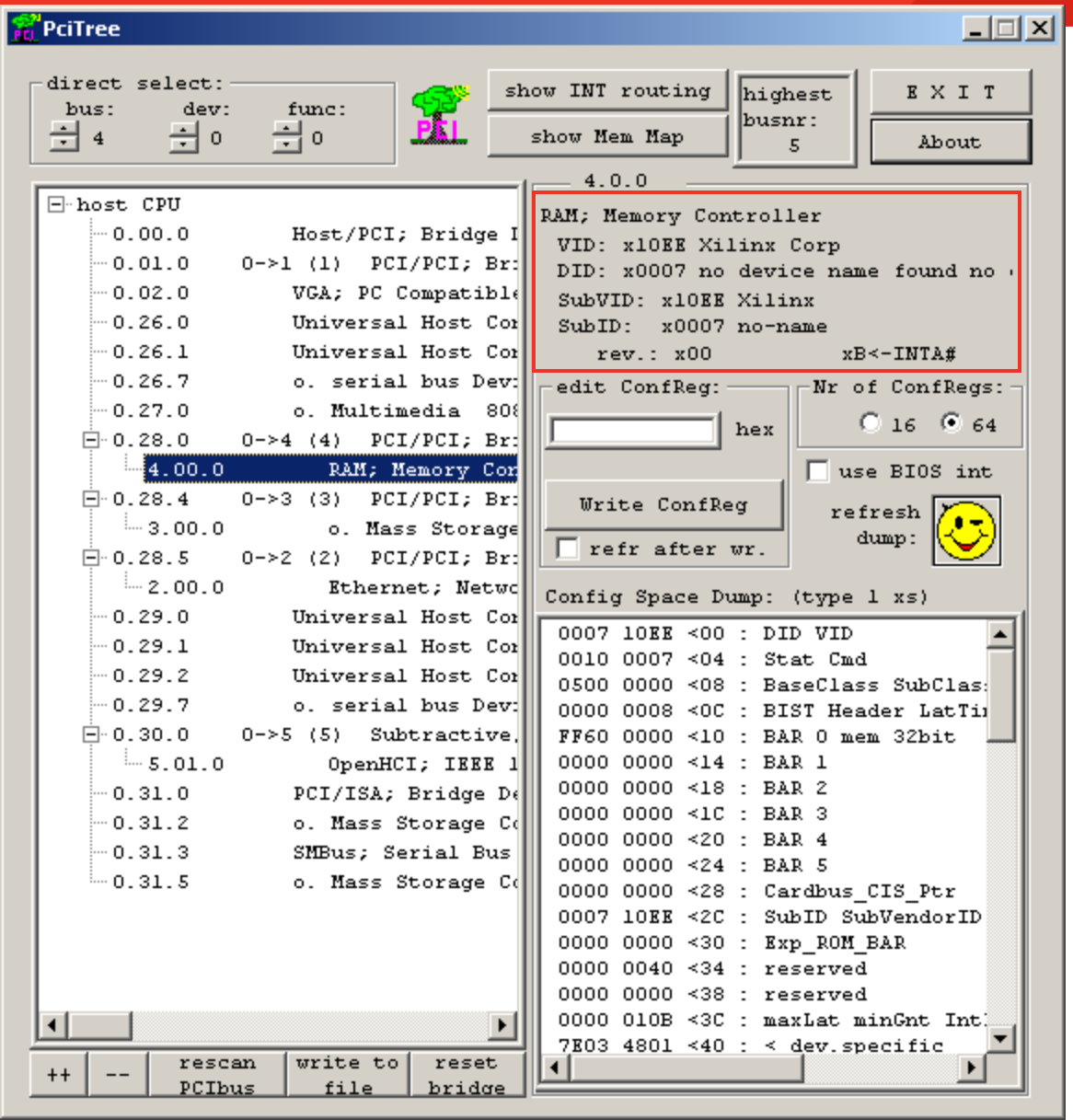
# Running the PCIe x1 Gen1 Design




- **Locate the Xilinx Device**
  - Vendor ID is **0x10EE**
  - Device ID is **0x0007**

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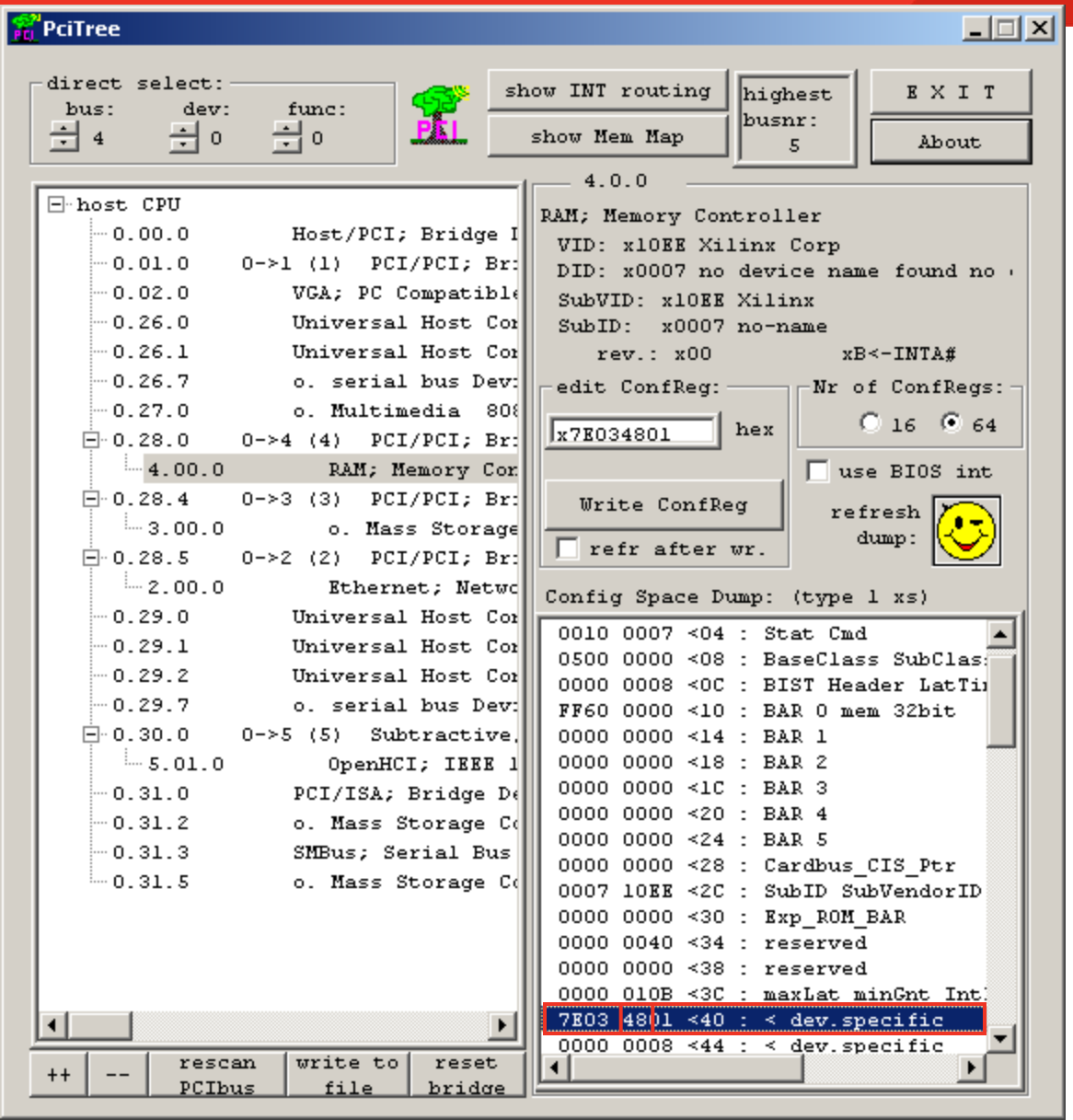
# Running the PCIe x1 Gen1 Design




- **Navigate the linked list in configuration space to locate the PCIe Capabilities Structure**
  - See UG654 for details
- **With the Xilinx device selected, select Register 0x40**
  - Register 0x40 points to the next structure
  - 0x48 is the address of the next structure

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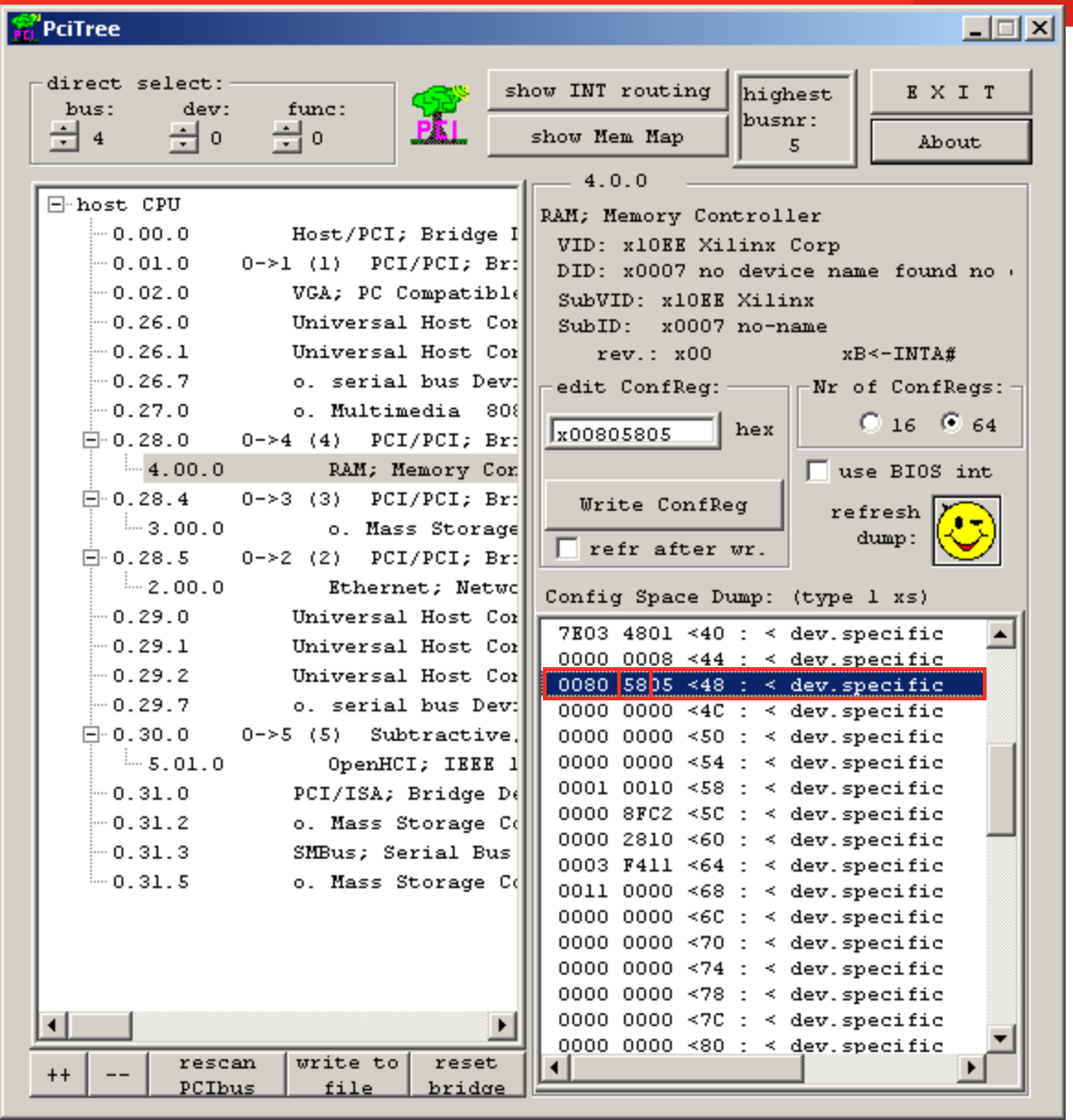
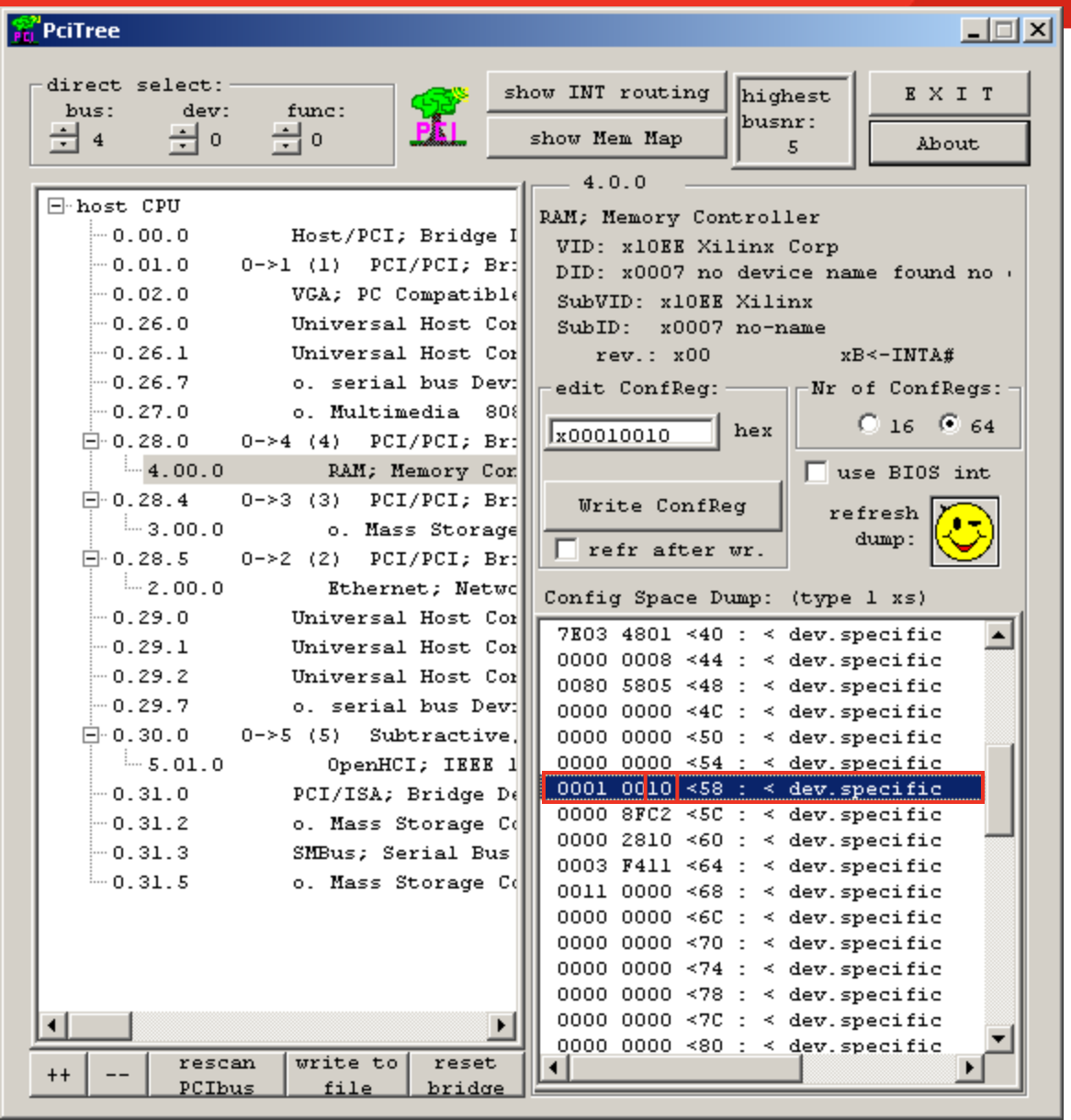
# Running the PCIe x1 Gen1 Design



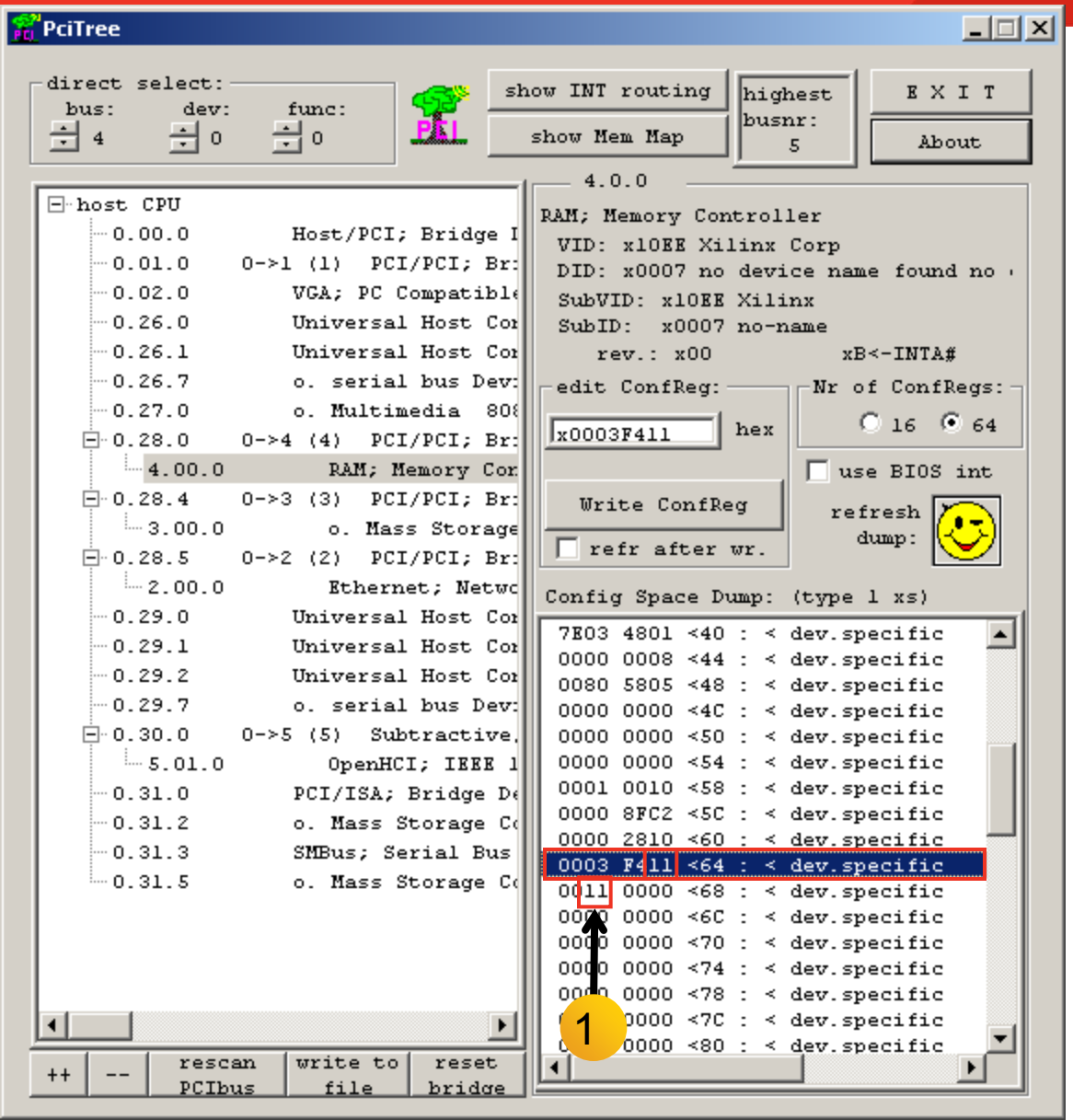

- **Select Register 0x48**
  - Register 0x48 points to the next structure
  - 0x58 is the address of the next structure

# Running the PCIe x1 Gen1 Design



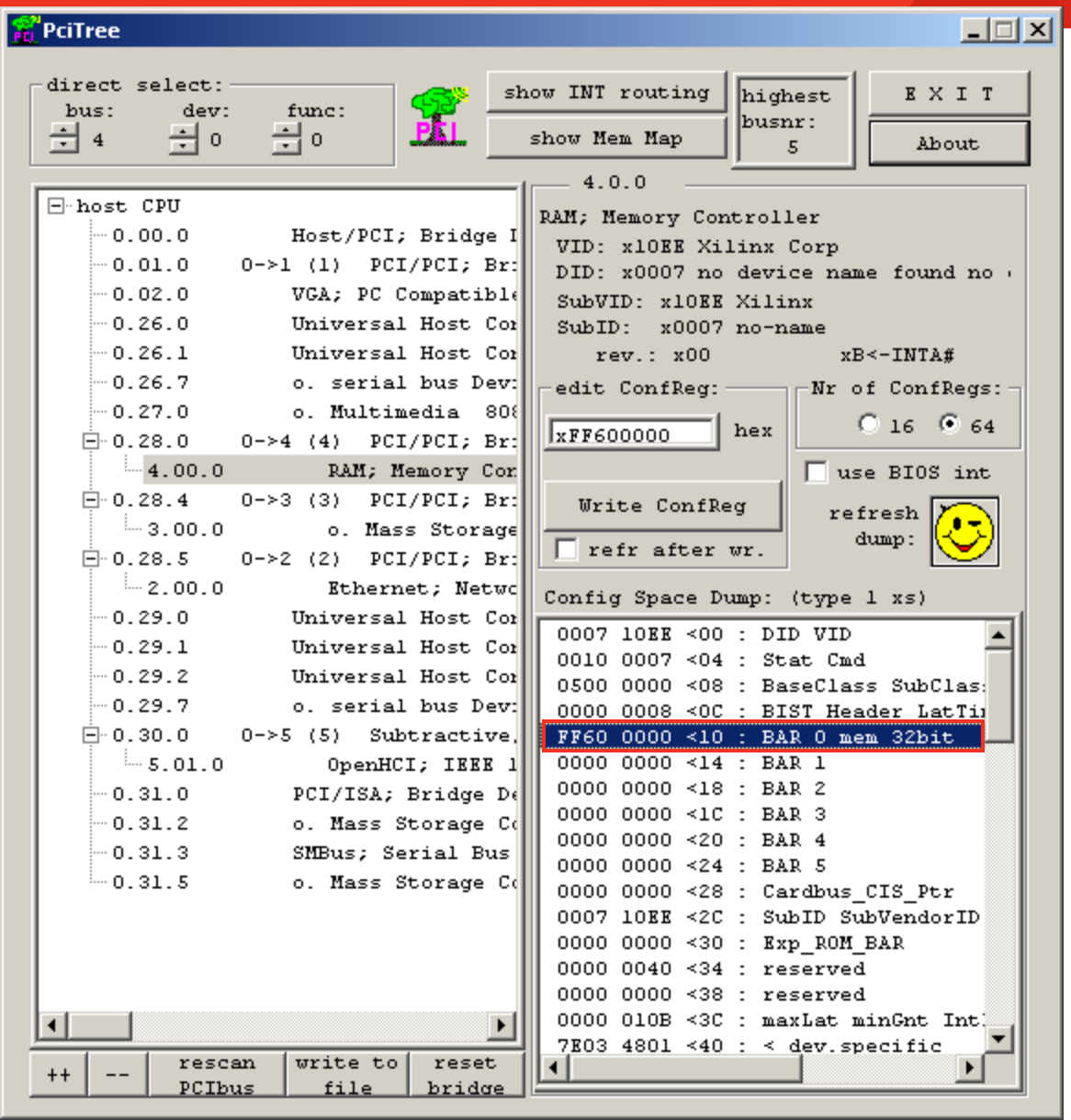

- **Register 0x58**
  - 0x58 is a type 0x10, indicating PCIe Capabilities Structure
  - Last Structure

# Running the PCIe x1 Gen1 Design

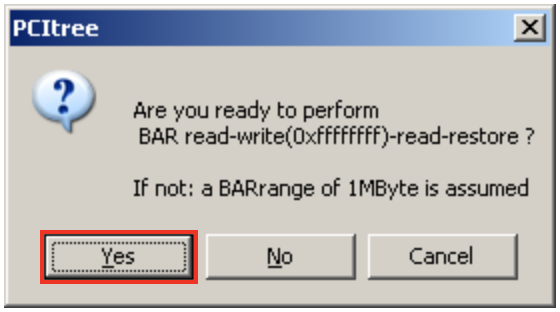



- **Register 0x64**
  - Link Capabilities Register
  - Indicates the maximum number of lanes and speed (Gen1, Gen2) for device
  - The value 0x11 shows this is an x1 Gen1 device
- **Link Status Register**
  - 0x68
  - Shows the current link status
  - This design trained to x1 Gen1 (1)

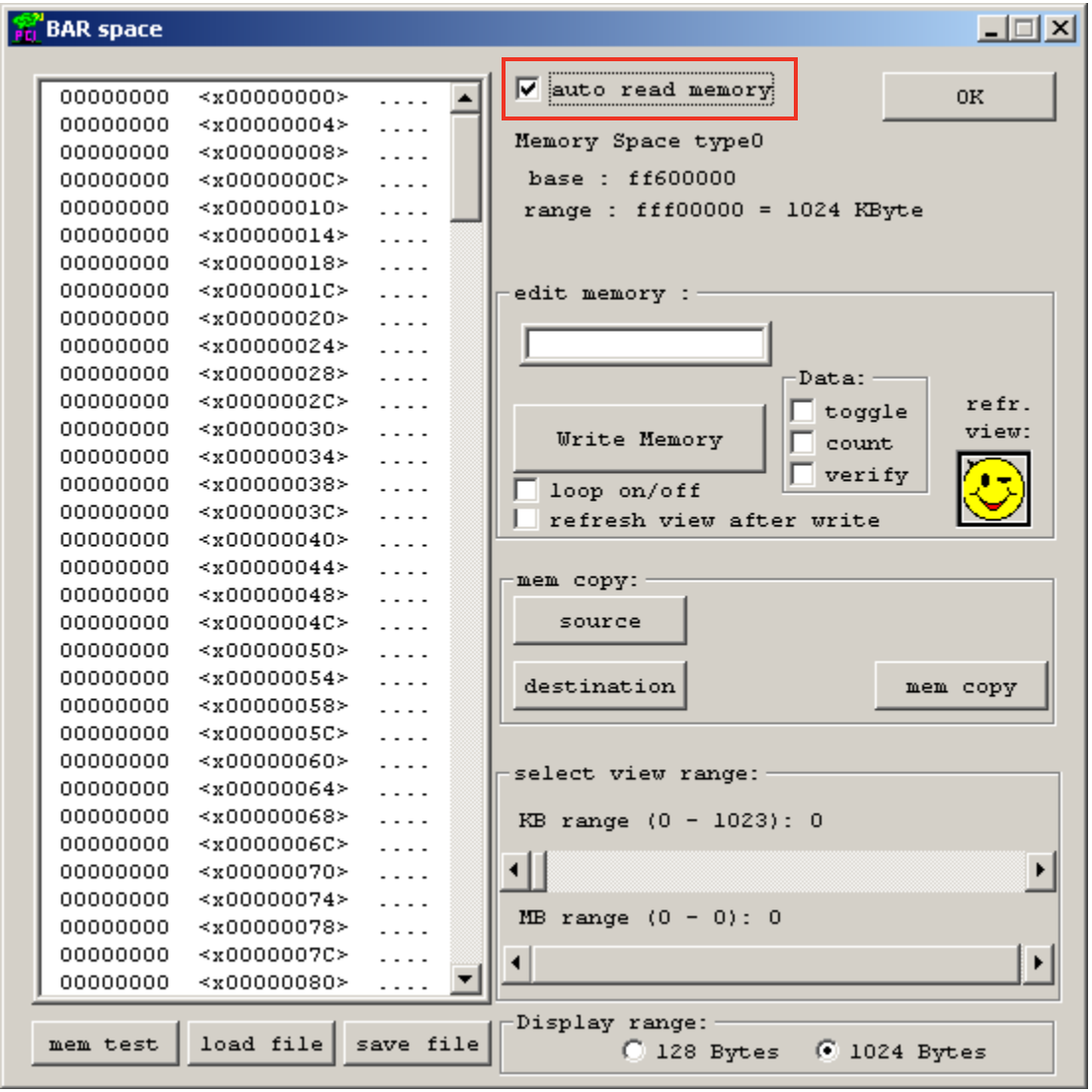
# Running the PCIe x1 Gen1 Design




- **Double-click on BAR 0**
  - BAR 0 Address is machine dependent
- **Click Yes on the Dialog box seen below**



# Running the PCIe x1 Gen1 Design




- Select auto read memory

**Note:** Presentation applies to the SP605

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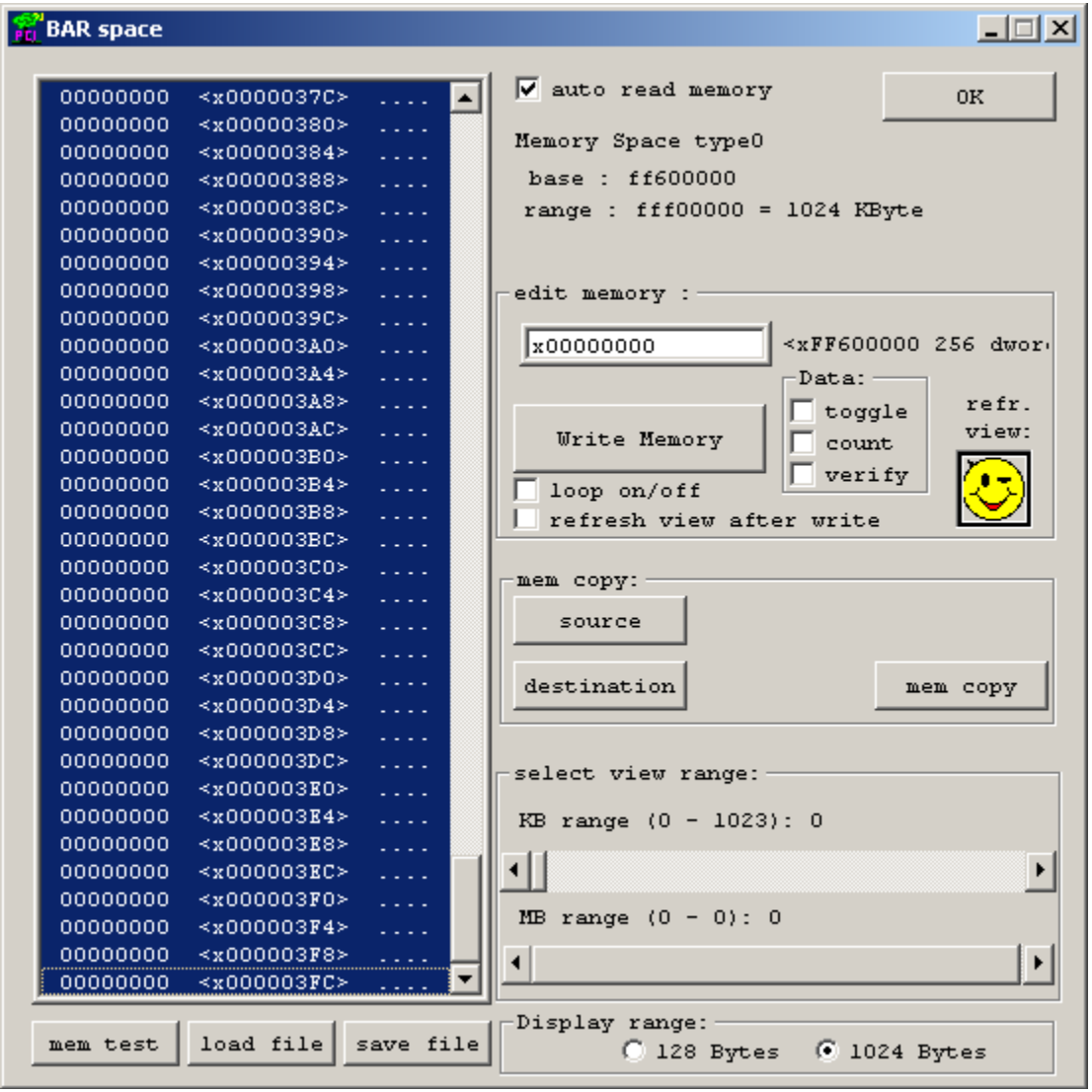
# Running the PCIe x1 Gen1 Design




- **Click on the first memory location**
  - Type <Shift-End> to select 1024 Bytes

**Note:** Presentation applies to the SP605

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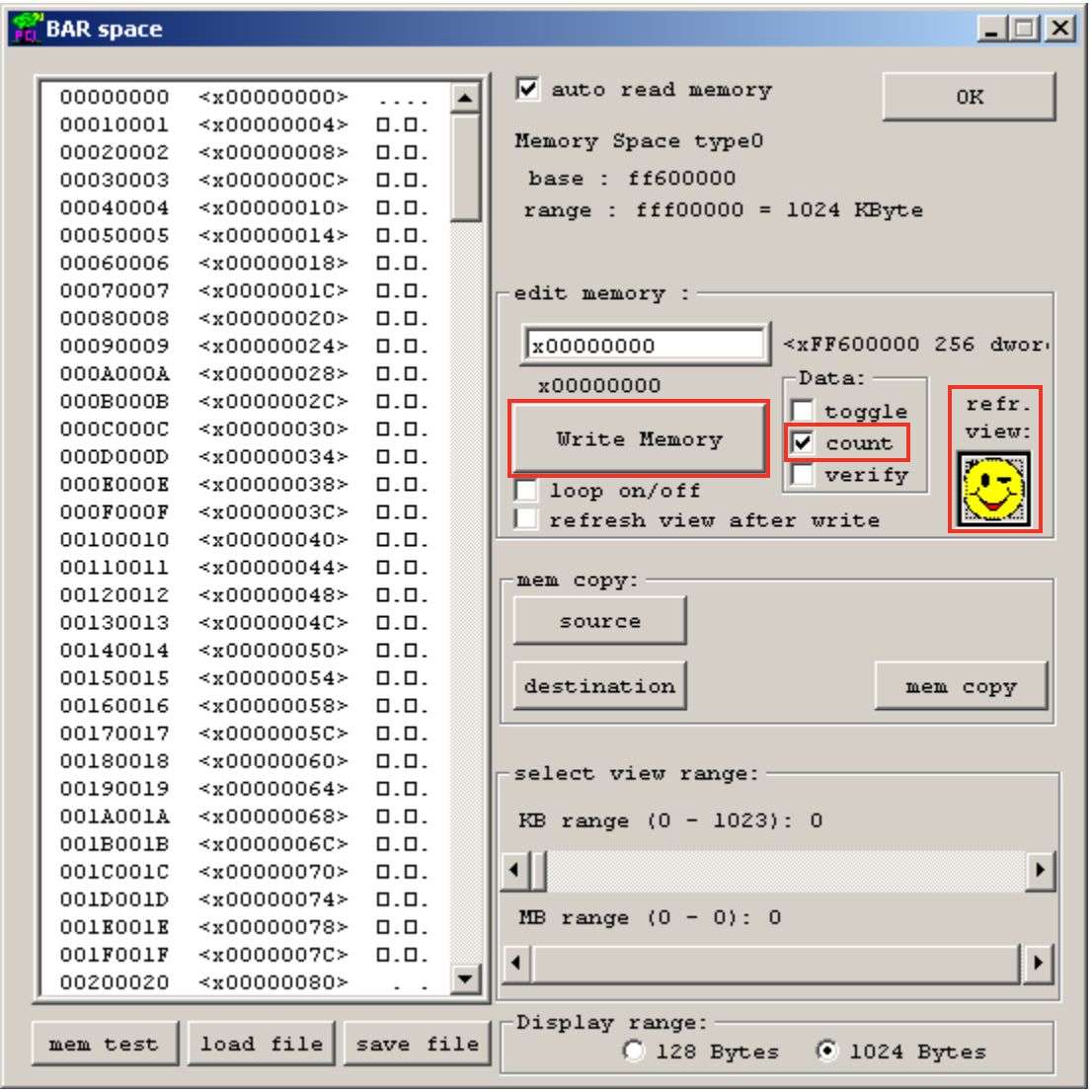
# Running the PCIe x1 Gen1 Design




- **Write Memory**
  - Select count
  - Click Write Memory
  - Click refr view
- **View results – counting up to FF**

**Note:** Presentation applies to the SP605

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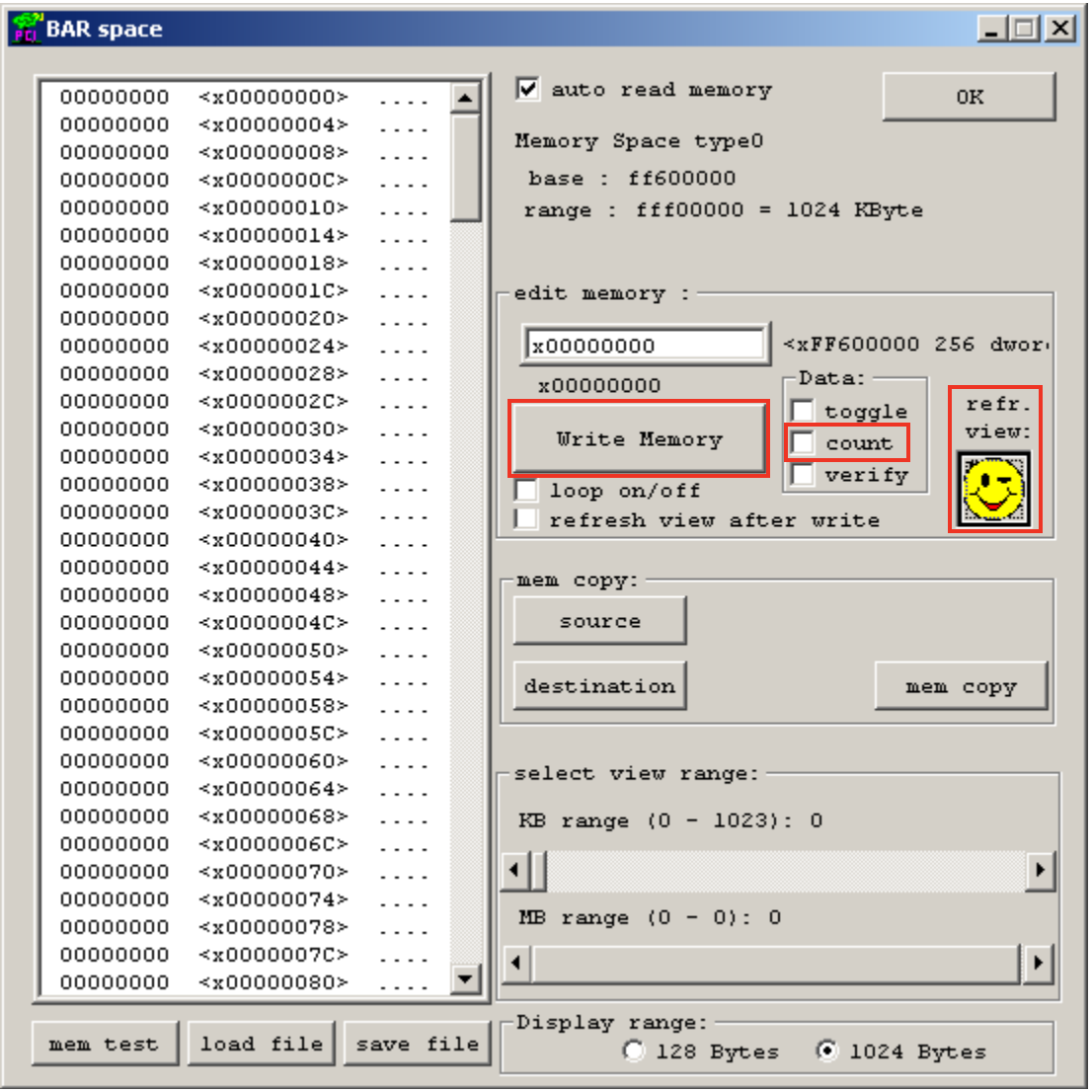
# Running the PCIe x1 Gen1 Design




- **Restore Memory**
  - Deselect count
  - Click Write Memory
  - Click refr view
- **Memory is reset to zeros**

**Note:** Presentation applies to the SP605

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# Spartan-6 PCIe x1 Gen1 Capability

- **SP605 Supports PCIe Gen1 Capability**
  - x1 Gen1 lane width
- **LogiCORE PIO Example Design**
  - RDF0035.zip
  - Available through http://www.xilinx.com/sp605
- **LogiCORE Integrated Block for PCI Express**
  - See UG654 for details

**Note:** Presentation applies to the SP605

# References

# References

- **PCIe Base Specification**
  - PCI SIG Web Site
    http://www.pcisig.com/home
- **Spartan-6 PCIe**
  - PCIe Product Overview
    http://www.xilinx.com/products/intellectual-property/S6_PCI_Express_Block.htm
  - Spartan-6 FPGA Integrated Block for PCI Express User Guide
    http://www.xilinx.com/support/documentation/user_guides/s6_pcie_ug654.pdf
  - Spartan-6 FPGA Integrated Block for PCI Express Data Sheet
    http://www.xilinx.com/support/documentation/ip_documentation/s6_pcie_ds718.pdf
  - IP Release Notes Guide
    http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf

# Documentation

# Documentation

- **Spartan-6**
  - Spartan-6 FPGA Family
    http://www.xilinx.com/products/silicon-devices/fpga/spartan-6/index.htm
- **SP605 Documentation**
  - Spartan-6 FPGA SP605 Evaluation Kit
    http://www.xilinx.com/products/boards-and-kits/EK-S6-SP605-G.htm
  - SP605 Getting Started Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug525.pdf
  - SP605 Hardware User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug526.pdf
  - SP605 Reference Design User Guide
    http://www.xilinx.com/support/documentation/boards_and_kits/ug527.pdf