

SP605 PCIe x1 Gen1 Design Creation

March 2012

Revision History

Date	Version	Description
03/16/12	13.4	Recompiled under 13.4.
10/26/11	13.3	Recompiled under 13.3.
07/06/11	13.2	Recompiled under 13.2.
03/01/11	13.1	Recompiled under 13.1.
12/21/10	12.4	Recompiled under 12.4.
10/05/10	12.3	Recompiled under 12.3.
07/23/10	12.2	Recompiled under 12.2.

© Copyright 2012 Xilinx, Inc. All Rights Reserved.

XILINX, the Xilinx logo, the Brand Window and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

NOTICE OF DISCLAIMER: The information disclosed to you hereunder (the "Information") is provided "AS-IS" with no warranty of any kind, express or implied. Xilinx does not assume any liability arising from your use of the Information. You are responsible for obtaining any rights you may require for your use of this Information. Xilinx reserves the right to make changes, at any time, to the Information without notice and at its sole discretion. Xilinx assumes no obligation to correct any errors contained in the Information or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE INFORMATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

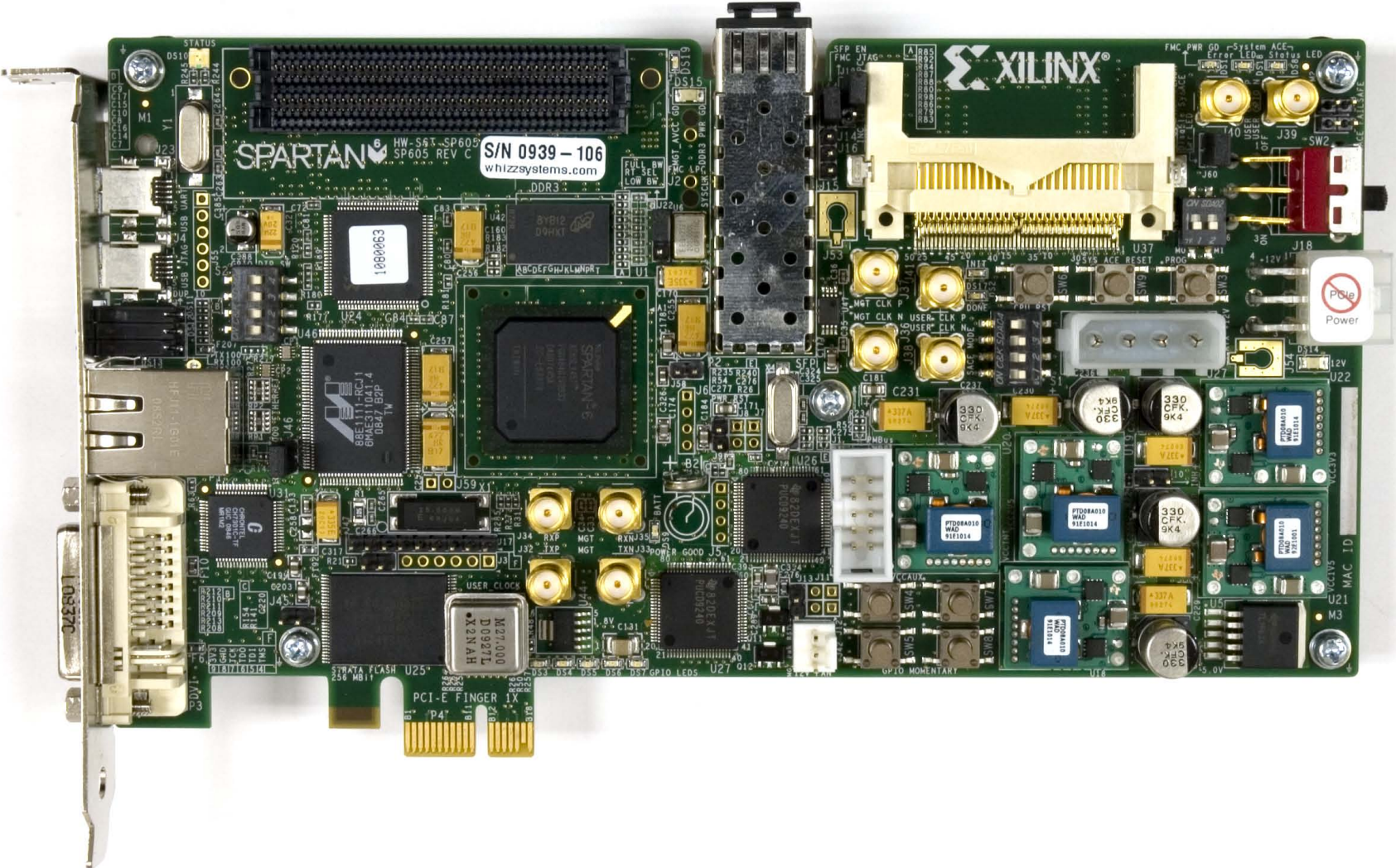
Overview

- **Spartan-6 PCIe x1 Gen1 Capability**
- **Xilinx SP605 Board**
- **Software Requirements**
- **Generate PCIe Core**
- **Compile PCIe Core**
- **Program SPI Flash with PCIe Design**
- **SP605 Setup**
- **Running the PCIe x1 Gen1 Design**
- **References**
 - IP Release Notes Guide [XTP025](#)

Spartan-6 PCIe x1 Gen1 Capability

- **Integrated Block for PCI Express**
 - PCI Express Base 1.1 Specification
- **Generation 1 (2.5 Gb/s) data rates**
 - x1 Gen1 lane width
- **Configurable for Endpoint**
 - SP605 configured for Endpoint Applications
- **GTP Transceivers implement a fully compliant PHY**
- **Large range of maximum payload size**
 - 128 / 256 / 512 bytes
- **Configurable BAR spaces**
 - Up to 6 x 32 bit, 3 x 64 bit, or a combination
 - Memory or IO
 - BAR and ID filtering

Xilinx SP605 Board



Note: Presentation applies to the SP605



ISE Software Requirement

- **Xilinx ISE 13.4 software**



PciTree Software Requirement

■ PciTree Bus Viewer

- Free [download](#)
- HLP.SYS must be copied to C:\WINDOWS\system32\drivers directory

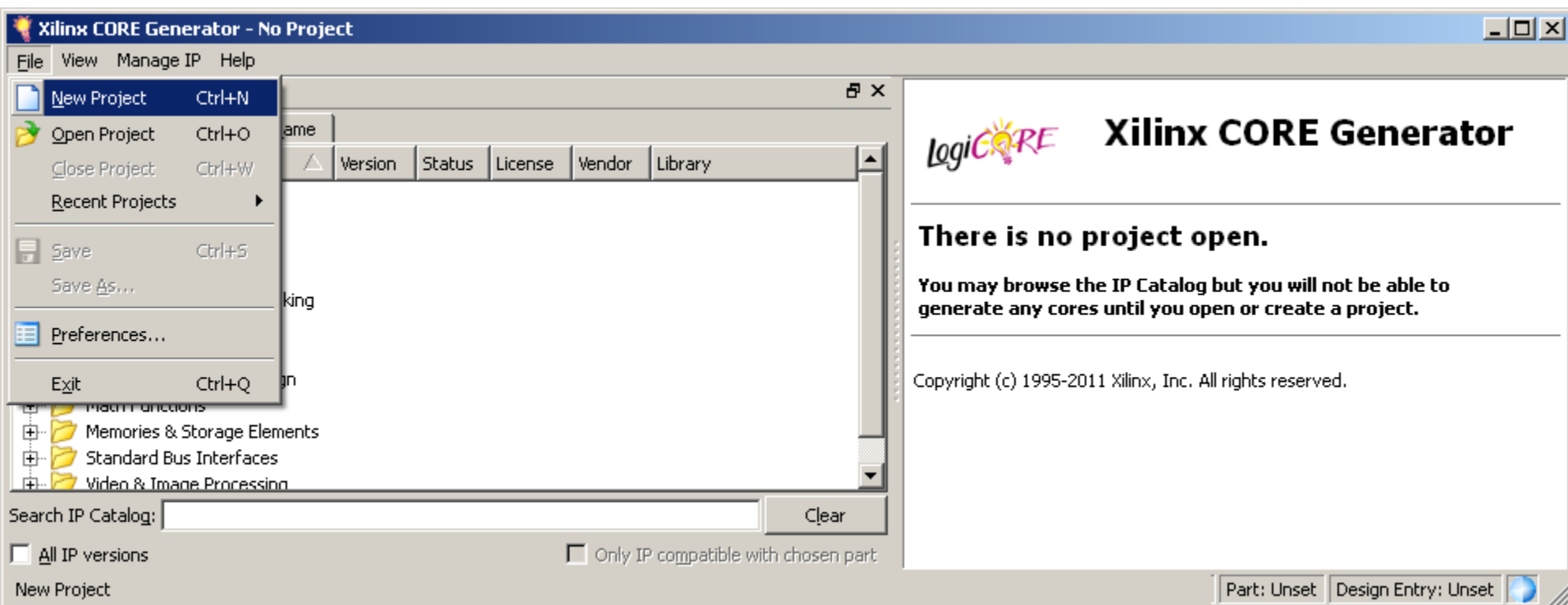


Generate PCIe Core

- **Open the CORE Generator**

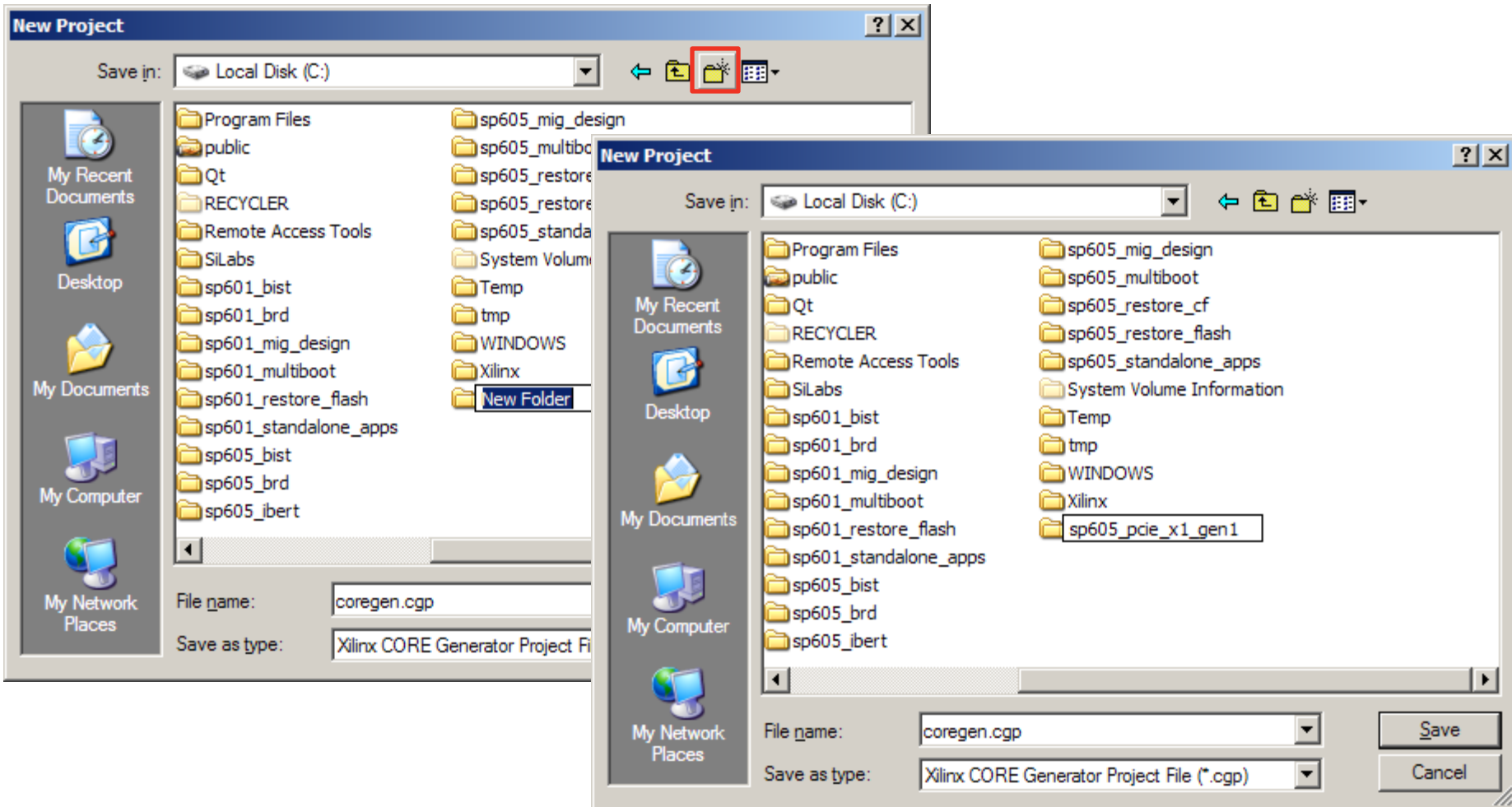
**Start → All Programs → Xilinx ISE Design Suite 13.4 →
ISE Design Tools → Tools → CORE Generator**

- **Create a new project; select File → New Project**



Generate MIG Example Design

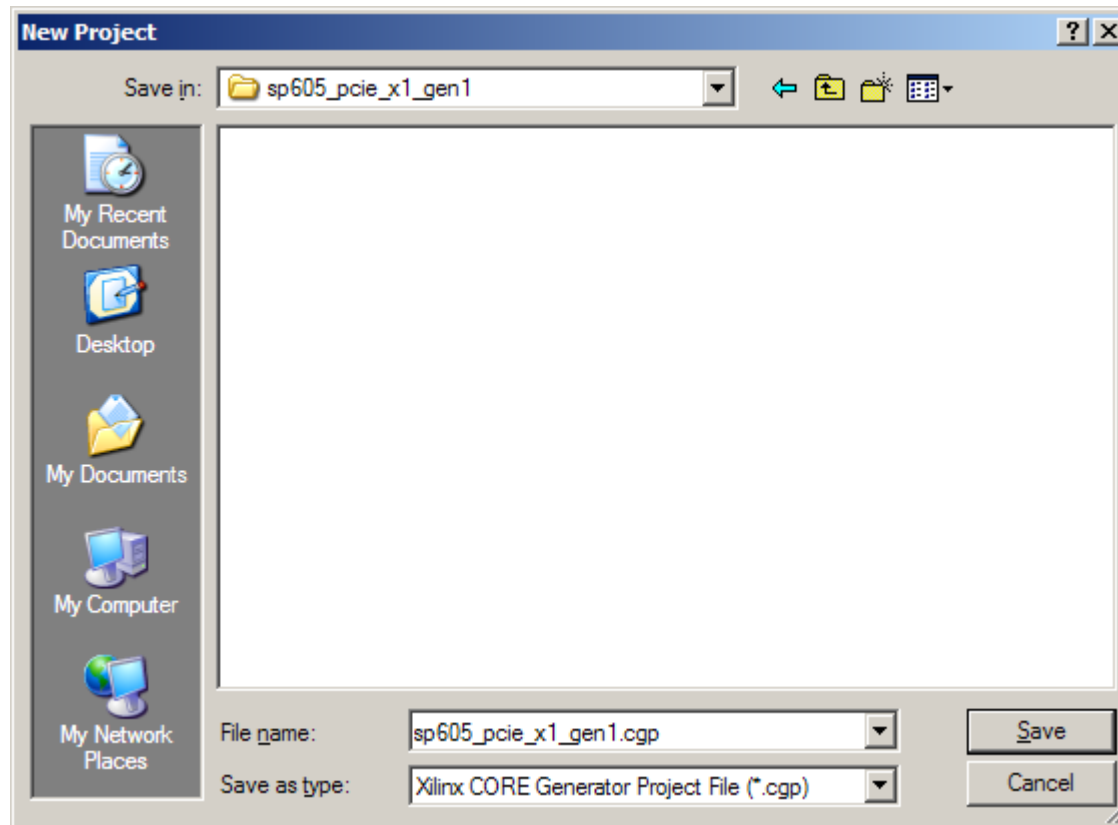
- Create a project directory: `sp605_pcie_x1_gen1`



Note: Presentation applies to the SP605

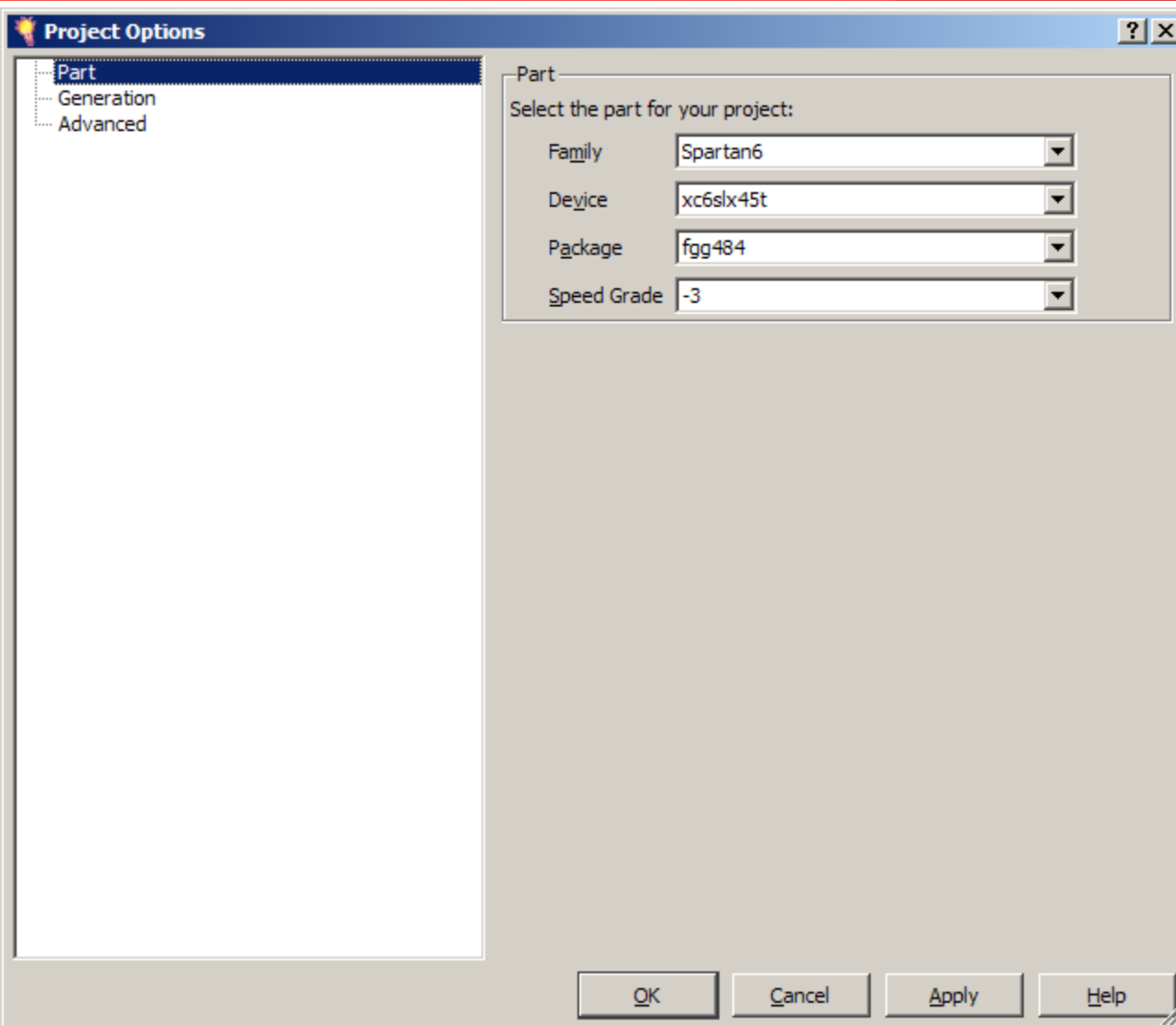
Generate MIG Example Design

- Name the project: sp605_pcie_x1_gen1.cgp



Note: Presentation applies to the SP605

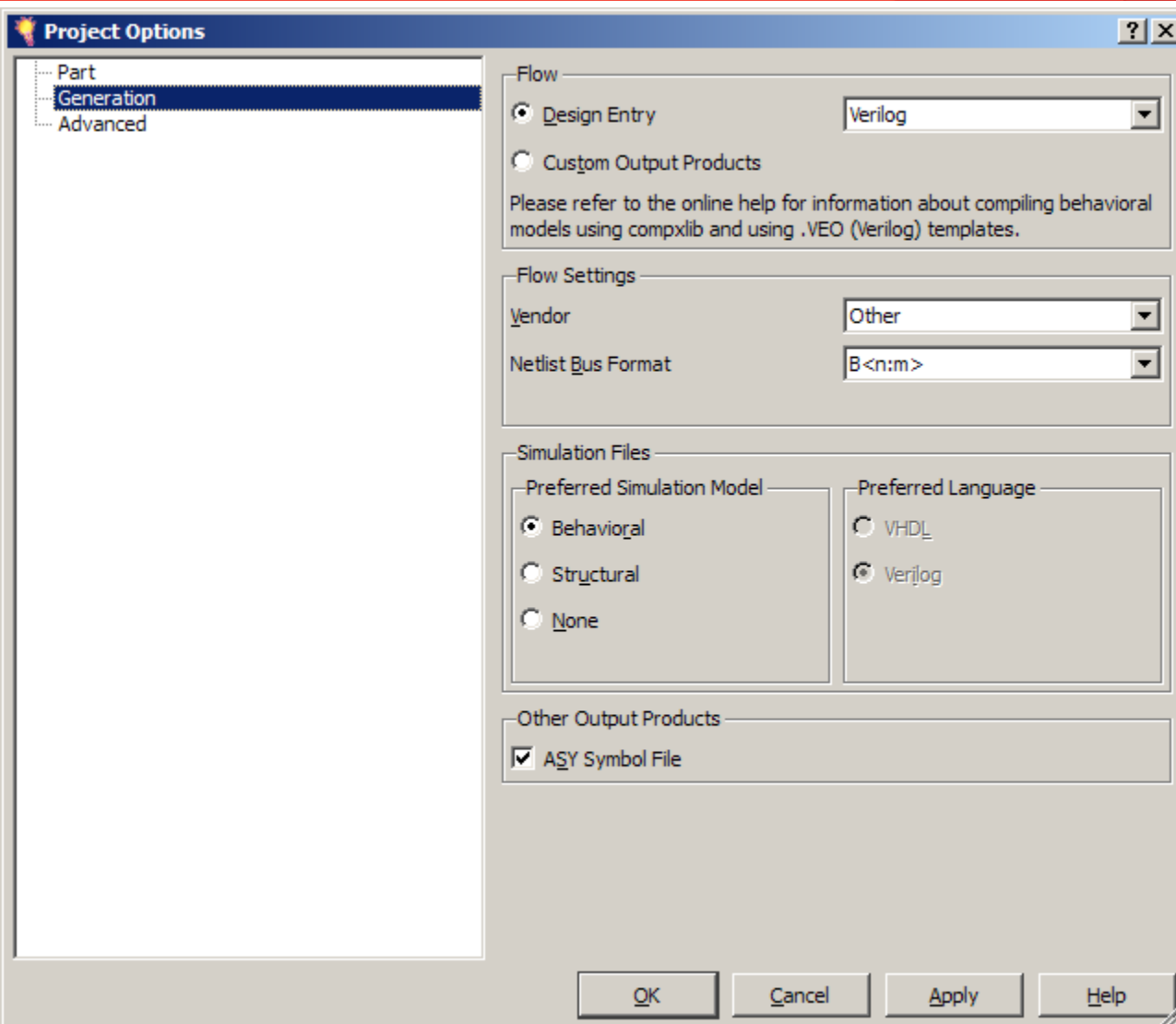
Generate PCIe Core



- The Project options will appear
- Set the Part (as seen here):
 - Family: Spartan6
 - Device: xc6slx45t
 - Package: fgg484
 - Speed Grade: -3
- Select Generation

Note: Presentation applies to the SP605

Generate PCIe Core



- **Under Generation**
 - Set the Design Entry to Verilog
- **Click OK**

Note: Presentation applies to the SP605

Generate PCIe Core

- Right click on the **Spartan-6 Integrated Block for PCI Express, Version 2.4**
 - Select **Customize and Generate**

The screenshot shows the Xilinx CORE Generator interface. The IP Catalog is open, displaying a list of IP blocks. The 'Spartan-6 Integrated Block for PCI Express' is selected, and a context menu is open with 'Customize and Generate' highlighted. The details pane on the right shows the core's name, version (2.4), and status (Production).

Name	Version	Status	License	Vendor	Library
7 Series Integrated Block for PCI Express	1.3			xilinx.com	ip
Endpoint Block Plus for PCI Express	1.15			xilinx.com	ip
Endpoint for PCI Express	3.7			xilinx.com	ip
Endpoint PIPE for PCI Express	1.7			xilinx.com	ip
Endpoint PIPE for PCI Express	1.8			xilinx.com	ip
Spartan-6 Integrated Block for PCI Express					
Spartan-6 Integrated Block for PCI Express					
Virtex-6 Integrated Block for PCI Express					
Virtex-6 Integrated Block for PCI Express					

LogiCORE **Spartan-6 Integrated Block for PCI Express** [Show Project](#)

This core is supported at status **Production** by your chosen part.

Information

Core type: Spartan-6 Integrated Block for PCI Express
Version: 2.4
Identifier: xilinx.com:ip:s6_pcie:2.4
Core Summary: The Xilinx Spartan-6 Integrated Block for PCI Express

Part: xc6slx45t-3fgg484 Design Entry: Verilog

Note: Presentation applies to the SP605

Generate PCIe Core

- Click Next

The screenshot shows a software window titled "Spartan-6 Integrated Block for PCI Express" with a "Documents" path. The window contains the following elements:

- LogiCORE** logo and title: **Spartan-6 Integrated Block for PCI Express**
- Version/URL: `xilinx.com:ip:s6_pcie:2.4`
- Component Name:
- Section: **PCIe Device / Port Type**
- Description: "The Integrated Block for PCI Express allows selection of the Device / Port Type"
- Device / Port Type:
- Navigation buttons at the bottom: [Datasheet](#), [< Back](#), [Page 1 of 9](#), [Next >](#), [Generate](#), [Cancel](#), [Help](#)

Generate PCIe Core

Spartan-6 Integrated Block for PCI Express

Documents

LogiCORE

Base Address Registers

Base Address Registers (BARs) serve two purposes. Initially, they serve as a mechanism for the device to request blocks of address space in the system memory map. After the BIOS or OS determines what addresses to assign to the device, the Base Address Registers are programmed with addresses and the device uses this information to perform address decoding.

BAR 0 Options

Bar0 Type: Memory 64 bit Prefetchable

Size: 1 Megabytes

Value: FFF00000 (Hex)

BAR 1 Options

Bar1 Type: N/A 64 bit Prefetchable

Size: 1 Bytes

Value: 00000000 (Hex)

BAR 2 Options

Bar2 Type: N/A 64 bit Prefetchable

Size: 128 Bytes

Value: 00000000 (Hex)

BAR 3 Options

Bar3 Type: N/A 64 bit Prefetchable

Size: 1 Bytes

Value: 00000000 (Hex)

BAR 4 Options

Bar4 Type: N/A 64 bit Prefetchable

Size: 1 Bytes

Value: 00000000 (Hex)

BAR 5 Options

Bar5 Type: N/A Prefetchable

Size: 1 Kilobytes

Value: 00000000 (Hex)

Expansion ROM Base Address Register

Expansion Rom Size: 2 Kilobytes

Value: 00000000 (Hex)

Datasheet < Back Page 2 of 9 Next > Generate Cancel Help

- **BAR 0**
 - Set to 1 Megabytes
- **BAR 2**
 - Deselect BAR 2
- **Click Next**

Generate PCIe Core

Spartan-6 Integrated Block for PCI Express

Documents

LogiCORE Spartan-6 Integrated Block for PCI Express xilinx.com:ip:s6_pcie:2.4

ID Initial Values

Vendor ID	10EE	Range: 0000..FFFF
Device ID	0007	Range: 0000..FFFF
Revision ID	00	Range: 00..FF
Subsystem Vendor ID	10EE	Range: 0000..FFFF
Subsystem ID	0007	Range: 0000..FFFF

Class Code

Base Class	05	Range: 00..FF
Sub-Class	00	Range: 00..FF
Interface	00	Range: 00..FF
Class Code	050000	(Hex)

Class Code Lookup Assistant

Base Class	Simple communication controllers
Base Class	07h
Sub-Class/Interface Value	Generic XT compatible serial controller
Sub-Class	00h
Interface	00h

Cardbus CIS Pointer

Cardbus CIS Pointer	00000000	Range: 00000000..FFFFFFFF
---------------------	----------	---------------------------

Datasheet < Back Page 3 of 9 Next > Generate Cancel Help

■ Note ID Initial Values

- Vendor ID = **10EE**
- Device ID = **0007**
- Revision ID = **00**
- Subsystem Vendor ID = **10EE**
- Subsystem ID = **0007**

■ Click Next 6 times

Generate PCIe Core

Spartan-6 Integrated Block for PCI Express

Documents

Spartan-6 Integrated Block for PCI Express

xilinx.com:ip:s6_pcie:2.4

Advanced Settings

Transaction Layer Module Advanced Settings

- Trim TLP Digest ECRC
- Pipeline Registers for Transaction Block RAM Buffers:

Advanced Physical Layer Settings

- Force No Scrambling

Xilinx Reference Boards

Generate Xilinx Reference Board specific Design files.

Xilinx Reference Boards:

Reference Clock Frequency

The Integrated Block for PCI Express allows selection of the reference clock frequency

Frequency (MHz):

Transceiver Selection

- Transceiver Location:
- Transceiver Channel:
- Expose Unused Transceiver Ports

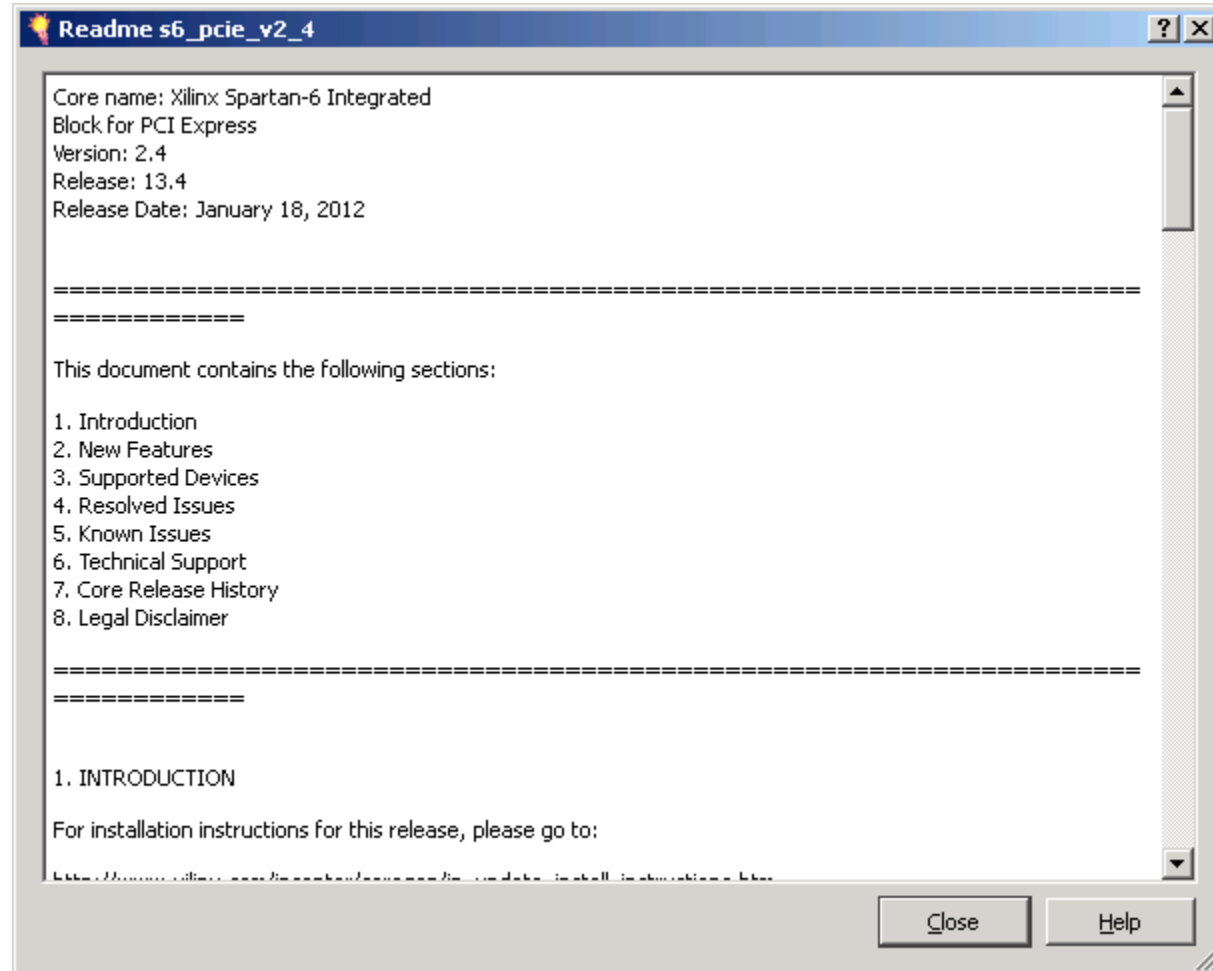
Datasheet

< Back Page 9 of 9 Next > Generate Cancel Help

- On Page 9
 - Select SP605
- Click Generate

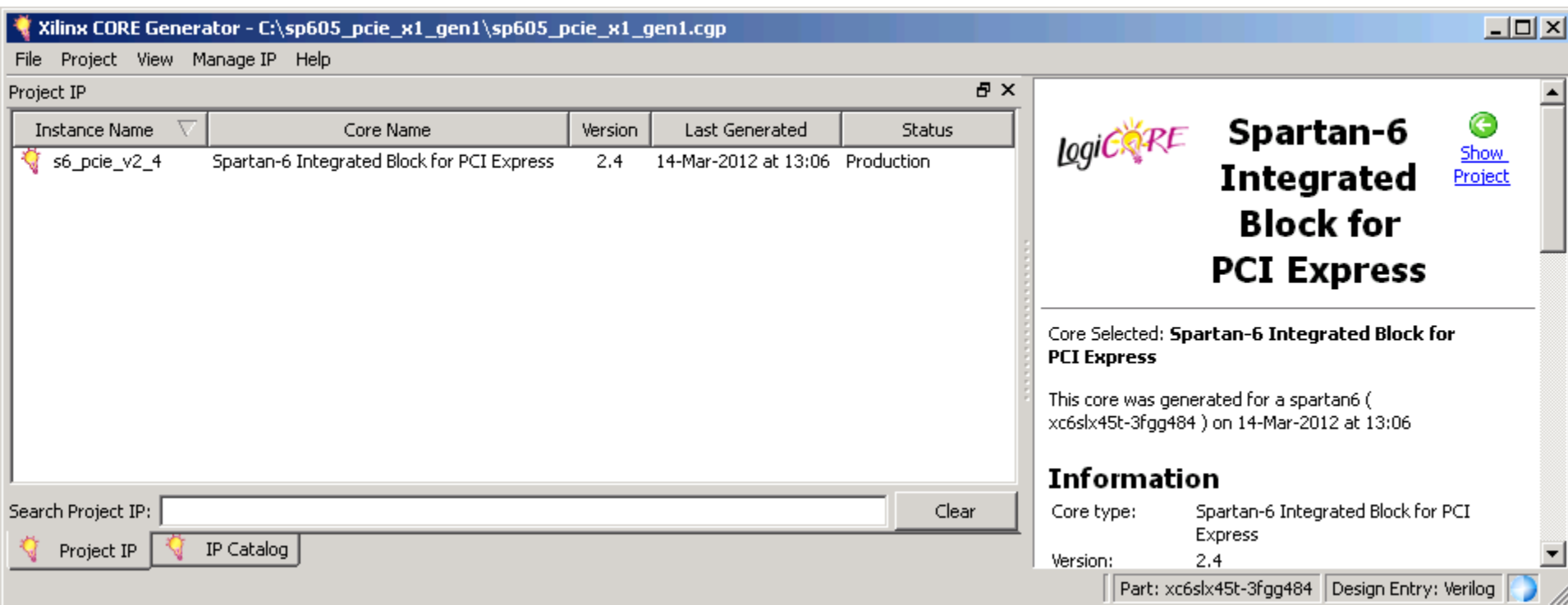
Generate PCIe Core

- After the PCIe core finishes generating, click OK on the Readme File window



Generate PCIe Core

- The s6_pcie_v2_4 IP appears under the Project IP tab



The screenshot shows the Xilinx CORE Generator interface. The title bar reads "Xilinx CORE Generator - C:\sp605_pcie_x1_gen1\sp605_pcie_x1_gen1.cgp". The menu bar includes "File", "Project", "View", "Manage IP", and "Help". The "Project IP" tab is active, displaying a table with the following data:

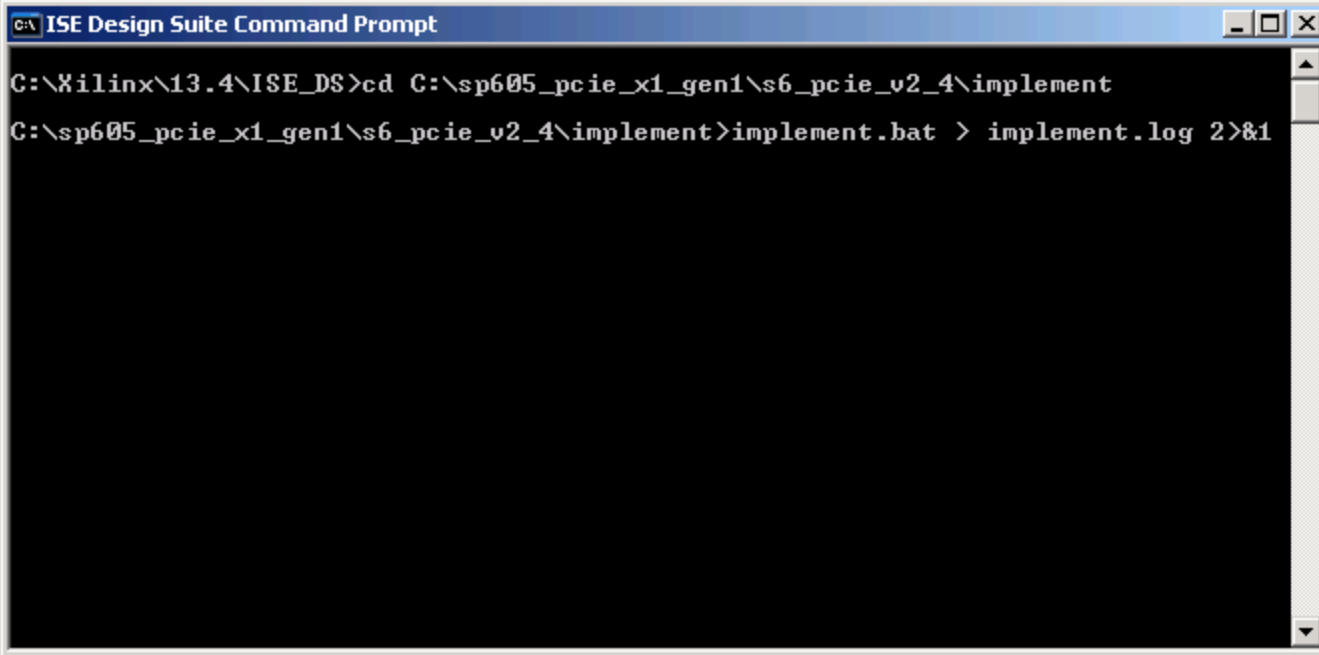
Instance Name	Core Name	Version	Last Generated	Status
s6_pcie_v2_4	Spartan-6 Integrated Block for PCI Express	2.4	14-Mar-2012 at 13:06	Production

Below the table is a "Search Project IP:" field with a "Clear" button. At the bottom left, there are two buttons: "Project IP" (selected) and "IP Catalog". On the right side, a detailed view for the selected IP is shown, featuring the "LogiCORE" logo and the text "Spartan-6 Integrated Block for PCI Express". A "Show Project" link is also present. Below this, it states "Core Selected: Spartan-6 Integrated Block for PCI Express" and "This core was generated for a spartan6 (xc6slx45t-3fgg484) on 14-Mar-2012 at 13:06". An "Information" section lists "Core type: Spartan-6 Integrated Block for PCI Express" and "Version: 2.4". At the bottom right, it shows "Part: xc6slx45t-3fgg484" and "Design Entry: Verilog".

Note: Presentation applies to the SP605

Compile PCIe Core

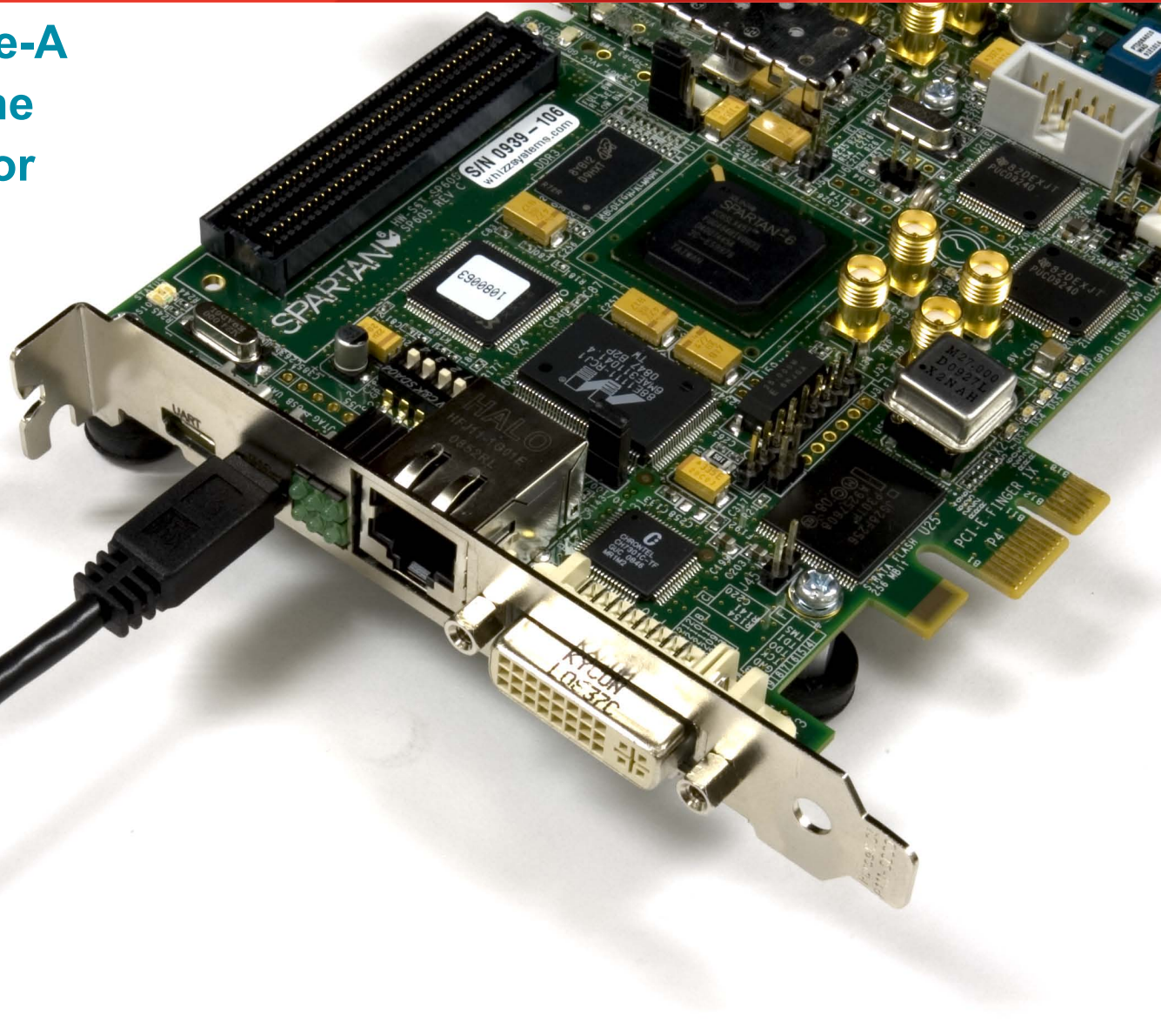
- **Type these commands in an ISE Design Suite Command Prompt:**
`cd C:\sp605_pcie_x1_gen1\s6_pcie_v2_4\implement`
`implement.bat > implement.log 2>&1`



```
C:\Xilinx\13.4\ISE_DS>cd C:\sp605_pcie_x1_gen1\s6_pcie_v2_4\implement
C:\sp605_pcie_x1_gen1\s6_pcie_v2_4\implement>implement.bat > implement.log 2>&1
```

Program SPI Flash with PCIe Design

- Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the SP605 board
 - Connect this cable to your PC



Program SPI Flash with PCIe Design



- Set the mode pins for SPI x4 Flash

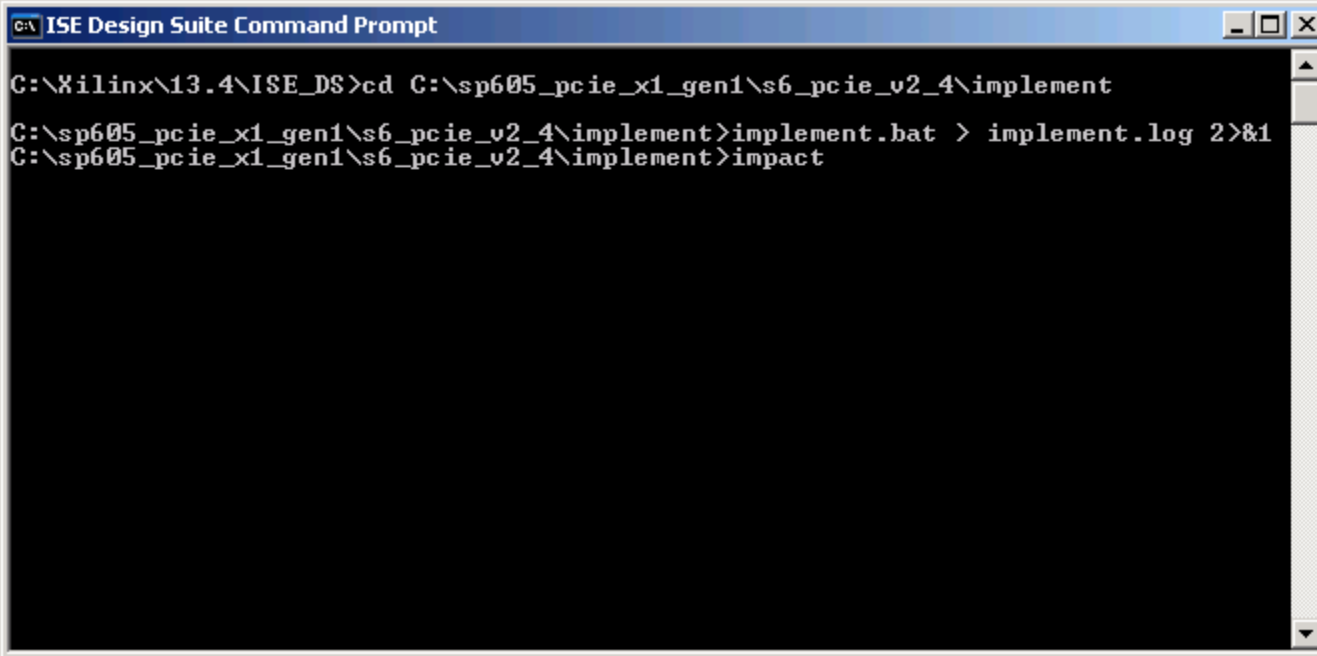
- M0 = 1
- M1 = 0

- Set S1 to 0000

Program SPI Flash with PCIe Design

- **Run iMPACT:**

impact

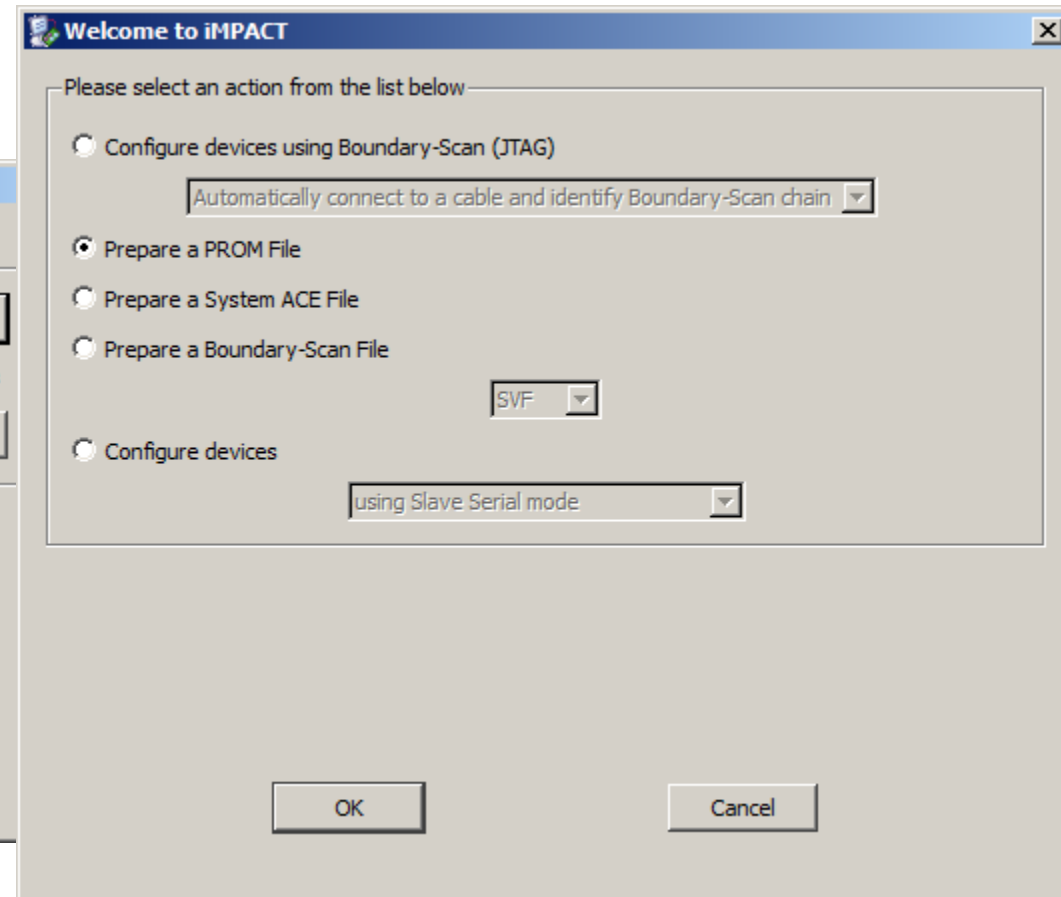
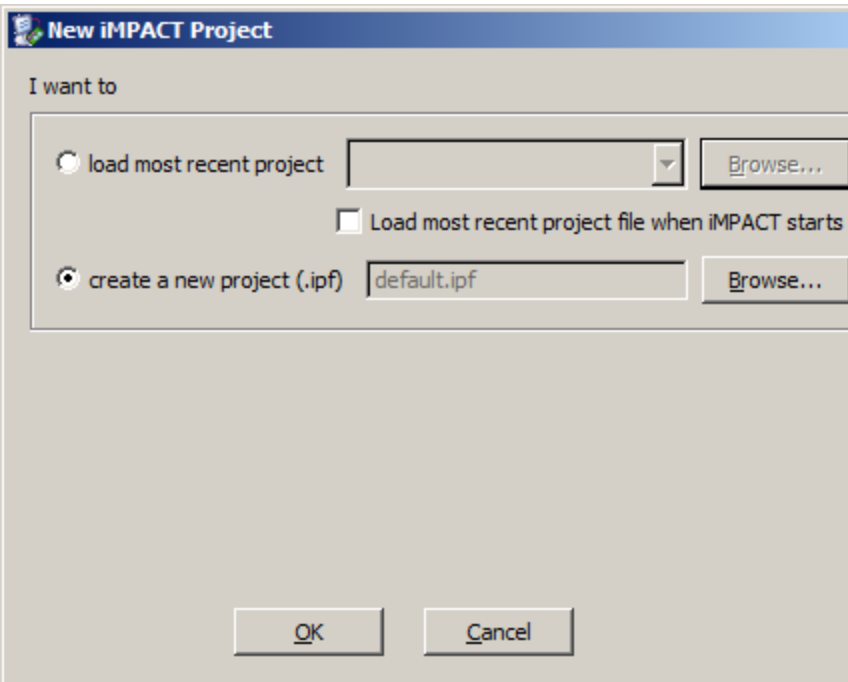


```
C:\Xilinx\13.4\ISE_DS>cd C:\sp605_pcie_x1_gen1\s6_pcie_v2_4\implement
C:\sp605_pcie_x1_gen1\s6_pcie_v2_4\implement>implement.bat > implement.log 2>&1
C:\sp605_pcie_x1_gen1\s6_pcie_v2_4\implement>impact
```

Program SPI Flash with PCIe Design

▪ Select

- Create a new project
- Prepare a PROM File



Program SPI Flash with PCIe Design

- To generate a PROM file for the SPI Flash, select:
 - SPI Flash – Configure Single FPGA

The screenshot displays the PROM File Formatter application window, which is divided into three main steps:

- Step 1. Select Storage Target:** A tree view on the left shows the hierarchy of storage device types. Under "SPI Flash", the option "Configure Single FPGA" is selected and highlighted with a red dashed border. A green arrow points from this selection towards the next step.
- Step 2. Add Storage Device(s):** This section contains two dropdown menus: "Target FPGA" set to "Spartan3E" and "Storage Device (bits)" set to "512K". Below these are "Add Storage Device" and "Remove Storage Device" buttons. A large empty box is provided for listing multiple devices. At the bottom, there is an unchecked checkbox labeled "Auto Select PROM".
- Step 3. Enter Data:** This section contains two tables for configuring file properties and flash data.

General File Detail	Value
Checksum Fill Value	FF
Output File Name	Untitled
Output File Location	C:\Xilinx\12.2\

Flash/PROM File Property	Value
File Format	BIN
Use Power-of-2 for Start Addr	No
Number of Bitstream	2
Bitstream 0 Start Address	0
Bitstream 1 Start Address	675840
Add Non-Configuration Data Files	Yes
Number of Data File	

Program SPI Flash with PCIe Design

- Add 64M

The screenshot shows the PROM File Formatter application window, which is divided into three main sections: Step 1, Step 2, and Step 3.

Step 1. Select Storage Target

Storage Device Type :

- Xilinx Flash/PROM
 - Non-Volatile FPGA
 - Spartan3AN
 - SPI Flash
 - Configure Single FPGA
 - Configure MultiBoot FPGA
 - BPI Flash
 - Configure Single FPGA
 - Configure MultiBoot FPGA
 - Configure from Paralleled PROMs
 - Generic Parallel PROM

A green arrow button is located to the right of the list.

Step 2. Add Storage Device(s)

Storage Device (bits) 64M

Add Storage Device Remove Storage Device

64M

Auto Select PROM

A red box highlights the "Add Storage Device" button. A green arrow button is located to the right of the list.

Step 3. Enter Data

General File Detail	Value
Checksum Fill Value	FF
Output File Name	Untitled
Output File Location	C:\Xilinx\12.2\

Flash/PROM File Property	Value
File Format	BIN
Use Power-of-2 for Start Addr	No
Number of Bitstream	2
Bitstream 0 Start Address	0
Bitstream 1 Start Address	675840
Add Non-Configuration Data Files	Yes
Number of Data File	

A red box highlights the green arrow button to the left of the second table.

Note: Presentation applies to the SP605

Program SPI Flash with PCIe Design

- Set file name and save in <design path>\ready_for_download

The screenshot shows the PROM File Formatter dialog box, which is divided into three steps:

- Step 1. Select Storage Target:** A tree view shows the storage device type hierarchy. Under "SPI Flash", "Configure Single FPGA" is selected. A green arrow points to the right.
- Step 2. Add Storage Device(s):** A "Storage Device (bits)" dropdown is set to "64M". Below it, a list contains "64M". Buttons for "Add Storage Device" and "Remove Storage Device" are present. An "Auto Select PROM" checkbox is at the bottom. A green arrow points to the right.
- Step 3. Enter Data:** Two tables are shown. The first table, "General File Detail", has the following data:

General File Detail	Value
Checksum Fill Value	FF
Output File Name	sp605_pcie_x1_gen1
Output File Location	C:/sp605_pcie_x1_gen1/ready_

The second table, "Flash/PROM File Property", has the following data:

Flash/PROM File Property	Value
File Format	MCS
Add Non-Configuration Data Files	No

Description:

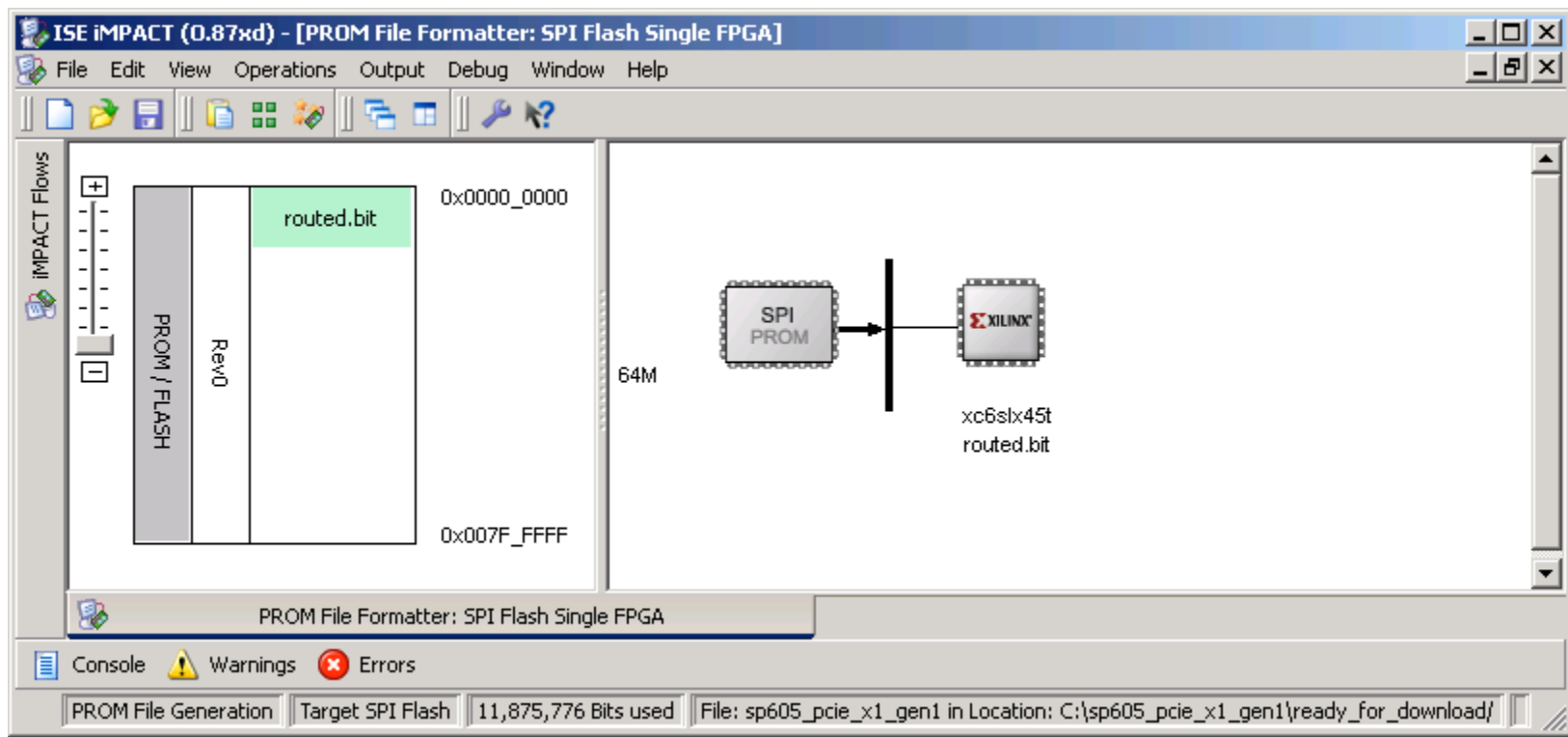
In this step, you will enter information to assist in setting up and generating a PROM file for the targeted storage device and mode.

- **Checksum Fill Value:** When data is insufficient to fill the entire memory of a PROM, the value specified here is used to calculate the checksum of the unused portions.
- **Output File Name:** This allows you to specify the base name of the file to which your PROM data will be written
- **Output File Location:** This allows you to specify the directory in which the file named above will be created

Buttons for "OK", "Cancel", and "Help" are at the bottom right.

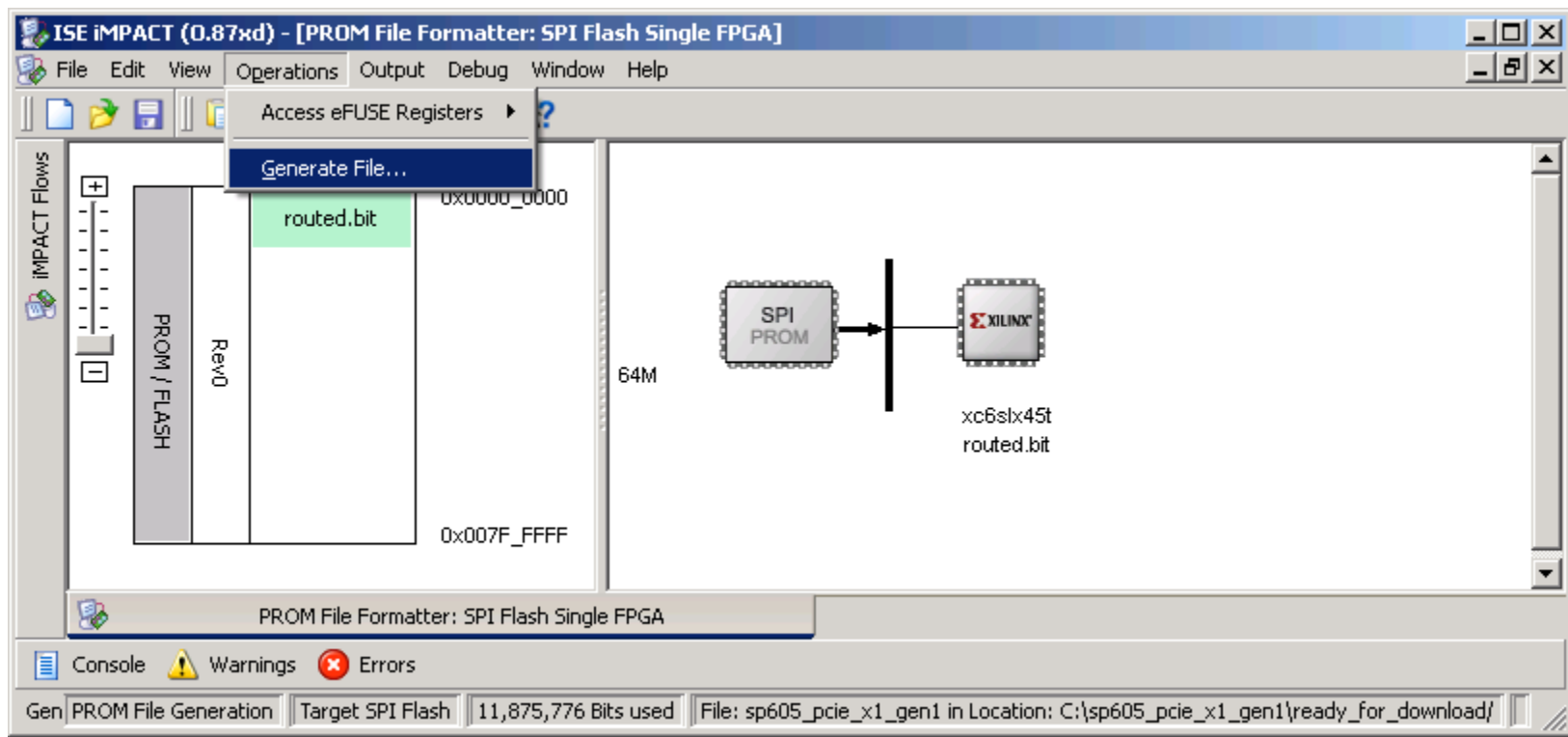
Program SPI Flash with PCIe Design

- Add routed.bit from the <design path>
 \ls6_pcie_v2_4\implement\results



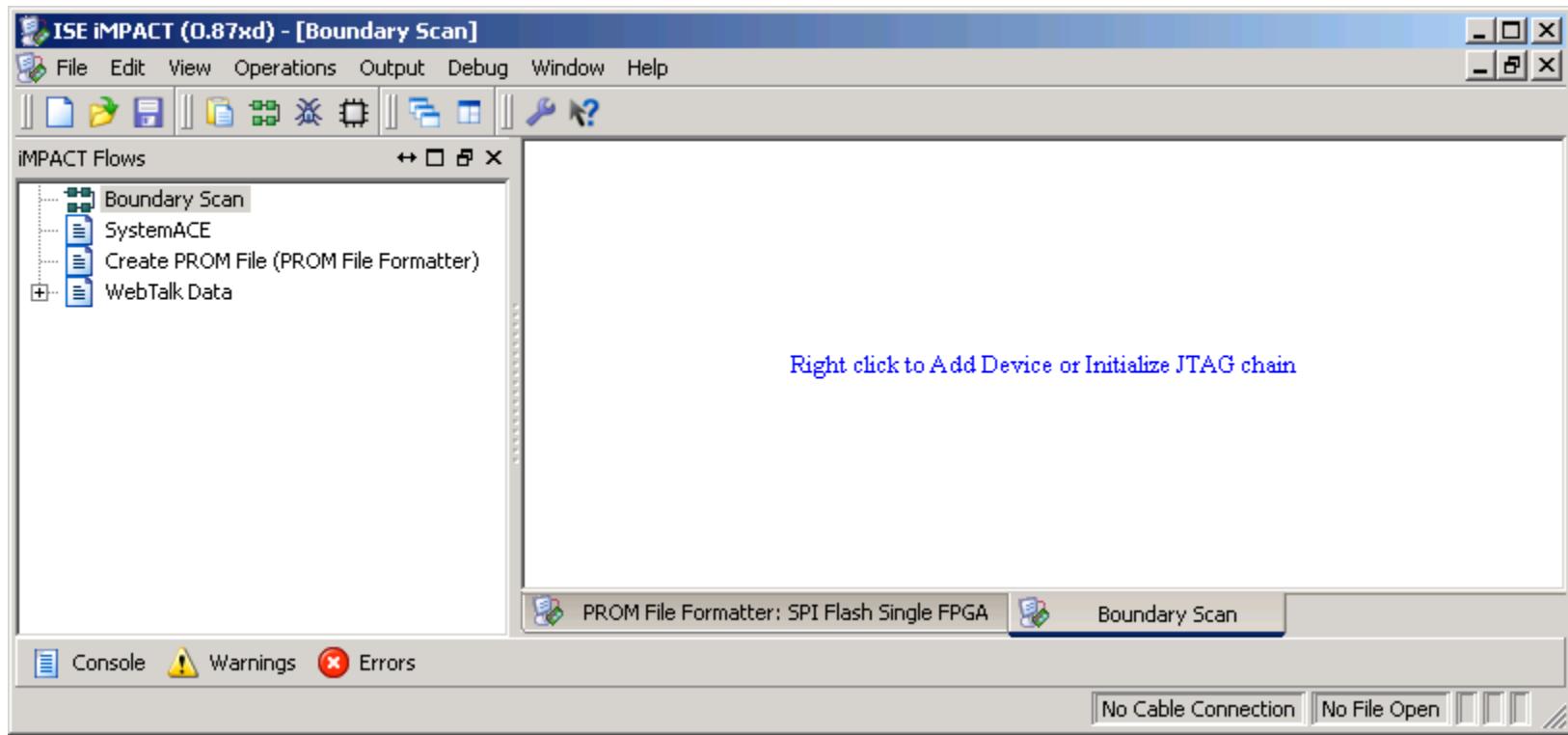
Program SPI Flash with PCIe Design

- From the iMPACT menu, select
Operations → Generate File...



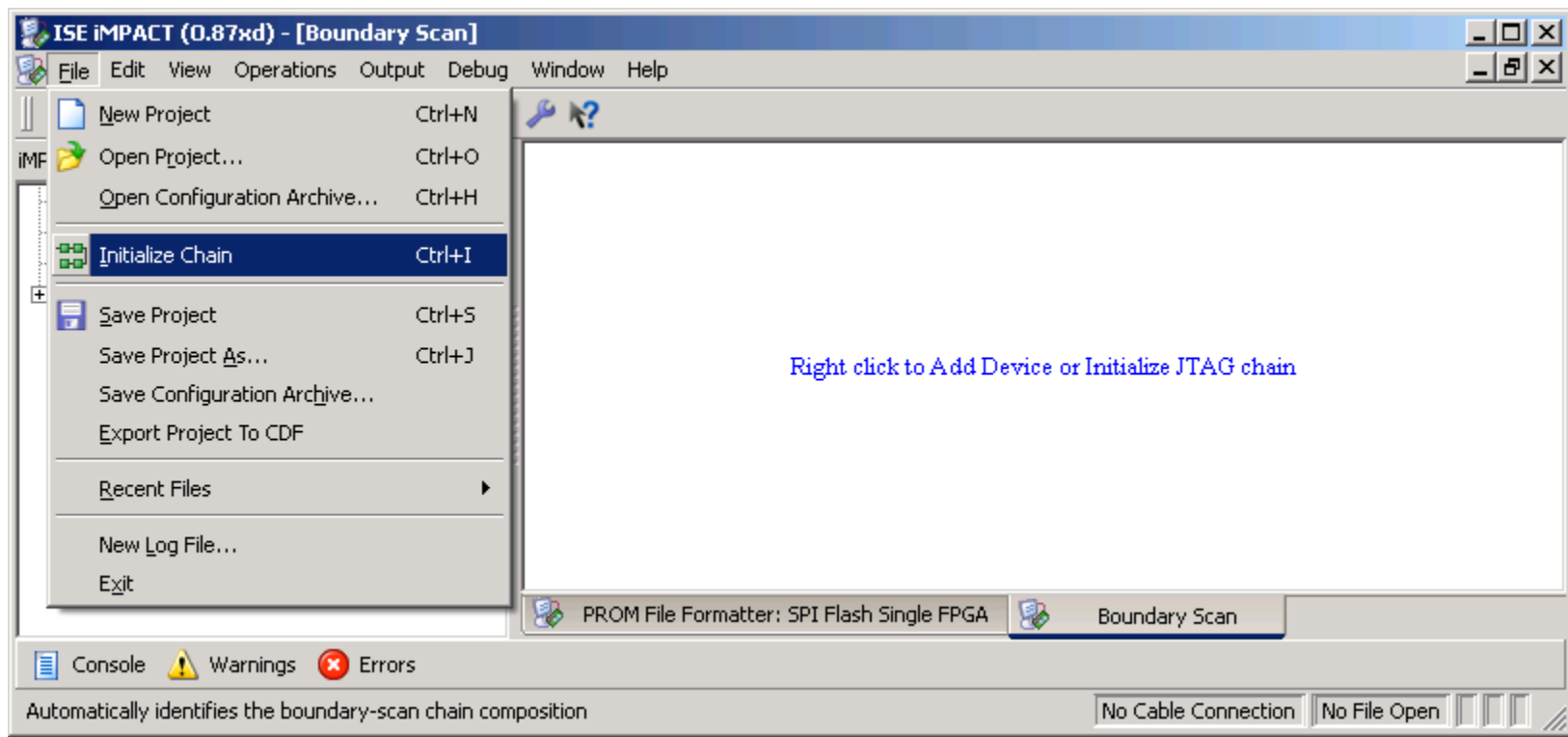
Program SPI Flash with PCIe Design

- After generation completes, under the iMPACT Flows, double click on Boundary Scan



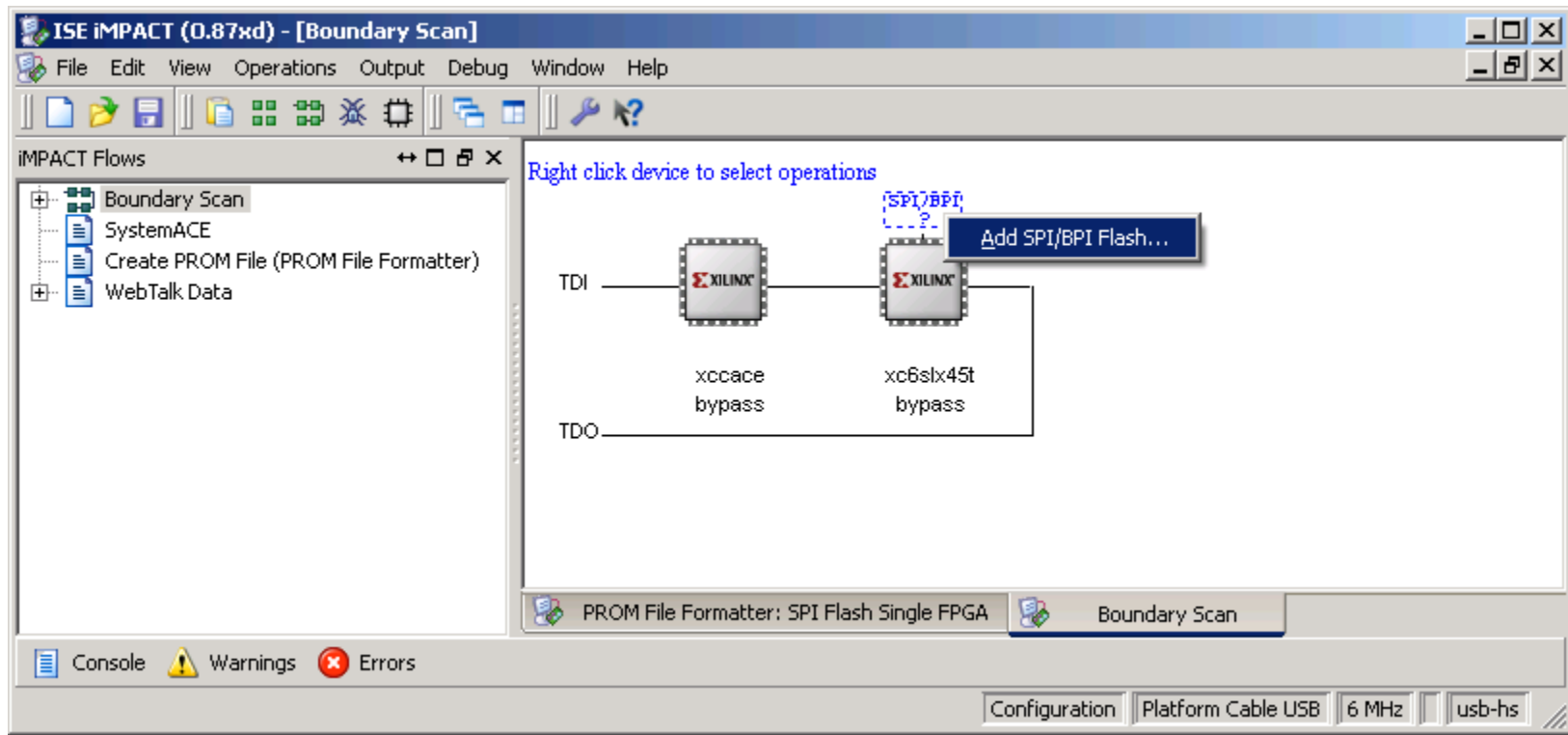
Program SPI Flash with PCIe Design

- From the iMPACT menu, select **File → Initialize Chain**



Program SPI Flash with PCIe Design

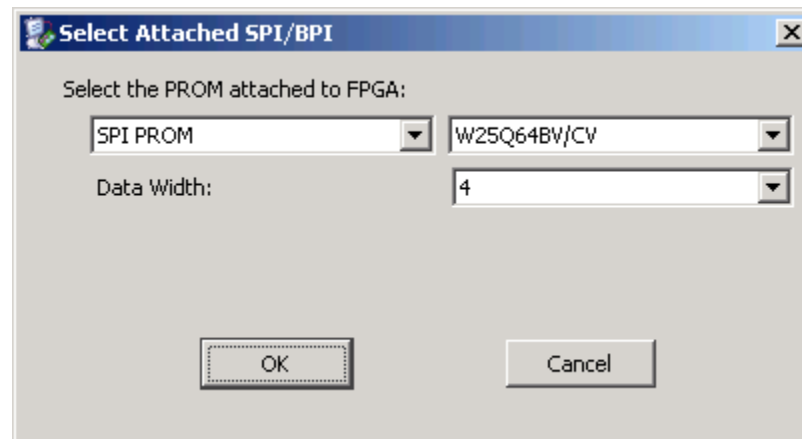
- Right click on the “SPI/BPI ?” box and select Add SPI/BPI Flash...
 - Add <design path>\ready_for_download\sp605_pcie_x1_gen1.mcs



Program SPI Flash with PCIe Design

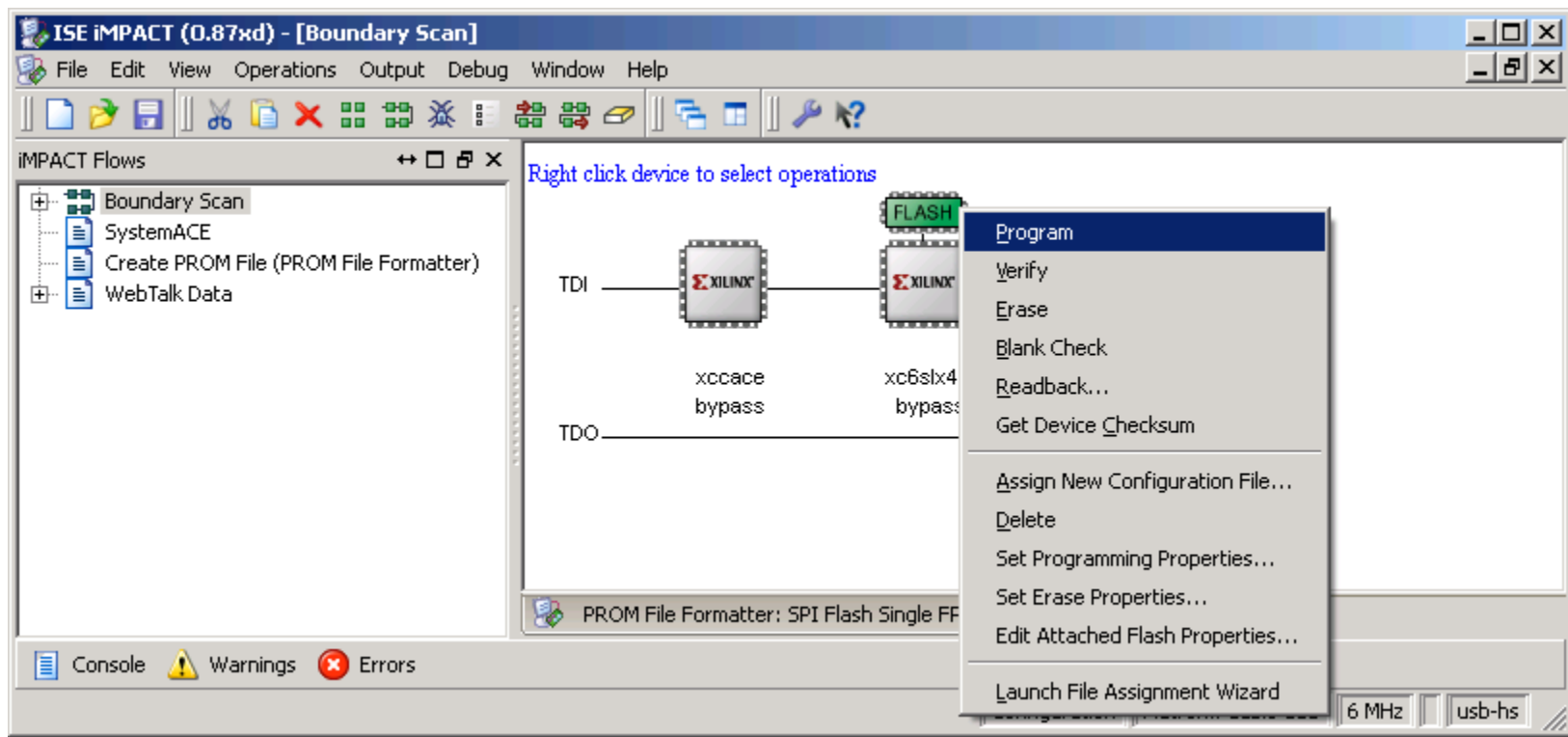
▪ Select

- **SPI PROM**
- **W25Q64BV/CV**
- Data Width: **4**



Program SPI Flash with PCIe Design

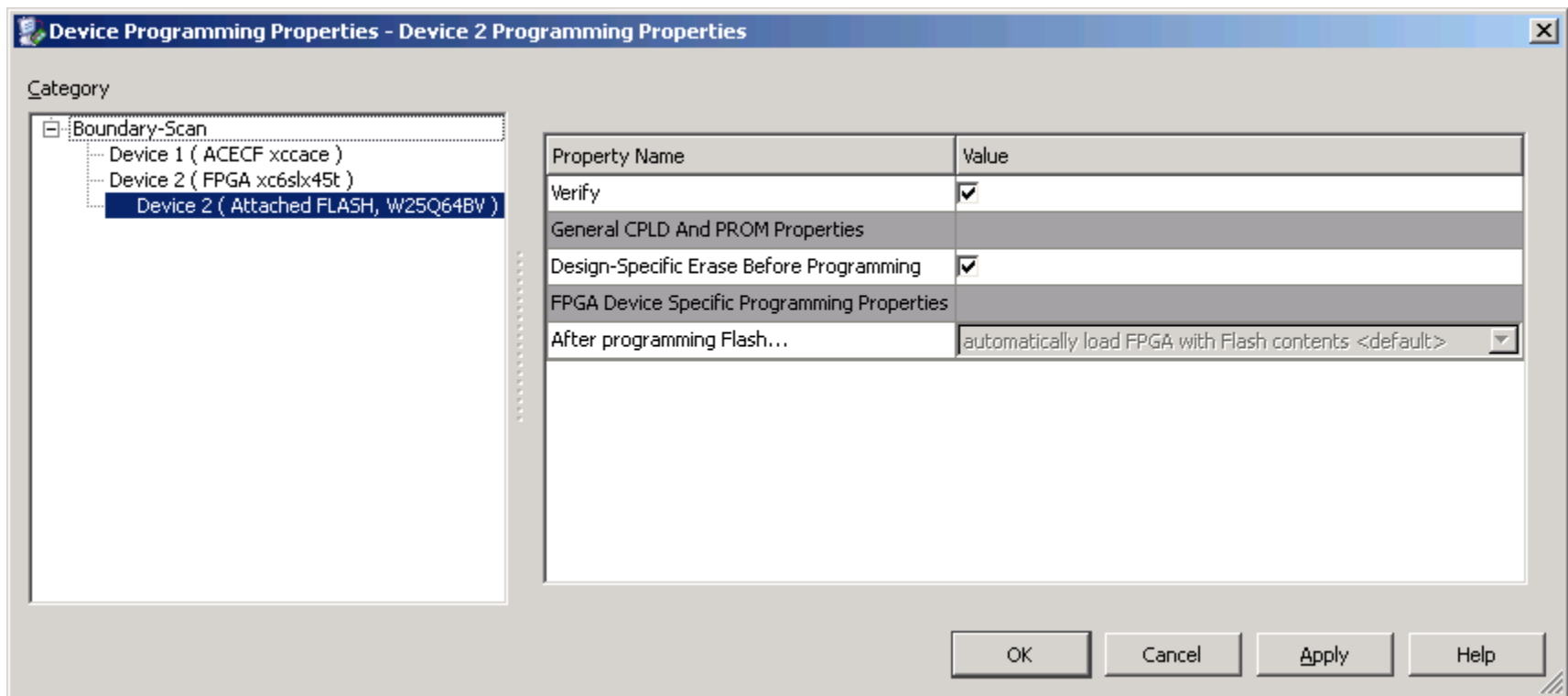
- **Right click on the Flash and select Program**
 - Use default settings to Erase and Verify device



Note: Programming takes about 5 minutes

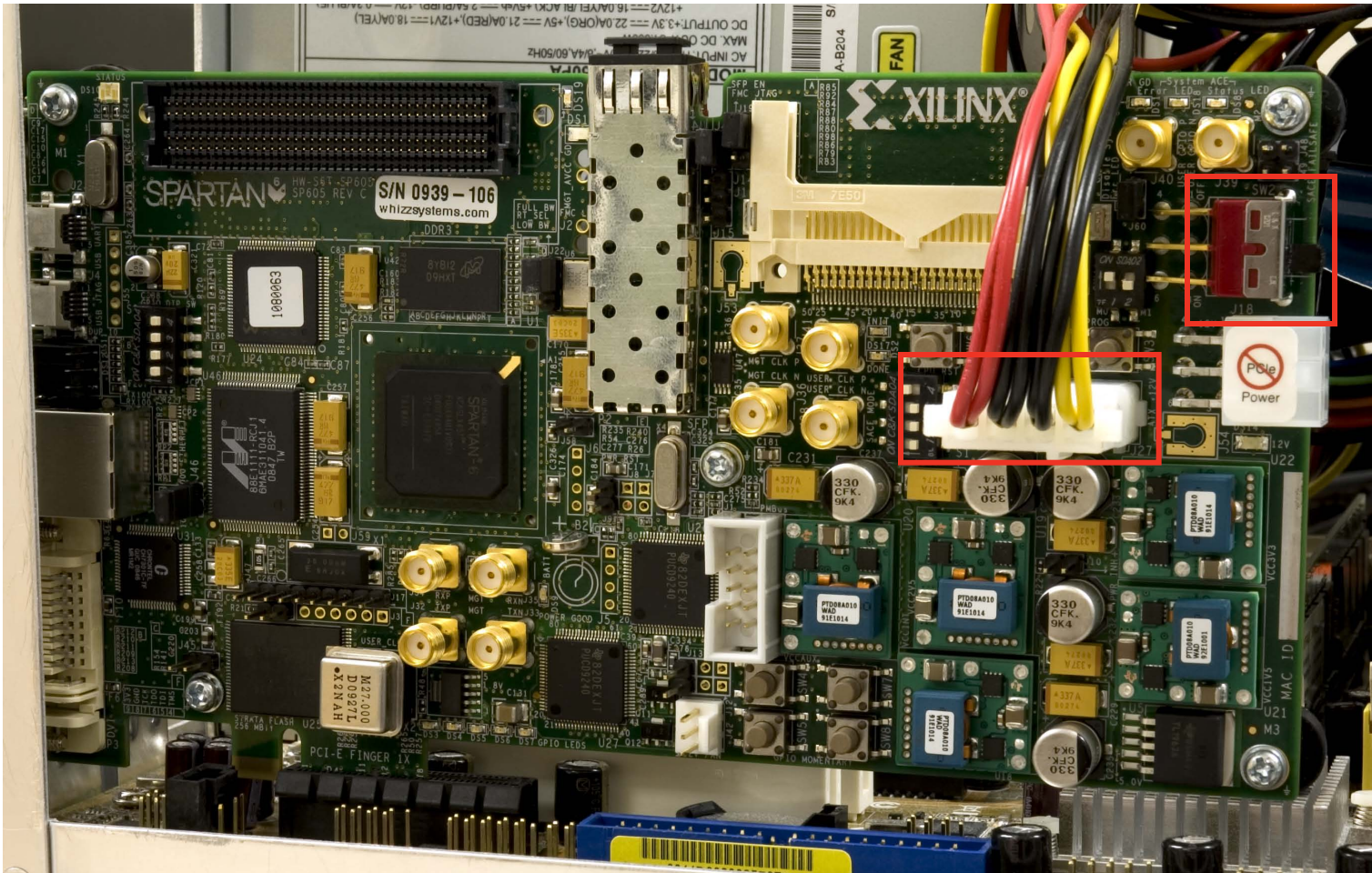
Program SPI Flash with PCIe Design

- Erase Before Programming must be selected



Hardware Setup

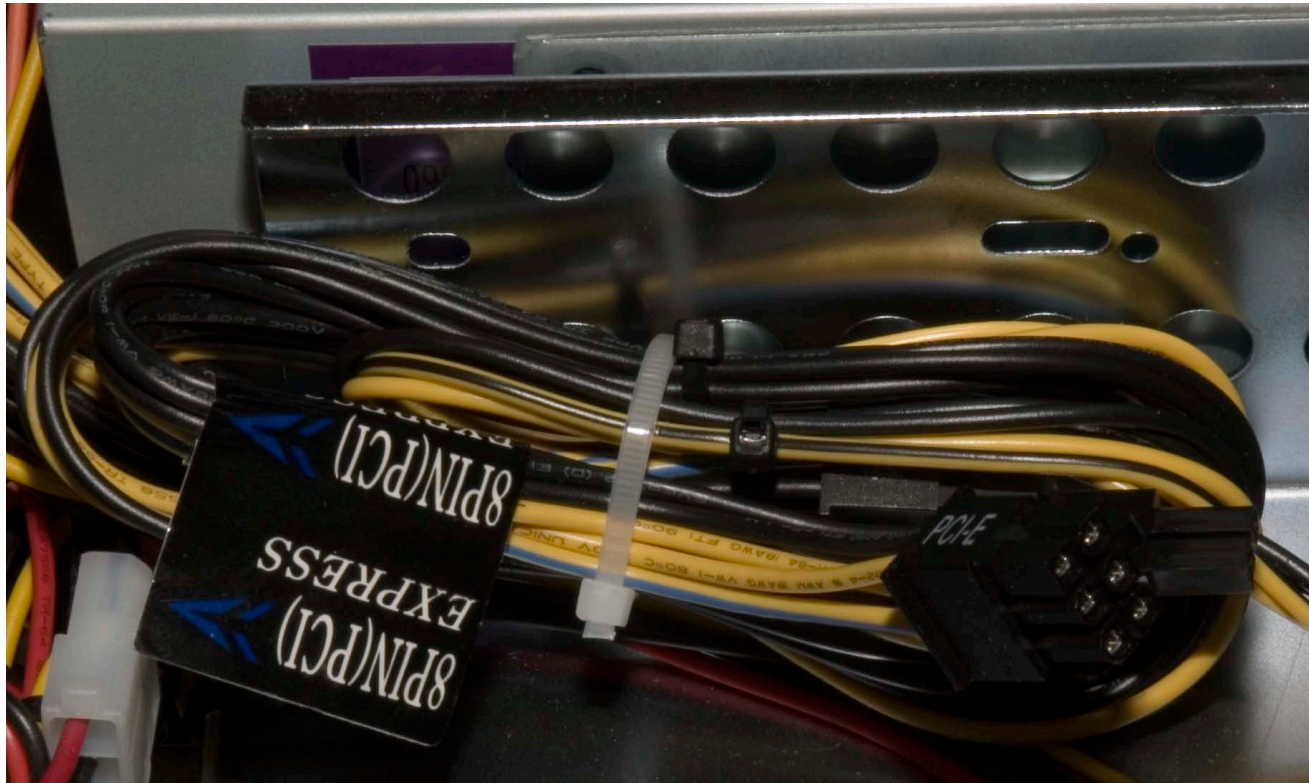
- After programming completes, insert the SP605 Board into a PCIe slot
 - Connect PC power to J27, turn on Power Switch



Note: Presentation applies to the SP605

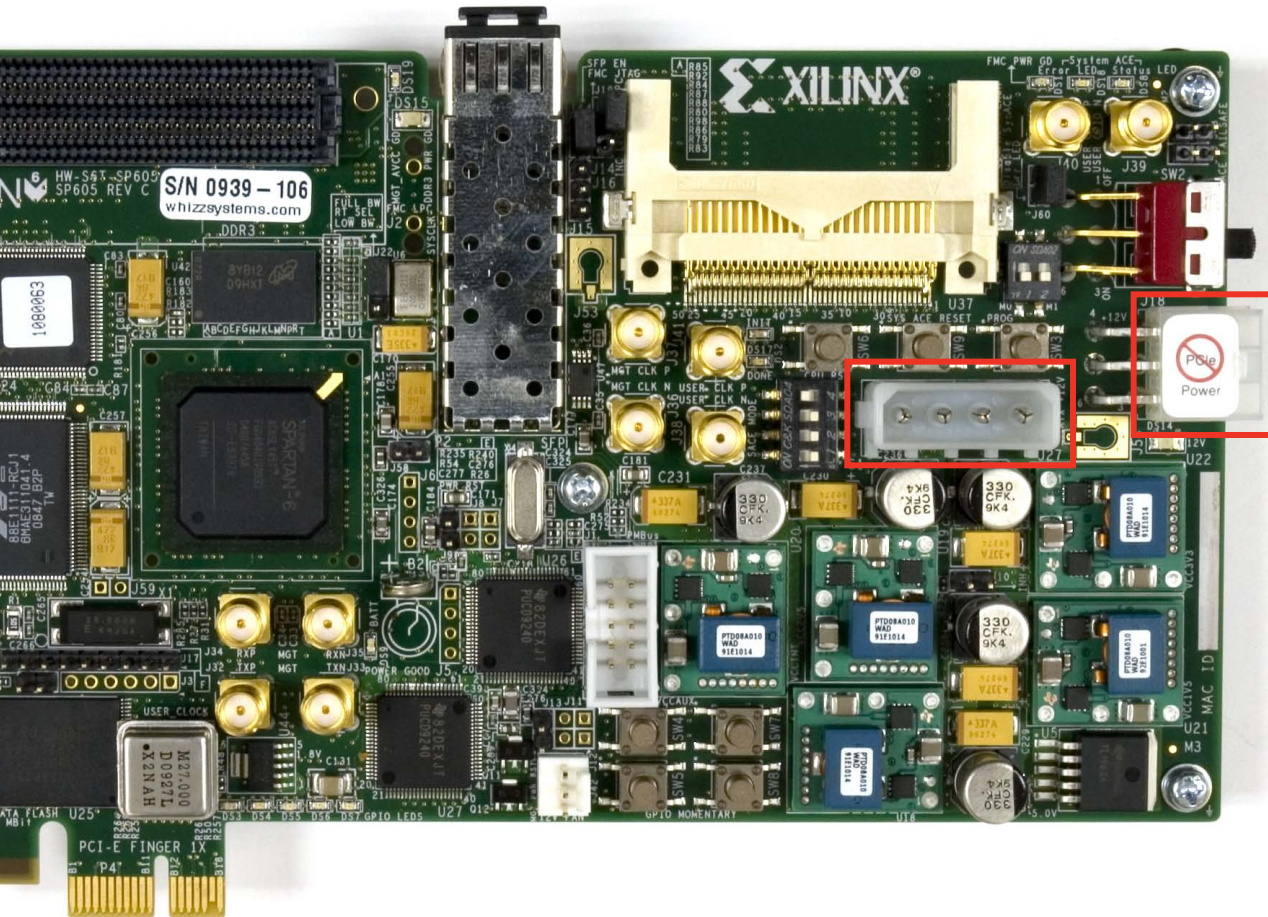
Hardware Setup

- Do *not* use the PCIe connector from the PC power supply



Hardware Setup

- Do not connect both the SP605 power brick connector (J60) and the four pin ATX power connector at the same time



Note: Presentation applies to the SP605


Running the PCIe x1 Gen1 Design

The screenshot shows the PciTree application window. The left pane displays a tree view of PCI devices, with the following visible entries:

- host CPU
 - 0.00.0 Host/PCI; Bridge Device
 - 0.01.0 0->1 (1) PCI/PCI; Bridge Device
 - 0.02.0 VGA; PC Compatible
 - 0.26.0 Universal Host Controller
 - 0.26.1 Universal Host Controller
 - 0.26.7 o. serial bus Device
 - 0.27.0 o. Multimedia 8086
 - 0.28.0 0->4 (4) PCI/PCI; Bridge Device
 - 4.00.0 RAM; Memory Controller
 - 0.28.4 0->3 (3) PCI/PCI; Bridge Device
 - 3.00.0 o. Mass Storage Controller
 - 0.28.5 0->2 (2) PCI/PCI; Bridge Device
 - 2.00.0 Ethernet; Network Controller
 - 0.29.0 Universal Host Controller
 - 0.29.1 Universal Host Controller
 - 0.29.2 Universal Host Controller
 - 0.29.7 o. serial bus Device
 - 0.30.0 0->5 (5) Subtractive; Bridge Device
 - 5.01.0 OpenHCI; IEEE 1394
 - 0.31.0 PCI/ISA; Bridge Device
 - 0.31.2 o. Mass Storage Controller
 - 0.31.3 SMBus; Serial Bus Controller
 - 0.31.5 o. Mass Storage Controller

The right pane shows the configuration details for the selected device (0.00.0):

Host/PCI; Bridge Device
VID: x8086 Intel Corporation
DID: x29A0 no device name found no
SubVID: x1043 Asustek
SubID: x81EA no-name
rev.: x02 no INT

edit ConfReg: [] hex
Nr of ConfRegs: 16 64
 use BIOS int
Write ConfReg
refresh 
 refr after wr. dump:

Config Space Dump: (type 1 xs)

```
29A0 8086 <00 : DID VID
2090 0006 <04 : Stat Cmd
0600 0002 <08 : BaseClass SubClass I
0000 0000 <0C : BIST Header LatTime
0000 0000 <10 : BAR 0
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
81EA 1043 <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 00E0 <34 : reserved
0000 0000 <38 : reserved
0000 0000 <3C : maxLat minGnt IntPir
```

- Power on the PC
- Start PciTree

Running the PCIe x1 Gen1 Design

The screenshot shows the PciTree application window. The left pane displays a tree view of PCI devices, with 0.28.0 selected. The right pane shows the configuration details for the selected device (Host/PCI; Bridge Device). The configuration includes fields for VID, DID, SubVID, and SubID. The 'Nr of ConfRegs' field is set to 64, and the 'refresh dump' button is highlighted with a red box. The 'Config Space Dump' section shows a list of configuration registers and their values.

direct select: bus: 0 dev: 0 func: 0

show INT routing highest busnr: 5 E X I T

show Mem Map About

0.0.0

Host/PCI; Bridge Device

VID: x8086 Intel Corporation
DID: x29A0 no device name found no
SubVID: x1043 Asustek
SubID: x81EA no-name
rev.: x02 no INT


edit ConfReg: hex

Nr of ConfRegs: 16 64

use BIOS int

Write ConfReg

refr after wr.

refresh dump: 

Config Space Dump: (type 1 xs)

```
29A0 8086 <00 : DID VID
2090 0006 <04 : Stat Cmd
0600 0002 <08 : BaseClass SubClass I
0000 0000 <0C : BIST Header LatTime
0000 0000 <10 : BAR 0
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
81EA 1043 <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 00E0 <34 : reserved
0000 0000 <38 : reserved
0000 0000 <3C : maxLat minGnt IntPir
```

- Set Number of Configuration Registers to 64
- Click on Refresh dump

Running the PCIe x1 Gen1 Design

The screenshot shows the PCI Tree utility interface. The left pane displays a tree of PCI devices, with the device at bus 4, device 0, function 0 (ID 4.00.0) selected. The right pane shows the configuration details for this device, which is a RAM; Memory Controller. The configuration details include:

- VID: x10EE Xilinx Corp
- DID: x0007 no device name found no
- SubVID: x10EE Xilinx
- SubID: x0007 no-name
- rev.: x00
- xB<-INTA#

The Config Space Dump (type 1 xs) is also visible, showing the following entries:

```
0007 10EE <00 : DID VID
0010 0007 <04 : Stat Cmd
0500 0000 <08 : BaseClass SubClas:
0000 0008 <0C : BIST Header LatTi
FF60 0000 <10 : BAR 0 mem 32bit
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
0007 10EE <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 010B <3C : maxLat minGnt Int:
7E03 4801 <40 : < dev.specific
```

Locate the Xilinx Device

- Vendor ID is **0x10EE**
- Device ID is **0x0007**

Running the PCIe x1 Gen1 Design

The screenshot shows the PciTree application interface. On the left, a tree view lists various PCI devices. The device at address 0.28.0 (RAM; Memory Controller) is selected. The main window displays the configuration space dump for this device, showing a list of registers and their values. The register at address 0x40 is highlighted in red, indicating it is the current selection.

direct select: bus: 4 dev: 0 func: 0

show INT routing highest busnr: 5

show Mem Map

E X I T

About

4.0.0

RAM; Memory Controller

VID: x10EE Xilinx Corp

DID: x0007 no device name found no

SubVID: x10EE Xilinx

SubID: x0007 no-name

rev.: x00 xB<-INTA#

edit ConfReg: hex

Nr of ConfRegs: 16 64

Write ConfReg

use BIOS int

refresh dump:

refr after wr.

Config Space Dump: (type 1 xs)

```
0010 0007 <04 : Stat Cmd
0500 0000 <08 : BaseClass SubClas:
0000 0008 <0C : BIST Header LatTi
FF60 0000 <10 : BAR 0 mem 32bit
0000 0000 <14 : BAR 1
0000 0000 <18 : BAR 2
0000 0000 <1C : BAR 3
0000 0000 <20 : BAR 4
0000 0000 <24 : BAR 5
0000 0000 <28 : Cardbus_CIS_Ptr
0007 10EE <2C : SubID SubVendorID
0000 0000 <30 : Exp_ROM_BAR
0000 0040 <34 : reserved
0000 0000 <38 : reserved
0000 010B <3C : maxLat minGnt Int:
7E03 4801 <40 : < dev.specific
0000 0008 <44 : < dev.specific
```

- Navigate the linked list in configuration space to locate the PCIe Capabilities Structure
 - See [UG654](#) for details
- With the Xilinx device selected, select Register 0x40
 - Register 0x40 points to the next structure
 - 0x48 is the address of the next structure

Running the PCIe x1 Gen1 Design

The screenshot shows the PciTree application interface. On the left, a tree view lists PCI devices. The device at 4.00.0 is selected. The main window displays the configuration details for this device, including its VID (x10EE Xilinx Corp), DID (x0007), and SubID (x10EE Xilinx). The configuration register address is set to 0x00805805. The Config Space Dump shows the register at 0080:5805:48.

```
4.00.0 RAM; Memory Controller
  VID: x10EE Xilinx Corp
  DID: x0007 no device name found no
  SubVID: x10EE Xilinx
  SubID: x0007 no-name
  rev.: x00 xB<-INTA#
  edit ConfReg: [x00805805] hex
  Write ConfReg
  [ ] refr after wr.
  Nr of ConfRegs: [16] [64]
  [ ] use BIOS int
  refresh dump: [smiley face]
```

Config Space Dump: (type 1 xs)

7E03	4801	<40	: <	dev.specific
0000	0008	<44	: <	dev.specific
0080	5805	<48	: <	dev.specific
0000	0000	<4C	: <	dev.specific
0000	0000	<50	: <	dev.specific
0000	0000	<54	: <	dev.specific
0001	0010	<58	: <	dev.specific
0000	8FC2	<5C	: <	dev.specific
0000	2810	<60	: <	dev.specific
0003	F411	<64	: <	dev.specific
0011	0000	<68	: <	dev.specific
0000	0000	<6C	: <	dev.specific
0000	0000	<70	: <	dev.specific
0000	0000	<74	: <	dev.specific
0000	0000	<78	: <	dev.specific
0000	0000	<7C	: <	dev.specific
0000	0000	<80	: <	dev.specific

■ Select Register 0x48

- Register 0x48 points to the next structure
- 0x58 is the address of the next structure

Running the PCIe x1 Gen1 Design

direct select: bus: 4 dev: 0 func: 0

show INT routing highest busnr: 5 E X I T

show Mem Map About

4.0.0

RAM; Memory Controller

VID: x10EE Xilinx Corp

DID: x0007 no device name found no

SubVID: x10EE Xilinx

SubID: x0007 no-name

rev.: x00 xB<-INTA#

edit ConfReg: x00010010 hex

Nr of ConfRegs: 16 64

use BIOS int

Write ConfReg

refresh dump: 😊

refr after wr.

Config Space Dump: (type 1 xs)

7E03	4801	<40	: < dev.specific
0000	0008	<44	: < dev.specific
0080	5805	<48	: < dev.specific
0000	0000	<4C	: < dev.specific
0000	0000	<50	: < dev.specific
0000	0000	<54	: < dev.specific
0001	0010	<58	: < dev.specific
0000	8FC2	<5C	: < dev.specific
0000	2810	<60	: < dev.specific
0003	F411	<64	: < dev.specific
0011	0000	<68	: < dev.specific
0000	0000	<6C	: < dev.specific
0000	0000	<70	: < dev.specific
0000	0000	<74	: < dev.specific
0000	0000	<78	: < dev.specific
0000	0000	<7C	: < dev.specific
0000	0000	<80	: < dev.specific

++ -- rescan write to reset PCIbus file bridge

Register 0x58

- 0x58 is a type 0x10, indicating PCIe Capabilities Structure
- Last Structure

Running the PCIe x1 Gen1 Design

direct select: bus: 4 dev: 0 func: 0

show INT routing highest busnr: 5

show Mem Map

E X I T

About

4.0.0

RAM; Memory Controller

VID: x10EE Xilinx Corp

DID: x0007 no device name found no

SubVID: x10EE Xilinx

SubID: x0007 no-name

rev.: x00 xB<-INTA#

edit ConfReg: hex

Nr of ConfRegs: 16 64

Write ConfReg

use BIOS int

refresh dump:

Config Space Dump: (type 1 xs)

7E03	4801	<40	: <	dev.specific
0000	0008	<44	: <	dev.specific
0080	5805	<48	: <	dev.specific
0000	0000	<4C	: <	dev.specific
0000	0000	<50	: <	dev.specific
0000	0000	<54	: <	dev.specific
0001	0010	<58	: <	dev.specific
0000	8FC2	<5C	: <	dev.specific
0000	2810	<60	: <	dev.specific
0003	F411	<64	: <	dev.specific
0011	0000	<68	: <	dev.specific
0000	0000	<6C	: <	dev.specific
0000	0000	<70	: <	dev.specific
0000	0000	<74	: <	dev.specific
0000	0000	<78	: <	dev.specific
0000	0000	<7C	: <	dev.specific
0000	0000	<80	: <	dev.specific

Register 0x64

- Link Capabilities Register
- Indicates the maximum number of lanes and speed (Gen1, Gen2) for device
- The value 0x11 shows this is an x1 Gen1 device

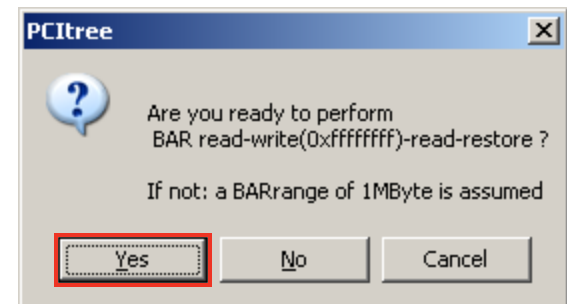
Link Status Register

- 0x68
- Shows the current link status
- This design trained to x1 Gen1 (1)

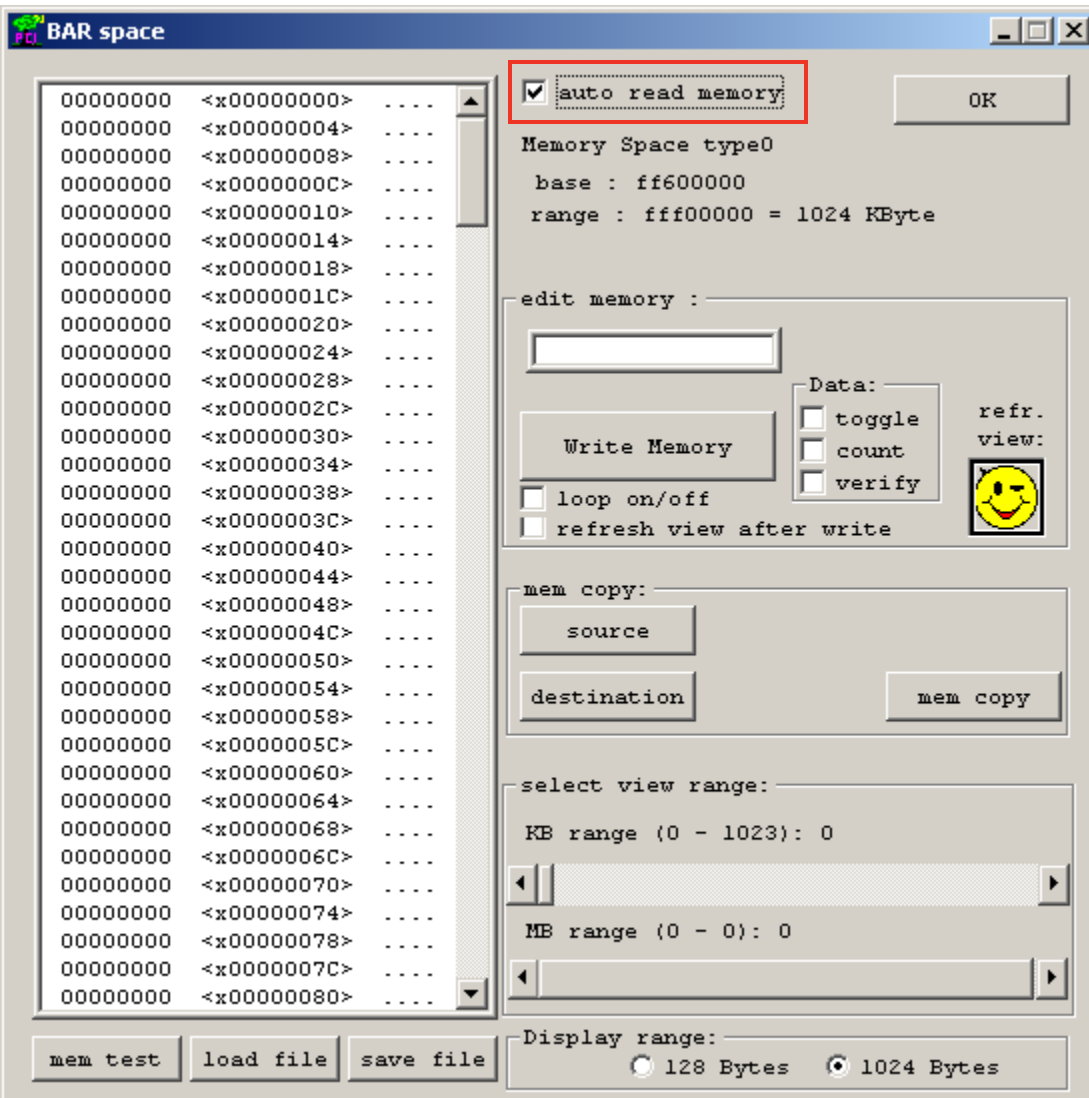
Running the PCIe x1 Gen1 Design

The screenshot shows the PCItree application interface. On the left, a tree view displays the PCI hierarchy, with the path 0.28.0 > 4.00.0 selected. The main window displays the configuration details for the selected device (4.00.0). The configuration includes fields for VID (x10EE Xilinx Corp), DID (x0007), SubVID (x10EE Xilinx), and SubID (x0007). The configuration register address is set to xFF600000. The configuration register dump shows the BAR 0 configuration: FF60 0000 <10 : BAR 0 mem 32bit.

- **Double-click on BAR 0**
 - BAR 0 Address is machine dependent
- **Click Yes on the Dialog box seen below**

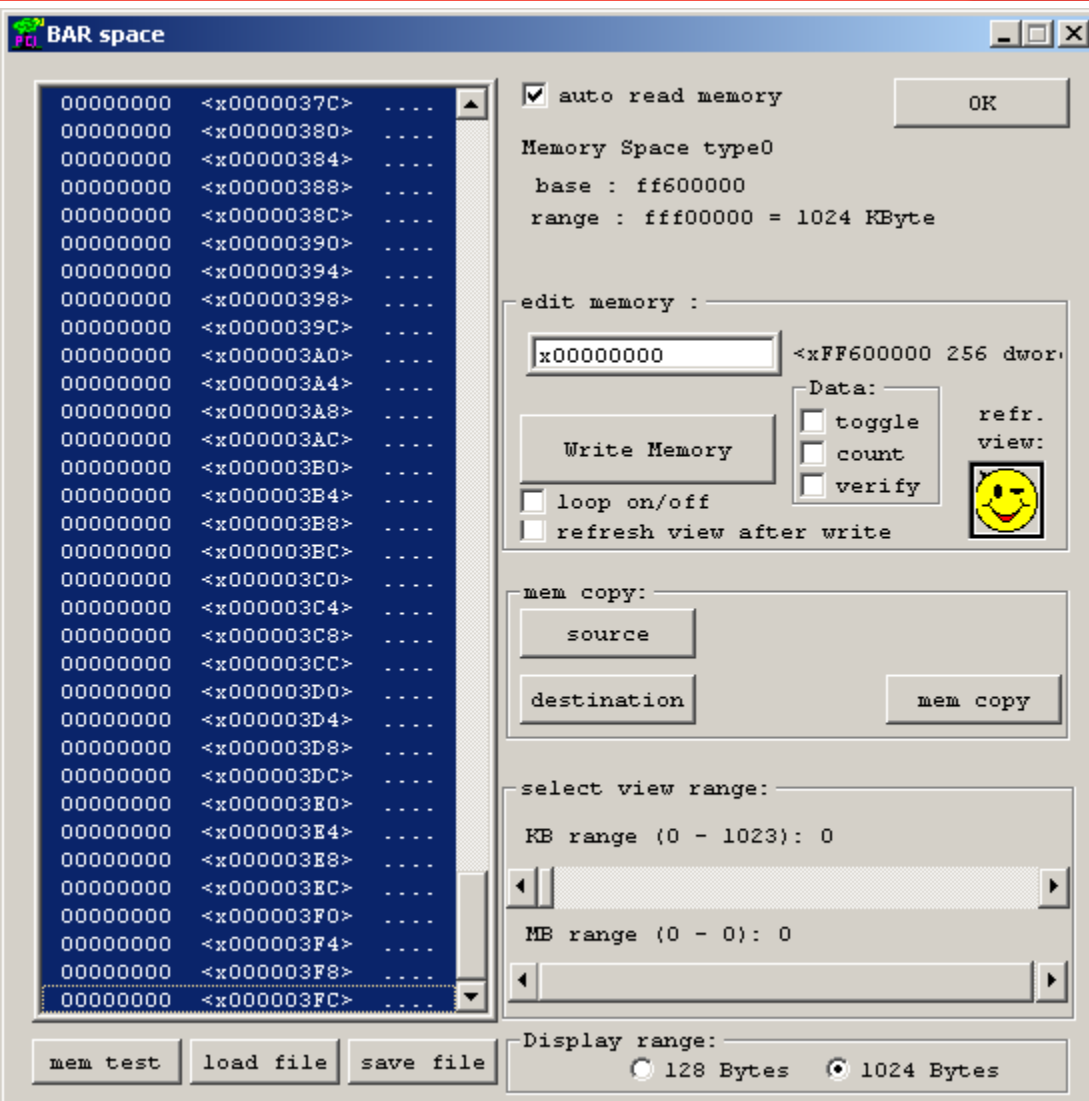


Running the PCIe x1 Gen1 Design



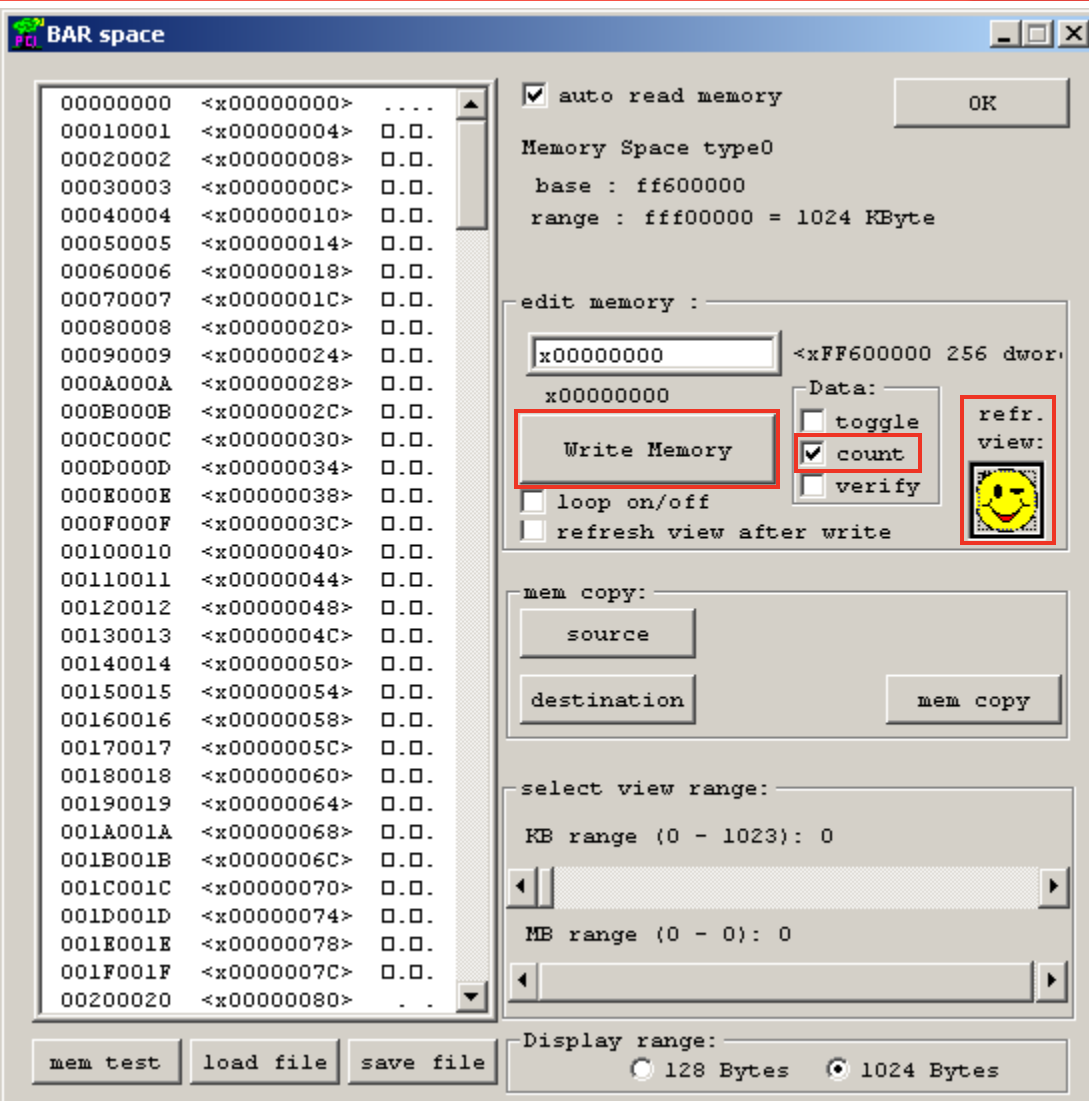
- Select auto read memory

Running the PCIe x1 Gen1 Design



- Click on the first memory location
 - Type <Shift-End> to select 1024 Bytes

Running the PCIe x1 Gen1 Design

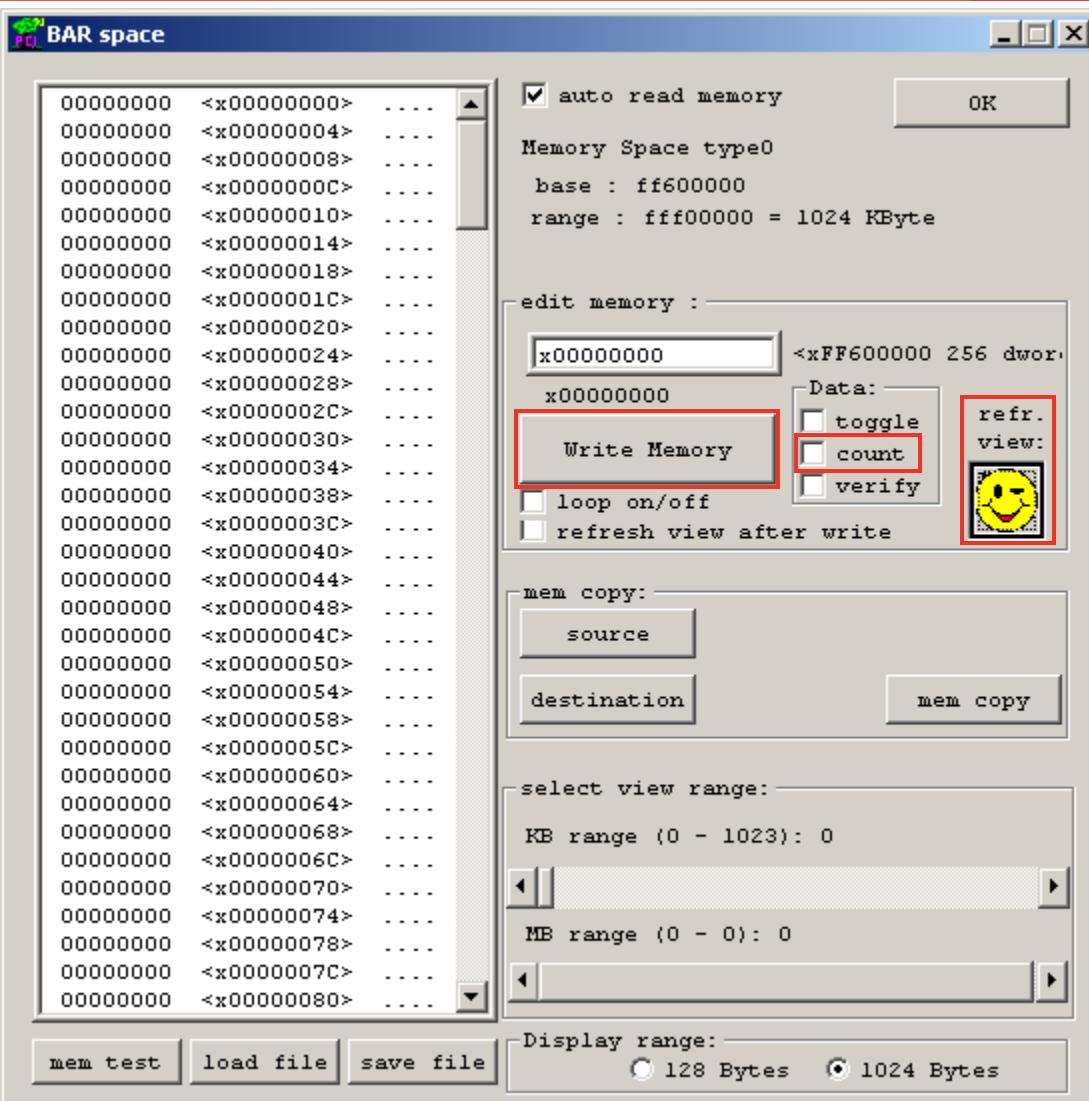


Write Memory

- Select count
- Click Write Memory
- Click refr view

View results – counting up to FF

Running the PCIe x1 Gen1 Design



Restore Memory

- Deselect count
- Click Write Memory
- Click refr view

Memory is reset to zeros

Spartan-6 PCIe x1 Gen1 Capability

- **SP605 Supports PCIe Gen1 Capability**
 - x1 Gen1 lane width
- **LogiCORE PIO Example Design**
 - RDF0035.zip
 - Available through <http://www.xilinx.com/sp605>
- **LogiCORE Integrated Block for PCI Express**
 - See [UG654](#) for details

References

References

- **PCIe Base Specification**

- PCI SIG Web Site

<http://www.pcisig.com/home>

- **Spartan-6 PCIe**

- PCIe Product Overview

http://www.xilinx.com/products/intellectual-property/S6_PCI_Express_Block.htm

- Spartan-6 FPGA Integrated Block for PCI Express User Guide

http://www.xilinx.com/support/documentation/user_guides/s6_pcie_ug654.pdf

- Spartan-6 FPGA Integrated Block for PCI Express Data Sheet

http://www.xilinx.com/support/documentation/ip_documentation/s6_pcie_ds718.pdf

- IP Release Notes Guide

http://www.xilinx.com/support/documentation/ip_documentation/xtp025.pdf

Documentation

Documentation

▪ Spartan-6

- Spartan-6 FPGA Family

<http://www.xilinx.com/products/silicon-devices/fpga/spartan-6/index.htm>

▪ SP605 Documentation

- Spartan-6 FPGA SP605 Evaluation Kit

<http://www.xilinx.com/products/boards-and-kits/EK-S6-SP605-G.htm>

- SP605 Getting Started Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug525.pdf

- SP605 Hardware User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug526.pdf

- SP605 Reference Design User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug527.pdf