

ZC706 EVALUATION PLATFORM HW-Z7-ZC706 (XC7Z045-FFG900)

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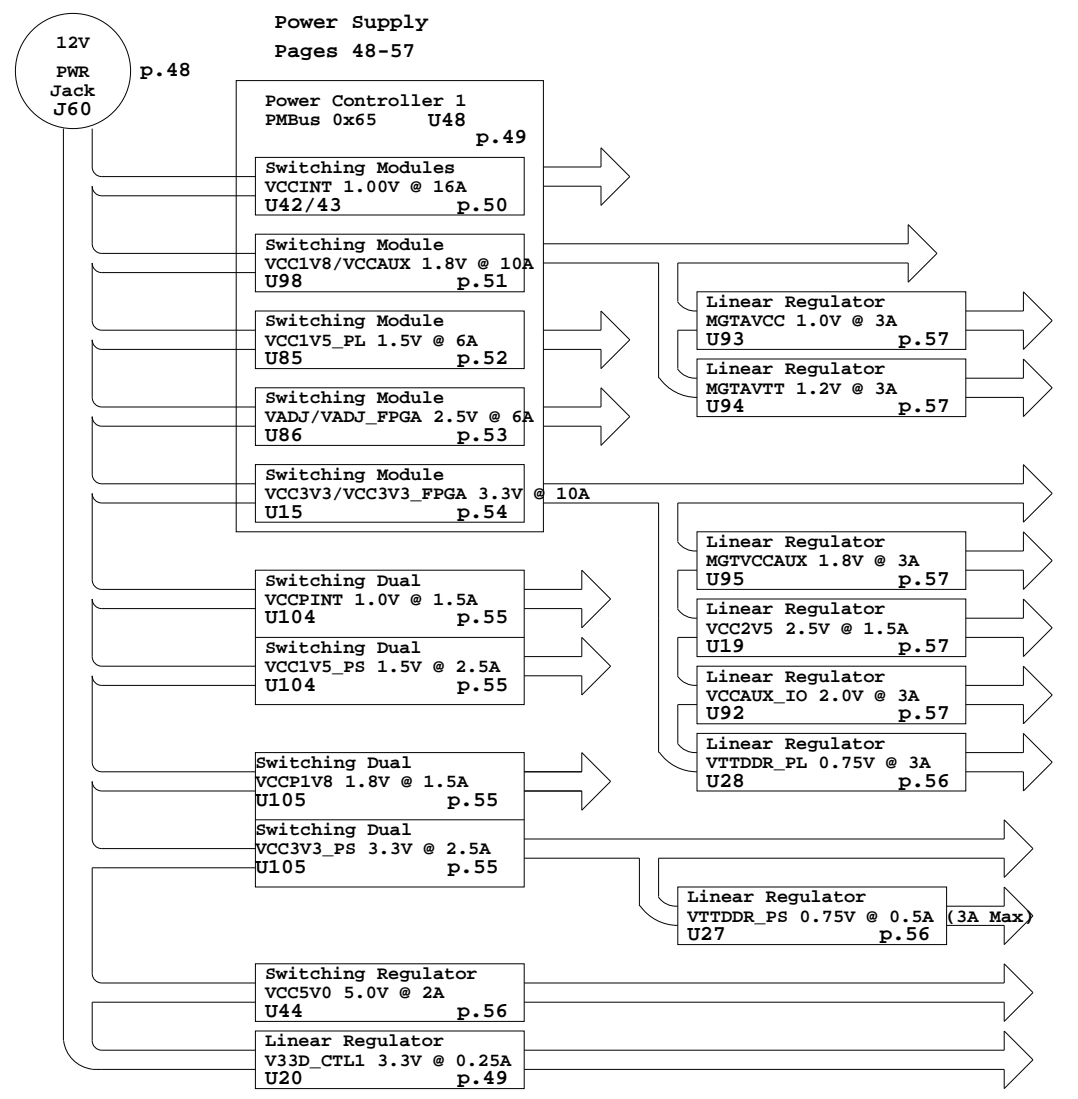
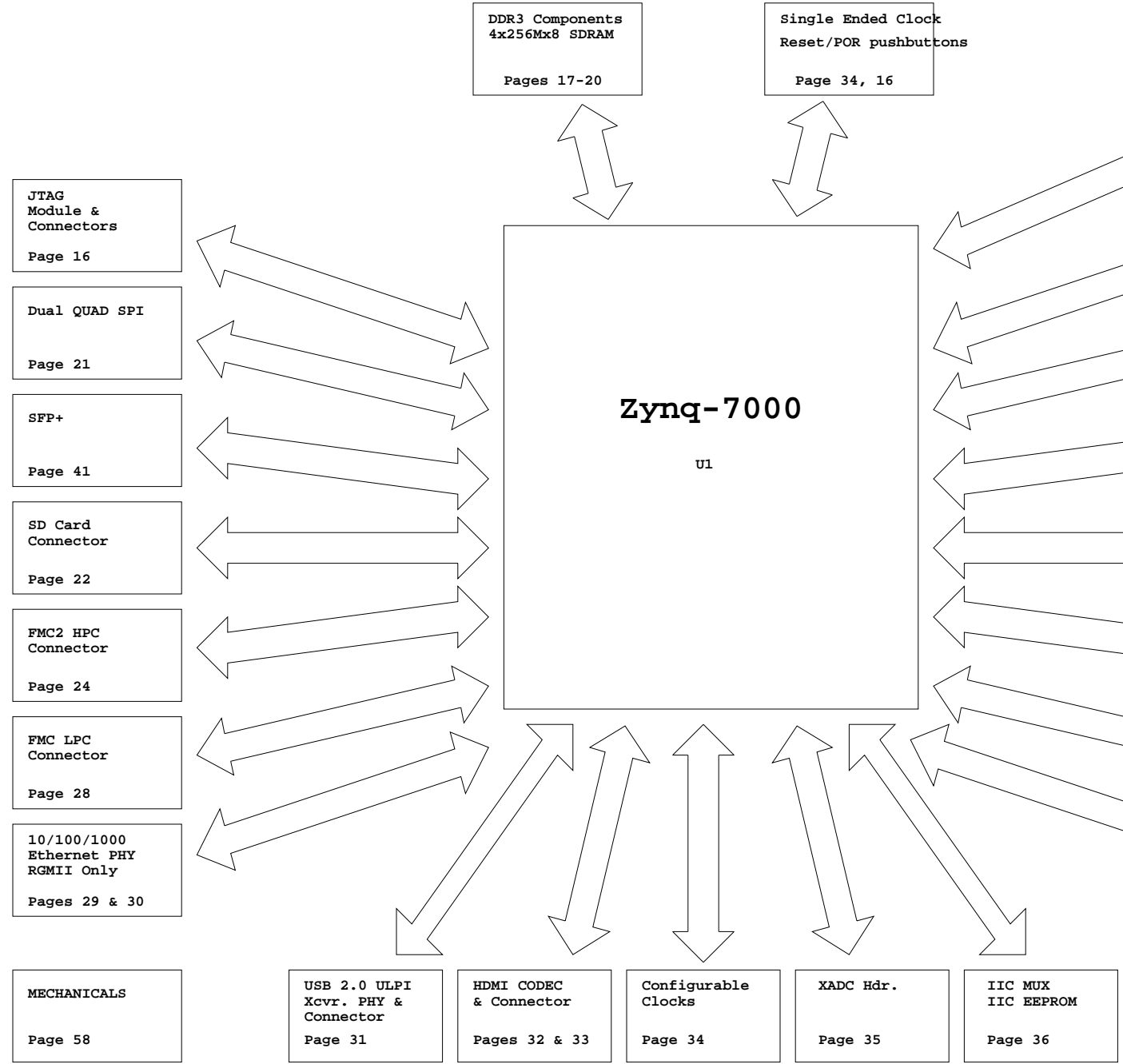
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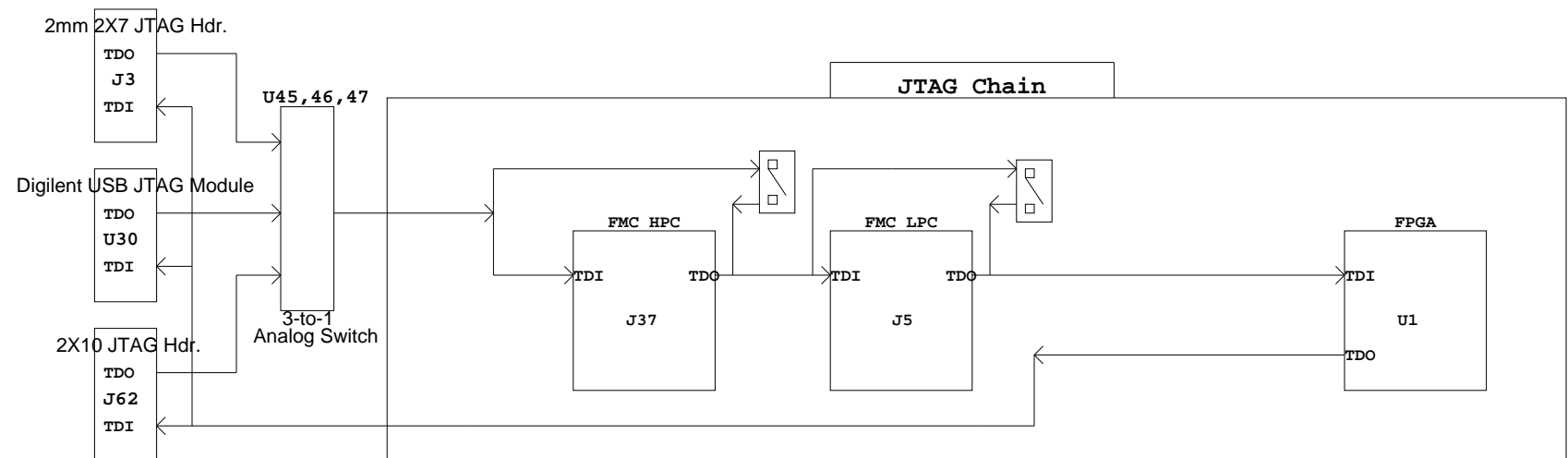


Title: DISCLAIMER		ASSY P/N: 0431760
SCHEM, ROHS COMPLIANT		PCB P/N: 1280681
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513
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IIC Addressing

0b1110100	PCA9548
0b1011101	SI570
0bxxxxx00	FMC HPC
0bxxxxx00	FMC LPC
0b1010100	IIC EEPROM
0b0100001	IIC Port Expander
0b0111001	ADV7511
0b1100101	PMBUS Controller
0b1010001	IIC RTC
0b1010000	SFP+
0b1101000	SI5324
0b1010000 0b0011000	DDR3 SODIMM



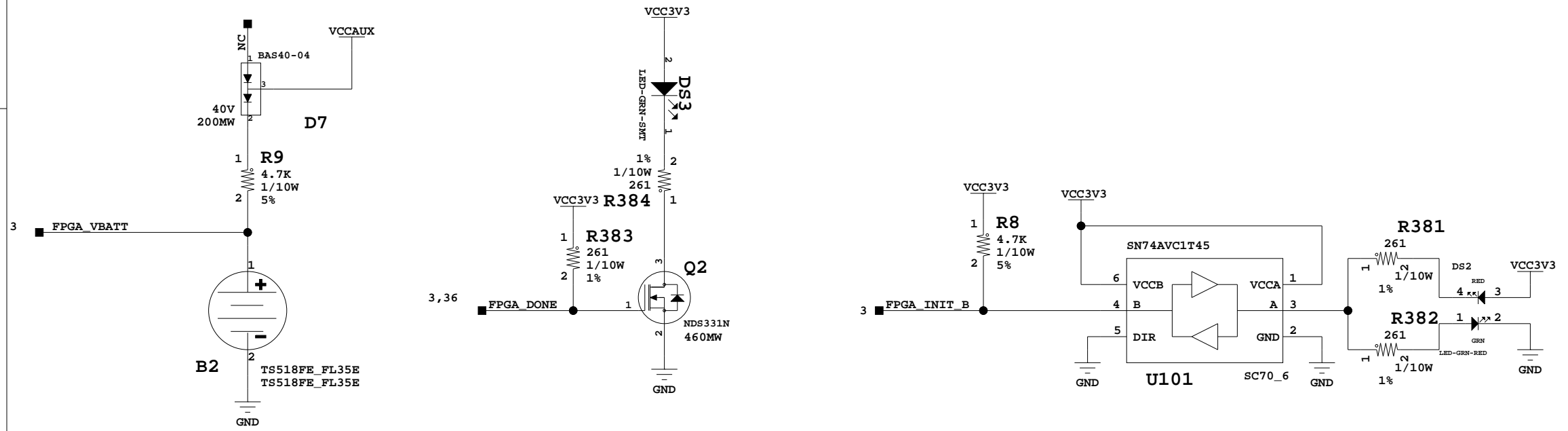
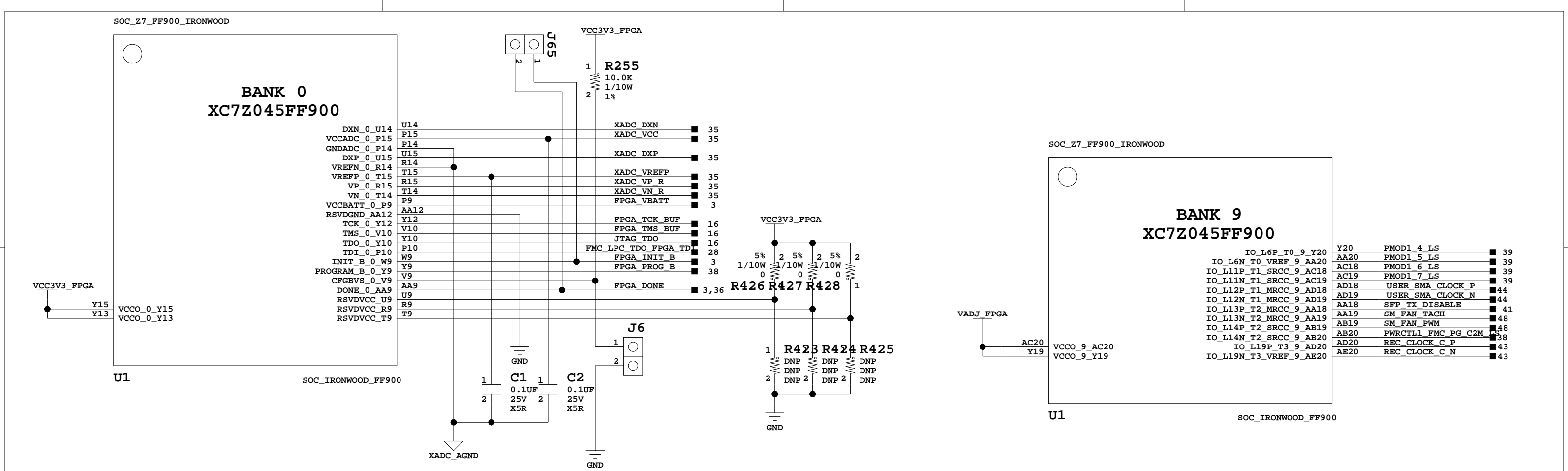
Title: ZC706 Block Diagram SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
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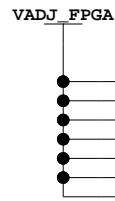
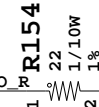


Zynq Bank 0, 9

Title: Zynq Bank 0, 9 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
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BANK 10 XC7Z045FF900

IO_0_10_AA13	AA13	PL PJTAG TDO	39
IO_L1P_T0_10_AK13	AK13	PL PJTAG TCK	39
IO_L1N_T0_10_AK12	AK12	PL PJTAG TMS	39
IO_L2P_T0_10_AH18	AH18	PL PJTAG TDI	39
IO_L2N_T0_10_AJ18	AJ18	IIC SDA MAIN LS	36
IO_L3P_T0_DQS_10_AJ14	AJ14	IIC SCL MAIN LS	36
IO_L3N_T0_DQS_10_AJ13	AJ13	GPIO DIP SW3	38
IO_L4P_T0_10_AJ16	AJ16	FMC LPC LA11 P	28
IO_L4N_T0_10_AK16	AK16	FMC LPC LA11 N	28
IO_L5P_T0_10_AJ15	AJ15	FMC LPC LA04 P	28
IO_L5N_T0_10_AK15	AK15	FMC LPC LA04 N	28
IO_L6P_T0_10_AH17	AH17	FMC LPC LA13 P	28
IO_L6N_T0_VREF_10_AH16	AH16	FMC LPC LA13 N	28
IO_L7P_T1_10_AE12	AE12	FMC LPC LA02 P	28
IO_L7N_T1_10_AF12	AF12	FMC LPC LA02 N	28
IO_L8P_T1_10_AH14	AH14	FMC LPC LA09 P	28
IO_L8N_T1_10_AH13	AH13	FMC LPC LA09 N	28
IO_L9P_T1_DQS_10_AD14	AD14	FMC LPC LA08 P	28
IO_L9N_T1_DQS_10_AD13	AD13	FMC LPC LA08 N	28
IO_L10P_T1_10_AG12	AG12	FMC LPC LA03 P	28
IO_L10N_T1_10_AH12	AH12	FMC LPC LA03 N	28
IO_L11P_T1_SRCC_10_AE13	AE13	FMC LPC LA00 CC P	28
IO_L11N_T1_SRCC_10_AF13	AF13	FMC LPC LA00 CC N	28
IO_L12P_T1_MRCC_10_AF14	AF14	USRCLK P	34
IO_L12N_T1_MRCC_10_AG14	AG14	USRCLK N	34
IO_L13P_T2_MRCC_10_AG17	AG17	FMC LPC CLK0 M2C P	28
IO_L13N_T2_MRCC_10_AG16	AG16	FMC LPC CLK0 M2C N	28
IO_L14P_T2_SRCC_10_AF15	AF15	FMC LPC LA01 CC P	28
IO_L14N_T2_SRCC_10_AG15	AG15	FMC LPC LA01 CC N	28
IO_L15P_T2_DQS_10_AF18	AF18	FMC LPC LA14 P	28
IO_L15N_T2_DQS_10_AF17	AF17	FMC LPC LA14 N	28
IO_L16P_T2_10_AE16	AE16	FMC LPC LA05 P	28
IO_L16N_T2_10_AE15	AE15	FMC LPC LA05 N	28
IO_L17P_T2_10_AE18	AE18	FMC LPC LA16 P	28
IO_L17N_T2_10_AE17	AE17	FMC LPC LA16 N	28
IO_L18P_T2_10_AD16	AD16	FMC LPC LA12 P	28
IO_L18N_T2_10_AD15	AD15	FMC LPC LA12 N	28
IO_L19P_T3_10_AC14	AC14	FMC LPC LA10 P	28
IO_L19N_T3_VREF_10_AC13	AC13	FMC LPC LA10 N	28
IO_L20P_T3_10_AA15	AA15	FMC LPC LA07 P	28
IO_L20N_T3_10_AA14	AA14	FMC LPC LA07 N	28
IO_L21P_T3_DQS_10_AB12	AB12	FMC LPC LA06 P	28
IO_L21N_T3_DQS_10_AB12	AB12	FMC LPC LA06 N	28
IO_L22P_T3_10_AB15	AB15	FMC LPC LA15 P	28
IO_L22N_T3_10_AB14	AB14	FMC LPC LA15 N	28
IO_L23P_T3_10_AC17	AC17	GPIO DIP SW2	38
IO_L23N_T3_10_AC16	AC16	GPIO DIP SW1	38
IO_L24P_T3_10_AB17	AB17	GPIO DIP SW0	38
IO_L24N_T3_10_AB16	AB16	PMOD1_3_LS	39
IO_25_10_AA17	AA17	IIC RTC IRQ_1_B	37

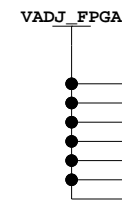


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SOC_IRONWOOD_FF900

BANK 11 XC7Z045FF900

IO_0_11_W23	W23	SI5324_RST_LS	47
IO_L1P_T0_11_AJ25	AJ25	SI5324_INT_ALM_LS	47
IO_L1N_T0_11_AK25	AK25	GPIO_SW_LEFT	38
IO_L2P_T0_11_AK22	AK22	PCIE_WAKE_B_LS	39
IO_L2N_T0_11_AK23	AK23	PCIE_PERST_LS	47
IO_L3P_T0_DQS_11_AJ21	AJ21	PMOD1_0_LS	39
IO_L3N_T0_DQS_11_AK21	AK21	PMOD1_1_LS	39
IO_L4P_T0_11_AJ23	AJ23	FMC_HPC_LA07_P	26
IO_L4N_T0_11_AJ24	AJ24	FMC_HPC_LA07_N	26
IO_L5P_T0_11_AH23	AH23	FMC_HPC_LA05_P	24
IO_L5N_T0_11_AH24	AH24	FMC_HPC_LA05_N	24
IO_L6P_T0_11_AG22	AG22	FMC_HPC_LA06_P	24
IO_L6N_T0_VREF_11_AH22	AH22	FMC_HPC_LA06_N	24
IO_L7P_T1_11_AC24	AC24	FMC_HPC_LA14_P	24
IO_L7N_T1_11_AD24	AD24	FMC_HPC_LA14_N	24
IO_L8P_T1_11_AG24	AG24	FMC_HPC_LA10_P	24
IO_L8N_T1_11_AG25	AG25	FMC_HPC_LA10_N	24
IO_L9P_T1_DQS_11_AF23	AF23	FMC_HPC_LA12_P	25
IO_L9N_T1_DQS_11_AF24	AF24	FMC_HPC_LA12_N	25
IO_L10P_T1_11_AD21	AD21	FMC_HPC_LA09_P	24
IO_L10N_T1_11_AE21	AE21	FMC_HPC_LA09_N	24
IO_L11P_T1_SRCC_11_AD23	AD23	FMC_HPC_LA11_P	26
IO_L11N_T1_SRCC_11_AE23	AE23	FMC_HPC_LA11_N	26
IO_L12P_T1_MRCC_11_AE22	AE22	FMC_HPC_CLK0_M2C_P	26
IO_L12N_T1_MRCC_11_AF22	AF22	FMC_HPC_CLK0_M2C_N	26
IO_L13P_T2_MRCC_11_AG21	AG21	FMC_HPC_LA01_CC_P	24
IO_L13N_T2_MRCC_11_AH21	AH21	FMC_HPC_LA01_CC_N	24
IO_L14P_T2_SRCC_11_AF20	AF20	FMC_HPC_LA00_CC_P	25
IO_L14N_T2_SRCC_11_AG20	AG20	FMC_HPC_LA00_CC_N	25
IO_L15P_T2_DQS_11_AJ20	AJ20	FMC_HPC_LA04_P	26
IO_L15N_T2_DQS_11_AK20	AK20	FMC_HPC_LA04_N	26
IO_L16P_T2_11_AK17	AK17	FMC_HPC_LA02_P	26
IO_L16N_T2_11_AK18	AK18	FMC_HPC_LA02_N	26
IO_L17P_T2_11_AH19	AH19	FMC_HPC_LA03_P	25
IO_L17N_T2_11_AJ19	AJ19	FMC_HPC_LA03_N	25
IO_L18P_T2_11_AF19	AF19	FMC_HPC_LA08_P	25
IO_L18N_T2_11_AG19	AG19	FMC_HPC_LA08_N	25
IO_L19P_T3_11_AB21	AB21	PMOD1_2_LS	39
IO_L19N_T3_VREF_11_AB22	AB22	HDMI_SPDIF_OUT_LS	38
IO_L20P_T3_11_W21	W21	GPIO_LED_RIGHT	38
IO_L20N_T3_11_Y21	Y21	GPIO_LED_LEFT	38
IO_L21P_T3_DQS_11_Y22	Y22	FMC_HPC_LA15_P	26
IO_L21N_T3_DQS_11_Y23	Y23	FMC_HPC_LA15_N	26
IO_L22P_T3_11_AA24	AA24	FMC_HPC_LA16_P	25
IO_L22N_T3_11_AB24	AB24	FMC_HPC_LA16_N	25
IO_L23P_T3_11_AA22	AA22	FMC_HPC_LA13_P	24
IO_L23N_T3_11_AA23	AA23	FMC_HPC_LA13_N	24
IO_L24P_T3_11_AC22	AC22	HDMI_R_D35	33
IO_L24N_T3_11_AC23	AC23	HDMI_INT	32
IO_25_11_AC21	AC21	HDMI_R_SPDIF	33



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SOC_IRONWOOD_FF900

Zynq Bank 10, 11



Title: Zynq Bank 10, 11 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM
 ASSY P/N: 0431760
 PCB P/N: 1280681
 SCH P/N: 0381513

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SOC_Z7_FF900_IRONWOOD

BANK 12 XC7Z045FF900

IO_0_12_Y25	Y25	HDMI_R_D21	33
IO_L1P_T0_12_Y30	Y30	FMC_LPC_LA33_P	28
IO_L1N_T0_12_AA30	AA30	FMC_LPC_LA33_N	28
IO_L2P_T0_12_AB29	AB29	FMC_LPC_LA30_P	28
IO_L2N_T0_12_AB30	AB30	FMC_LPC_LA30_N	28
IO_L3P_T0_DQS_12_Y26	Y26	FMC_LPC_LA32_P	28
IO_L3N_T0_DQS_12_Y27	Y27	FMC_LPC_LA32_N	28
IO_L4P_T0_12_Y28	Y28	HDMI_R_D28	33
IO_L4N_T0_12_AA29	AA29	HDMI_R_D22	33
IO_L5P_T0_12_AA27	AA27	HDMI_R_D31	33
IO_L5N_T0_12_AA28	AA28	HDMI_R_D18	33
IO_L6P_T0_12_AB25	AB25	HDMI_R_D10	33
IO_L6N_T0_VREF_12_AB26	AB26	HDMI_R_D17	33
IO_L7P_T1_12_AC26	AC26	HDMI_R_D19	33
IO_L7N_T1_12_AD26	AD26	HDMI_R_D16	33
IO_L8P_T1_12_AD30	AD30	HDMI_R_D23	33
IO_L8N_T1_12_AE30	AE30	HDMI_R_D20	33
IO_L9P_T1_DQS_12_AC29	AC29	FMC_LPC_LA31_P	28
IO_L9N_T1_DQS_12_AD29	AD29	FMC_LPC_LA31_N	28
IO_L10P_T1_12_AD25	AD25	FMC_LPC_LA28_P	28
IO_L10N_T1_12_AE26	AE26	FMC_LPC_LA28_N	28
IO_L11P_T1_SRCC_12_AB27	AB27	FMC_LPC_LA17_CC_P	28
IO_L11N_T1_SRCC_12_AC27	AC27	FMC_LPC_LA17_CC_N	28
IO_L12P_T1_MRCC_12_AC28	AC28	FMC_LPC_CLK1_M2C_P	28
IO_L12N_T1_MRCC_12_AD28	AD28	FMC_LPC_CLK1_M2C_N	28
IO_L13P_T2_MRCC_12_AE28	AE28	HDMI_R_D8	33
IO_L13N_T2_MRCC_12_AE28	AE28	HDMI_R_D29	33
IO_L14P_T2_SRCC_12_AE27	AE27	FMC_LPC_LA18_CC_P	28
IO_L14N_T2_SRCC_12_AF27	AF27	FMC_LPC_LA18_CC_N	28
IO_L15P_T2_DQS_12_AF29	AF29	FMC_LPC_LA25_P	28
IO_L15N_T2_DQS_12_AE29	AG29	FMC_LPC_LA25_N	28
IO_L16P_T2_12_AF30	AF30	FMC_LPC_LA24_P	28
IO_L16N_T2_12_AG30	AG30	FMC_LPC_LA24_N	28
IO_L17P_T2_12_AG26	AG26	FMC_LPC_LA20_P	28
IO_L17N_T2_12_AG27	AG27	FMC_LPC_LA20_N	28
IO_L18P_T2_12_AE25	AE25	FMC_LPC_LA29_P	28
IO_L18N_T2_12_AF25	AF25	FMC_LPC_LA29_N	28
IO_L19P_T3_12_AH28	AH28	FMC_LPC_LA21_P	28
IO_L19N_T3_VREF_12_AH29	AH29	FMC_LPC_LA21_N	28
IO_L20P_T3_12_AJ30	AJ30	FMC_LPC_LA26_P	28
IO_L20N_T3_12_AK30	AK30	FMC_LPC_LA26_N	28
IO_L21P_T3_DQS_12_AJ28	AJ28	FMC_LPC_LA27_P	28
IO_L21N_T3_DQS_12_AJ29	AJ29	FMC_LPC_LA27_N	28
IO_L22P_T3_12_AK27	AK27	FMC_LPC_LA22_P	28
IO_L22N_T3_12_AK28	AK28	FMC_LPC_LA22_N	28
IO_L23P_T3_12_AH26	AH26	FMC_LPC_LA19_P	28
IO_L23N_T3_12_AH27	AH27	FMC_LPC_LA19_N	28
IO_L24P_T3_12_AJ26	AJ26	FMC_LPC_LA23_P	28
IO_L24N_T3_12_AK26	AK26	FMC_LPC_LA23_N	28
IO_25_12_AA25	AA25	HDMI_R_D7	33

VADJ_FPGA

AA26	VCCO_12_AA26
AC30	VCCO_12_AC30
AD27	VCCO_12_AD27
AG28	VCCO_12_AG28
AK29	VCCO_12_AK29
Y29	VCCO_12_Y29

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SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK 13 XC7Z045FF900

IO_0_13_U21	U21	HDMI_R_VSYNC	33
IO_L1P_T0_13_P30	P30	FMC_HPC_LA28_P	26
IO_L1N_T0_13_R30	R30	FMC_HPC_LA28_N	26
IO_L2P_T0_13_T30	T30	FMC_HPC_LA24_P	26
IO_L2N_T0_13_U30	U30	FMC_HPC_LA24_N	26
IO_L3P_T0_DQS_13_N28	N28	HDMI_R_D33	33
IO_L3N_T0_DQS_13_P28	P28	HDMI_R_CLK	33
IO_L4P_T0_13_N29	N29	FMC_HPC_LA31_P	25
IO_L4N_T0_13_P29	P29	FMC_HPC_LA31_N	25
IO_L5P_T0_13_T29	T29	FMC_HPC_LA25_P	25
IO_L5N_T0_13_U29	U29	FMC_HPC_LA25_N	25
IO_L6P_T0_13_R28	R28	FMC_HPC_LA26_P	24
IO_L6N_T0_VREF_13_T28	T28	FMC_HPC_LA26_N	24
IO_L7P_T1_13_V28	V28	FMC_HPC_LA27_P	24
IO_L7N_T1_13_V29	V29	FMC_HPC_LA27_N	24
IO_L8P_T1_13_W29	W29	FMC_HPC_LA21_P	24
IO_L8N_T1_13_W30	W30	FMC_HPC_LA21_N	26
IO_L9P_T1_DQS_13_V27	V27	FMC_HPC_LA22_P	25
IO_L9N_T1_DQS_13_W28	W28	FMC_HPC_LA22_N	25
IO_L10P_T1_13_W25	W25	FMC_HPC_LA18_CC_P	24
IO_L10N_T1_13_W26	W26	FMC_HPC_LA18_CC_N	24
IO_L11P_T1_SRCC_13_U25	U25	FMC_HPC_LA20_P	25
IO_L11N_T1_SRCC_13_V26	V26	FMC_HPC_LA20_N	25
IO_L12P_T1_MRCC_13_U26	U26	FMC_HPC_CLK1_M2C_P	25
IO_L12N_T1_MRCC_13_U27	U27	FMC_HPC_CLK1_M2C_N	25
IO_L13P_T2_MRCC_13_R25	R25	FMC_HPC_LA29_P	25
IO_L13N_T2_MRCC_13_R26	R26	FMC_HPC_LA29_N	25
IO_L14P_T2_SRCC_13_R27	R27	GPIO_SW_RIGHT	38
IO_L14N_T2_SRCC_13_T27	T27	HDMI_R_D11	33
IO_L15P_T2_DQS_13_N26	N26	FMC_HPC_LA33_P	25
IO_L15N_T2_DQS_13_N27	N27	FMC_HPC_LA33_N	25
IO_L16P_T2_13_P25	P25	FMC_HPC_LA23_P	24
IO_L16N_T2_13_P26	P26	FMC_HPC_LA23_N	24
IO_L17P_T2_13_T24	T24	FMC_HPC_LA19_P	26
IO_L17N_T2_13_T25	T25	FMC_HPC_LA19_N	26
IO_L18P_T2_13_P23	P23	FMC_HPC_LA30_P	26
IO_L18N_T2_13_P24	P24	FMC_HPC_LA30_N	26
IO_L19P_T3_13_P21	P21	FMC_HPC_LA32_P	26
IO_L19N_T3_VREF_13_R21	R21	FMC_HPC_LA32_N	26
IO_L20P_T3_13_T22	T22	HDMI_R_D5	33
IO_L20N_T3_13_T23	T23	HDMI_R_D9	33
IO_L21P_T3_DQS_13_R22	R22	HDMI_R_HSYNC	33
IO_L21N_T3_DQS_13_R23	R23	HDMI_R_D6	33
IO_L22P_T3_13_U22	U22	HDMI_R_D30	33
IO_L22N_T3_13_V22	V22	HDMI_R_D32	33
IO_L23P_T3_13_U24	U24	HDMI_R_D4	33
IO_L23N_T3_13_V24	V24	HDMI_R_DE	33
IO_L24P_T3_13_V23	V23	FMC_HPC_LA17_CC_P	24
IO_L24N_T3_13_W24	W24	FMC_HPC_LA17_CC_N	24
IO_25_13_V21	V21	HDMI_R_D34	33

VADJ_FPGA

N30	VCCO_13_N30
P27	VCCO_13_P27
R24	VCCO_13_R24
T21	VCCO_13_T21
U28	VCCO_13_U28
V25	VCCO_13_V25

U1

SOC_IRONWOOD_FF900

Zynq Bank 12, 13



Title: Zynq Bank 12, 13
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1

Sheet Size: B Rev: 02

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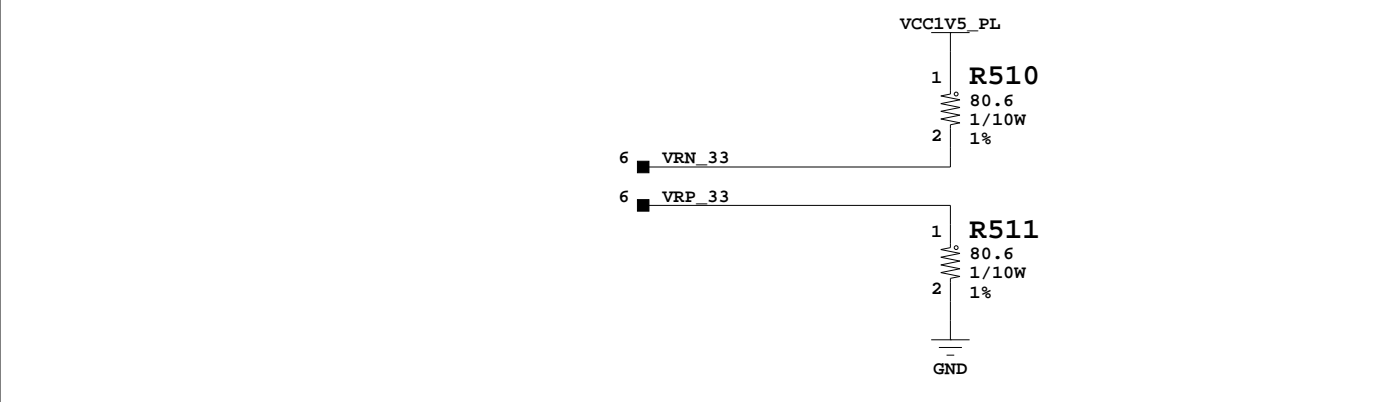
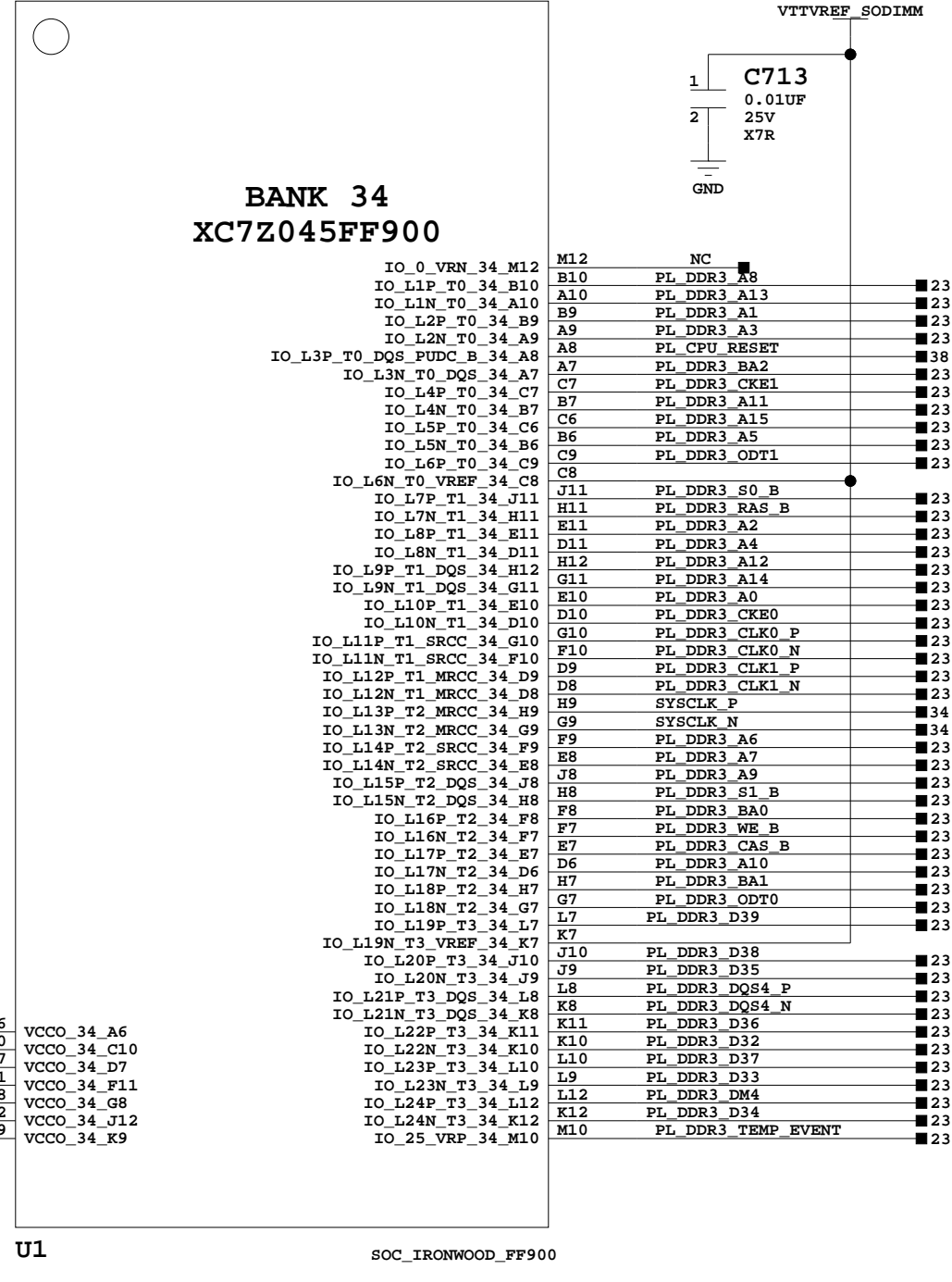
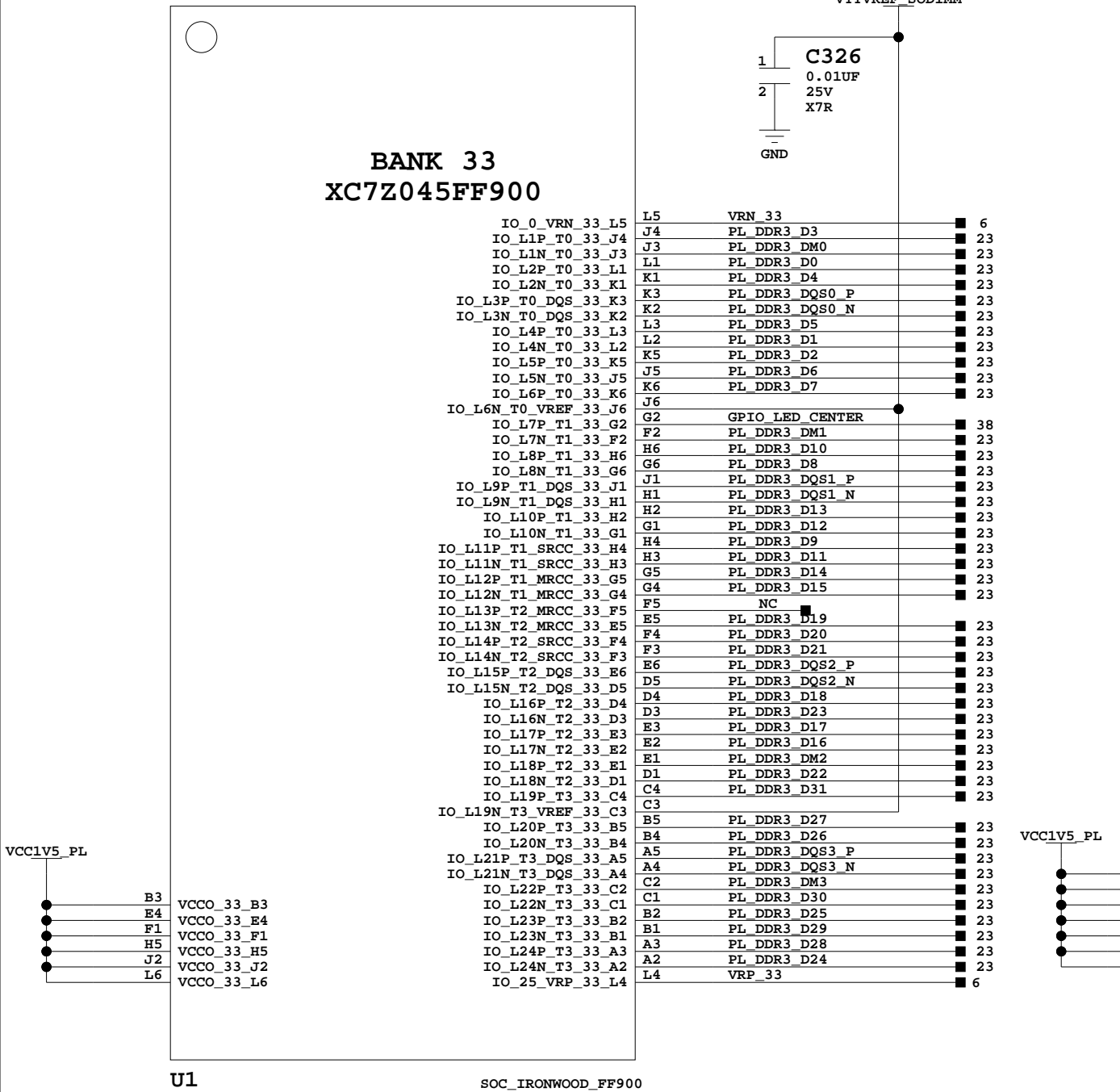
SOC_Z7_FF900_IRONWOOD

SOC_Z7_FF900_IRONWOOD

VTTVREF_SODIMM

BANK 33 XC7Z045FF900

BANK 34 XC7Z045FF900



Zynq Bank 33, 34

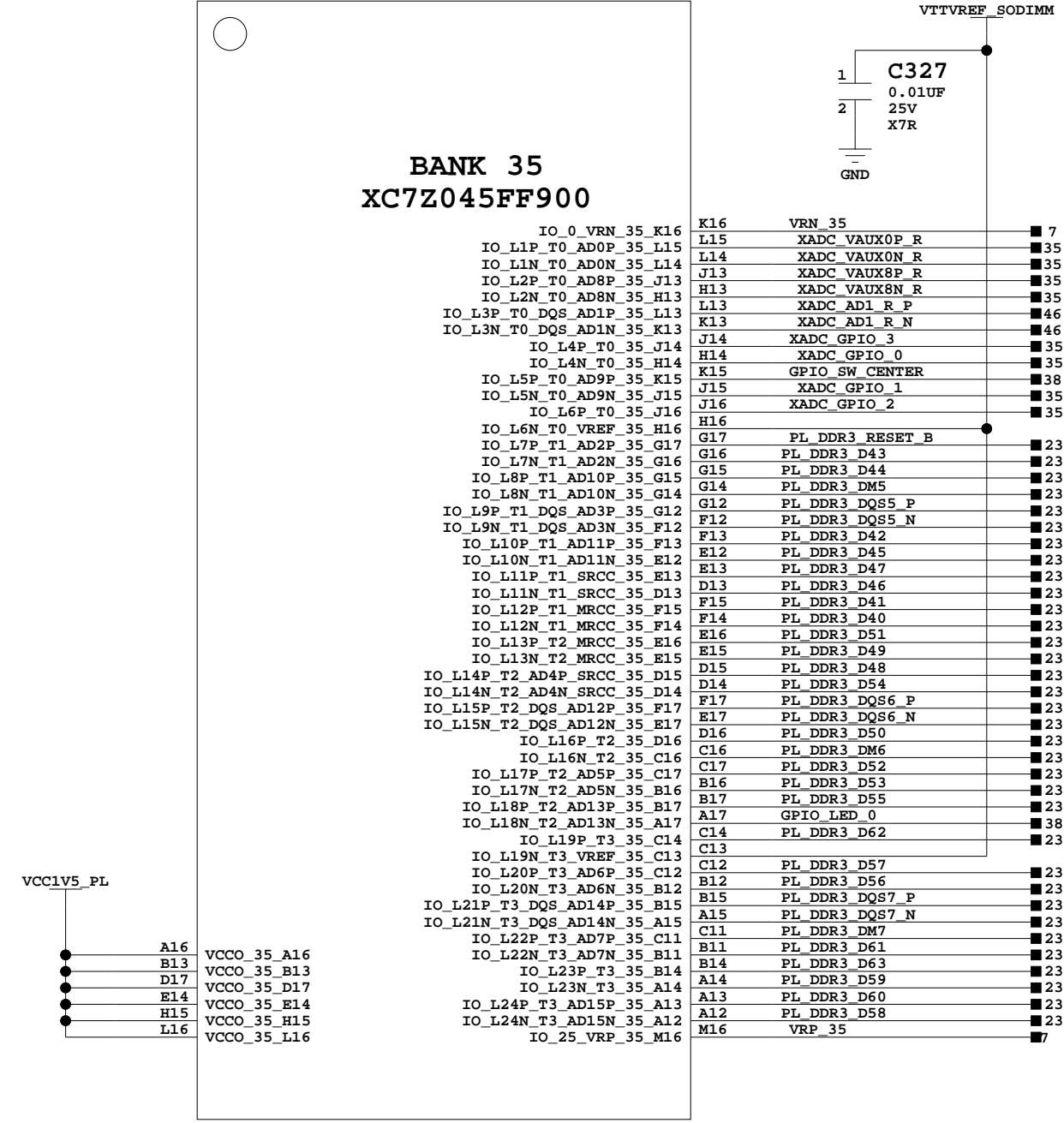


Title: Zynq Bank 33, 34
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
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SOC_Z7_FF900_IRONWOOD



Zynq Bank 35



Title: Zynq Bank 35		ASSY P/N: 0431760
SCHEM, ROHS COMPLIANT		PCB P/N: 1280681
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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SOC_Z7_FF900_IRONWOOD

BANK 109 XC7Z045FF900

MGTXXXP0_109_AK10	AK10	FMC HPC DP0 C2M P	24
MGTXXN0_109_AK9	AK9	FMC HPC DP0 C2M N	24
MGTXXXP0_109_AH10	AH10	FMC HPC DP0 M2C P	24
MGTXXN0_109_AH9	AH9	FMC HPC DP0 M2C N	24
MGTXXXP1_109_AK6	AK6	FMC HPC DP1 C2M P	24
MGTXXN1_109_AK5	AK5	FMC HPC DP1 C2M N	24
MGTXXXP1_109_AJ8	AJ8	FMC HPC DP1 M2C P	24
MGTXXN1_109_AJ7	AJ7	FMC HPC DP1 M2C N	24
MGTXXXP2_109_AJ4	AJ4	FMC HPC DP2 C2M P	24
MGTXXN2_109_AJ3	AJ3	FMC HPC DP2 C2M N	24
MGTXXXP2_109_AG8	AG8	FMC HPC DP2 M2C P	24
MGTXXN2_109_AG7	AG7	FMC HPC DP2 M2C N	24
MGTXXXP3_109_AK2	AK2	FMC HPC DP3 C2M P	24
MGTXXN3_109_AK1	AK1	FMC HPC DP3 C2M N	24
MGTXXXP3_109_AE8	AE8	FMC HPC DP3 M2C P	24
MGTXXN3_109_AE7	AE7	FMC HPC DP3 M2C N	24
MGTREFCLK0P_109_AD10	AD10	FMC HPC GBTCLK0 M2C P	18
MGTREFCLK0N_109_AD9	AD9	FMC HPC GBTCLK0 M2C N	18
MGTREFCLK1P_109_AF10	AF10	NC	
MGTREFCLK1N_109_AF9	AF9	NC	

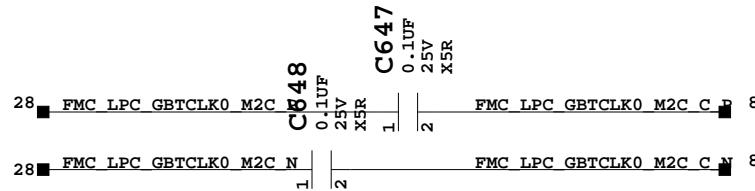
U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

BANK 110 XC7Z045FF900

MGTXXXP0_110_AH2	AH2	FMC HPC DP4 C2M P	24
MGTXXN0_110_AH1	AH1	FMC HPC DP4 C2M N	24
MGTXXXP0_110_AH6	AH6	FMC HPC DP4 M2C P	24
MGTXXN0_110_AH5	AH5	FMC HPC DP4 M2C N	24
MGTXXXP1_110_AF2	AF2	FMC HPC DP5 C2M P	24
MGTXXN1_110_AF1	AF1	FMC HPC DP5 C2M N	24
MGTXXXP1_110_AG4	AG4	FMC HPC DP5 M2C P	24
MGTXXN1_110_AG3	AG3	FMC HPC DP5 M2C N	24
MGTXXXP2_110_AE4	AE4	FMC HPC DP6 C2M P	24
MGTXXN2_110_AE3	AE3	FMC HPC DP6 C2M N	24
MGTXXXP2_110_AF6	AF6	FMC HPC DP6 M2C P	24
MGTXXN2_110_AF5	AF5	FMC HPC DP6 M2C N	24
MGTXXXP3_110_AD2	AD2	FMC HPC DP7 C2M P	24
MGTXXN3_110_AD1	AD1	FMC HPC DP7 C2M N	24
MGTXXXP3_110_AD6	AD6	FMC HPC DP7 M2C P	24
MGTXXN3_110_AD5	AD5	FMC HPC DP7 M2C N	24
MGTREFCLK0P_110_AA8	AA8	FMC HPC GBTCLK1 M2C P	18
MGTREFCLK0N_110_AA7	AA7	FMC HPC GBTCLK1 M2C N	18
MGTREFCLK1P_110_AC8	AC8	SI5324_OUT_C_P	43
MGTREFCLK1N_110_AC7	AC7	SI5324_OUT_C_N	43

U1 SOC_IRONWOOD_FF900

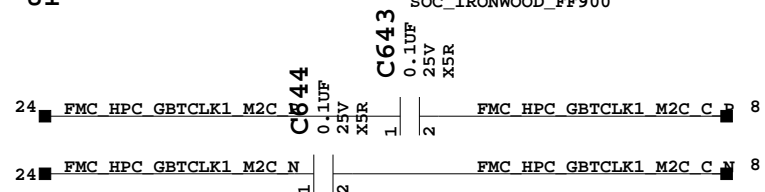


SOC_Z7_FF900_IRONWOOD

BANK 111 XC7Z045FF900

MGTXXXP0_111_AB2	AB2	FMC LPC DP0 C2M P	28
MGTXXN0_111_AB1	AB1	FMC LPC DP0 C2M N	28
MGTXXXP0_111_AC4	AC4	FMC LPC DP0 M2C P	28
MGTXXN0_111_AC3	AC3	FMC LPC DP0 M2C N	28
MGTXXXP1_111_Y2	Y2	SMA MGT TX P	44
MGTXXN1_111_Y1	Y1	SMA MGT TX N	44
MGTXXXP1_111_AB6	AB6	SMA MGT RX P	44
MGTXXN1_111_AB5	AB5	SMA MGT RX N	44
MGTXXXP2_111_W4	W4	SFP TX P	41
MGTXXN2_111_W3	W3	SFP TX N	41
MGTXXXP2_111_Y6	Y6	SFP RX P	41
MGTXXN2_111_Y5	Y5	SFP RX N	41
MGTXXXP3_111_V2	V2		
MGTXXN3_111_V1	V1		
MGTXXXP3_111_AA4	AA4		
MGTXXN3_111_AA3	AA3		
MGTREFCLK0P_111_U8	U8	FMC LPC GBTCLK0 M2C P	8
MGTREFCLK0N_111_U7	U7	FMC LPC GBTCLK0 M2C N	8
MGTREFCLK1P_111_W8	W8	SMA MGT REFCLK P	44
MGTREFCLK1N_111_W7	W7	SMA MGT REFCLK N	44

U1 SOC_IRONWOOD_FF900

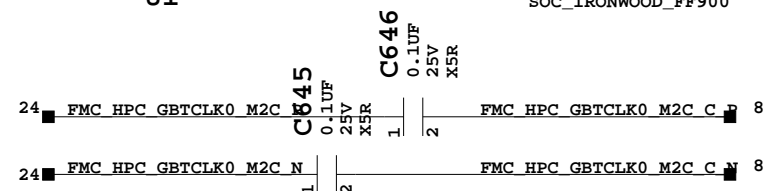


SOC_Z7_FF900_IRONWOOD

BANK 112 XC7Z045FF900

MGTXXXP0_112_T2	T2	PCIE TX3 P	42
MGTXXN0_112_T1	T1	PCIE TX3 N	42
MGTXXXP0_112_V6	V6	PCIE RX3 P	42
MGTXXN0_112_V5	V5	PCIE RX3 N	42
MGTXXXP1_112_R4	R4	PCIE TX2 P	42
MGTXXN1_112_R3	R3	PCIE TX2 N	42
MGTXXXP1_112_U4	U4	PCIE RX2 P	42
MGTXXN1_112_U3	U3	PCIE RX2 N	42
MGTXXXP2_112_P2	P2	PCIE TX1 P	42
MGTXXN2_112_P1	P1	PCIE TX1 N	42
MGTXXXP2_112_T6	T6	PCIE RX1 P	42
MGTXXN2_112_T5	T5	PCIE RX1 N	42
MGTXXXP3_112_N4	N4	PCIE TX0 P	42
MGTXXN3_112_N3	N3	PCIE TX0 N	42
MGTXXXP3_112_P6	P6	PCIE RX0 P	42
MGTXXN3_112_P5	P5	PCIE RX0 N	42
MGTREFCLK0P_112_N8	N8	PCIE CLK_Q0_P	42
MGTREFCLK0N_112_N7	N7	PCIE CLK_Q0_N	42
MGTREFCLK1P_112_R8	R8	NC	
MGTREFCLK1N_112_R7	R7	NC	
MGTAVTTRCAL_112_AB10	AB10	MGTAVTT	
MGTTRREF_112_AB9	AB9		

U1 SOC_IRONWOOD_FF900



Zynq MGT Banks



Title: Zynq MGT Banks
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
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BANK 500 XC7Z045FF900

PS_POR_B_500_D21	D21	PS_POR_B	15, 29, 31
PS_CLK_500_A22	A22	PS_CLK	34
PS_MIO0_500_F24	F24	QSPI1_CS_B	21
PS_MIO1_500_D23	D23	QSPI0_CS_B	21
PS_MIO2_500_F23	F23	QSPI0_IO0	15, 21
PS_MIO3_500_C23	C23	QSPI0_IO1	15, 21
PS_MIO4_500_E23	E23	QSPI0_IO2	15, 21
PS_MIO5_500_C24	C24	QSPI0_IO3	15, 21
PS_MIO6_500_D24	D24	QSPI0_CLK	15, 21
PS_MIO7_500_B24	B24	USB_RESET_B_AND	15, 31
PS_MIO8_500_C21	C21	PS_MIO8	15
PS_MIO9_500_A24	A24	QSPI1_CLK	21
PS_MIO10_500_E22	E22	QSPI1_IO0	21
PS_MIO11_500_A23	A23	QSPI1_IO1	21
PS_MIO12_500_E21	E21	QSPI1_IO2	21
PS_MIO13_500_F22	F22	QSPI1_IO3	21
PS_MIO14_500_B22	B22	SDIO_SDDDET	22
PS_MIO15_500_C22	C22	SDIO_SDWP	22

VCCP1V8

B23 VCCO_MIO0_500_B23
E24 VCCO_MIO0_500_E24
F21 VCCO_MIO0_500_F21

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SOC_IRONWOOD_FF900

BANK 501 XC7Z045FF900

PS_MIO53_501_C18	C18	PHY_MDIO	29
PS_MIO52_501_D19	D19	PHY_MDC	29
PS_MIO51_501_F19	F19	PS_SDA_MAIN	36
PS_MIO50_501_A19	A19	PS_SCL_MAIN	36
PS_MIO49_501_D18	D18	USB_UART_TX	36
PS_MIO48_501_C19	C19	USB_UART_RX	40
PS_MIO47_501_A18	A18	PHY_RESET_B_AND	40
PS_MIO46_501_F20	F20	IIC_MUX_RESET_B_LS	38
PS_MIO45_501_H18	H18	SDIO_CD_DAT3_LS	22
PS_MIO44_501_E20	E20	SDIO_DAT2_LS	22
PS_MIO43_501_E18	E18	SDIO_DAT1_LS	22
PS_MIO42_501_D20	D20	SDIO_DAT0_LS	22
PS_MIO41_501_J18	J18	SDIO_CMD_LS	22
PS_MIO40_501_B20	B20	SDIO_CLK_LS_R	22
PS_MIO39_501_F18	F18	USB_DATA7	31
PS_MIO38_501_A20	A20	USB_DATA6	31
PS_MIO37_501_B21	B21	USB_DATA5	31
PS_MIO36_501_H17	H17	USB_CLKOUT	31
PS_MIO35_501_G21	G21	USB_DATA3	31
PS_MIO34_501_K18	K18	USB_DATA2	31
PS_MIO33_501_G22	G22	USB_DATA1	31
PS_MIO32_501_K17	K17	USB_DATA0	31
PS_MIO31_501_H21	H21	USB_NXT	31
PS_MIO30_501_L18	L18	USB_STP	31
PS_MIO29_501_H22	H22	USB_DIR	31
PS_MIO28_501_L17	L17	USB_DATA4	31
PS_MIO27_501_G20	G20	PHY_RX_CTRL	29
PS_MIO26_501_M17	M17	PHY_RXD3	29
PS_MIO25_501_G19	G19	PHY_RXD2	29
PS_MIO24_501_M19	M19	PHY_RXD1	29
PS_MIO23_501_J21	J21	PHY_RXD0	29
PS_MIO22_501_L20	L20	PHY_RX_CLK	29
PS_MIO21_501_J19	J19	PHY_TX_CTRL	29
PS_MIO20_501_M20	M20	PHY_TXD3	29
PS_MIO19_501_J20	J20	PHY_TXD2	29
PS_MIO18_501_K20	K20	PHY_TXD1	29
PS_MIO17_501_K21	K21	PHY_TXD0	29
PS_MIO16_501_L19	L19	PHY_TX_CLK	29
PS_SRST_B_501_B19	B19	PS_SRST_B	15
PS_MIO_VREF_501_H19	H19	PS_MIO_VREF	15

VCCP1V8

C20 VCCO_MIO1_501_C20
G18 VCCO_MIO1_501_G18
J22 VCCO_MIO1_501_J22
K19 VCCO_MIO1_501_K19

U1

SOC_IRONWOOD_FF900

R541
49.9
1/20W
1%

SDIO_CLK_LS 22

R352
1.00K
1/16W
1%

R353
1.00K
1/16W
1%

VCCP1V8

C328
0.01UF
25V
X7R

Zynq Banks 500, 501



Title: Zynq Banks 500, 501
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1

Sheet Size: B Rev: 02

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SOC_Z7_FF900_IRONWOOD

BANK 502 XC7Z045FF900

PS_DDR_DRST_B_502_F25	F25	PS_DDR3_RESET_B	17,18,19,20
PS_DDR_DQ1_502_E25	E25	PS_DDR3_DQ3	17
PS_DDR_DQ0_502_A25	A25	PS_DDR3_DQ1	17
PS_DDR_DQ3_502_D25	D25	PS_DDR3_DQ6	17
PS_DDR_DQ2_502_B27	B27	PS_DDR3_DQ7	17
PS_DDR_DM0_502_C27	C27	PS_DDR3_DM0	17
PS_DDR_DQS_N0_502_B26	B26	PS_DDR3_DQS0_N	17
PS_DDR_DQS_P0_502_C26	C26	PS_DDR3_DQS0_P	17
PS_DDR_DQ5_502_E26	E26	PS_DDR3_DQ0	17
PS_DDR_DQ4_502_B25	B25	PS_DDR3_DQ5	17
PS_DDR_DQ7_502_E27	E27	PS_DDR3_DQ2	17
PS_DDR_DQ6_502_D26	D26	PS_DDR3_DQ4	17
PS_DDR_DQ9_502_A27	A27	PS_DDR3_DQ8	18
PS_DDR_DQ8_502_A29	A29	PS_DDR3_DQ10	18
PS_DDR_DQ11_502_A28	A28	PS_DDR3_DQ9	18
PS_DDR_DQ10_502_A30	A30	PS_DDR3_DQ13	18
PS_DDR_DM1_502_B30	B30	PS_DDR3_DM1	18
PS_DDR_DQS_N1_502_B29	B29	PS_DDR3_DQS1_N	18
PS_DDR_DQS_P1_502_C29	C29	PS_DDR3_DQS1_P	18
PS_DDR_DQ13_502_D30	D30	PS_DDR3_DQ12	18
PS_DDR_DQ12_502_C28	C28	PS_DDR3_DQ11	18
PS_DDR_DQ15_502_D29	D29	PS_DDR3_DQ14	18
PS_DDR_DQ14_502_D28	D28	PS_DDR3_DQ15	18
PS_DDR_A13_502_H23	H23	PS_DDR3_A13	17,18,19,20
PS_DDR_A14_502_J24	J24	PS_DDR3_A14	17,18,19,20
PS_DDR_A11_502_H24	H24	PS_DDR3_A11	17,18,19,20
PS_DDR_A12_502_K23	K23	PS_DDR3_A12	17,18,19,20
PS_DDR_A9_502_J23	J23	PS_DDR3_A9	17,18,19,20
PS_DDR_A10_502_G26	G26	PS_DDR3_A10	17,18,19,20
PS_DDR_A7_502_K22	K22	PS_DDR3_A7	17,18,19,20
PS_DDR_A8_502_F27	F27	PS_DDR3_A8	17,18,19,20
PS_DDR_A5_502_G24	G24	PS_DDR3_A5	17,18,19,20
PS_DDR_A6_502_H26	H26	PS_DDR3_A6	17,18,19,20
PS_DDR_A3_502_G25	G25	PS_DDR3_A3	17,18,19,20
PS_DDR_A4_502_J26	J26	PS_DDR3_A4	17,18,19,20
PS_DDR_VRP_502_M21	M21	PS_VRP	10
PS_DDR_VRN_502_N21	N21	PS_VRN	10
PS_DDR_CKP_502_K25	K25	PS_DDR3_CLK_P	17,18,19,20
PS_DDR_CKN_502_J25	J25	PS_DDR3_CLK_N	17,18,19,20
PS_DDR_A2_502_L27	L27	PS_DDR3_A2	17,18,19,20
PS_DDR_A1_502_K26	K26	PS_DDR3_A1	17,18,19,20
PS_DDR_A0_502_L25	L25	PS_DDR3_A0	17,18,19,20
PS_DDR_BA2_502_M25	M25	PS_DDR3_BA2	17,18,19,20
PS_DDR_BA1_502_M26	M26	PS_DDR3_BA1	17,18,19,20
PS_DDR_BA0_502_M27	M27	PS_DDR3_BA0	17,18,19,20
PS_DDR_ODT_502_L23	L23	PS_DDR3_ODT	17,18,19,20
PS_DDR_CS_B_502_N22	N22	PS_DDR3_CS_B	17,18,19,20
PS_DDR_CKE_502_M22	M22	PS_DDR3_CKE	17,18,19,20
PS_DDR_WE_B_502_N23	N23	PS_DDR3_WE_B	17,18,19,20
PS_DDR_CAS_B_502_M24	M24	PS_DDR3_CAS_B	17,18,19,20
PS_DDR_RAS_B_502_N24	N24	PS_DDR3_RAS_B	17,18,19,20
PS_DDR_DQ16_502_H27	H27	PS_DDR3_DQ16	19
PS_DDR_DQ17_502_G27	G27	PS_DDR3_DQ17	19
PS_DDR_DQ18_502_H28	H28	PS_DDR3_DQ18	19
PS_DDR_DQ19_502_E28	E28	PS_DDR3_DQ19	19
PS_DDR_DM2_502_H29	H29	PS_DDR3_DM2	19
PS_DDR_DQS_P2_502_G29	G29	PS_DDR3_DQS2_P	19
PS_DDR_DQS_N2_502_F29	F29	PS_DDR3_DQS2_N	19
PS_DDR_DQ20_502_E30	E30	PS_DDR3_DQ20	19
PS_DDR_DQ21_502_F28	F28	PS_DDR3_DQ21	19
PS_DDR_DQ22_502_G30	G30	PS_DDR3_DQ22	19
PS_DDR_DQ23_502_F30	F30	PS_DDR3_DQ23	19
PS_DDR_DQ24_502_J29	J29	PS_DDR3_DQ27	20
PS_DDR_DQ25_502_K27	K27	PS_DDR3_DQ24	20
PS_DDR_DQ26_502_J30	J30	PS_DDR3_DQ25	20
PS_DDR_DQ27_502_J28	J28	PS_DDR3_DQ26	20
PS_DDR_DM3_502_K28	K28	PS_DDR3_DM3	20
PS_DDR_DQS_P3_502_L28	L28	PS_DDR3_DQS3_P	20
PS_DDR_DQS_N3_502_L29	L29	PS_DDR3_DQS3_N	20
PS_DDR_DQ28_502_K30	K30	PS_DDR3_DQ28	20
PS_DDR_DQ29_502_M29	M29	PS_DDR3_DQ29	20
PS_DDR_DQ30_502_L30	L30	PS_DDR3_DQ30	20
PS_DDR_DQ31_502_M30	M30	PS_DDR3_DQ31	20
PS_DDR_VREF0_502_L22	L22		
PS_DDR_VREF1_502_L24	L24		

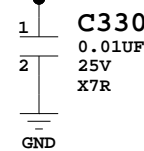
VCC1V5_PS

A26	VCCO_DDR_502_A26
C30	VCCO_DDR_502_C30
D27	VCCO_DDR_502_D27
G28	VCCO_DDR_502_G28
H25	VCCO_DDR_502_H25
K29	VCCO_DDR_502_K29
L26	VCCO_DDR_502_L26
M23	VCCO_DDR_502_M23

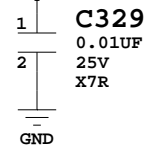
U1

SOC_IRONWOOD_FF900

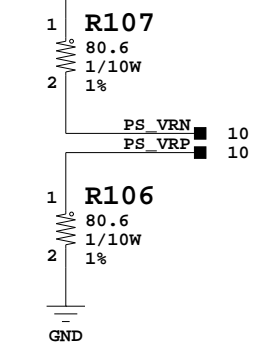
VTTVREF_PS



VTTVREF_PS



VCC1V5_PS



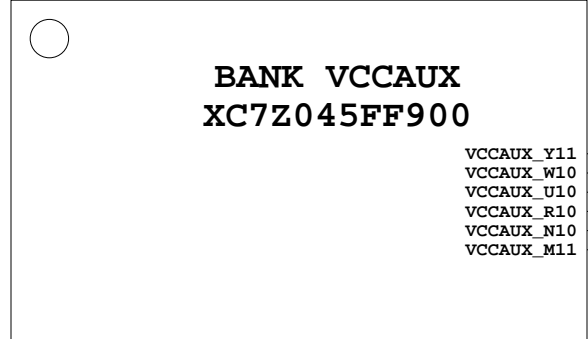
Zynq Bank 502



Title: Zynq Bank 502 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM
 ASSY P/N: 0431760
 PCB P/N: 1280681
 SCH P/N: 0381513

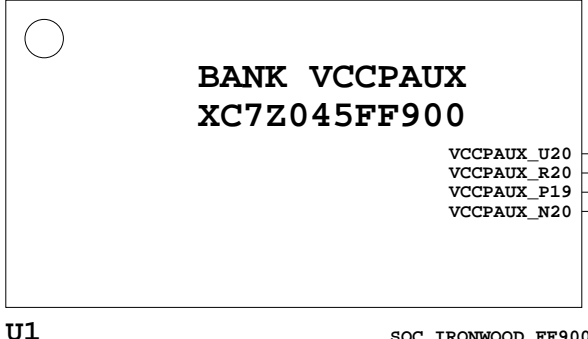
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	10 of 58	Drawn By	BF

SOC_Z7_FF900_IRONWOOD



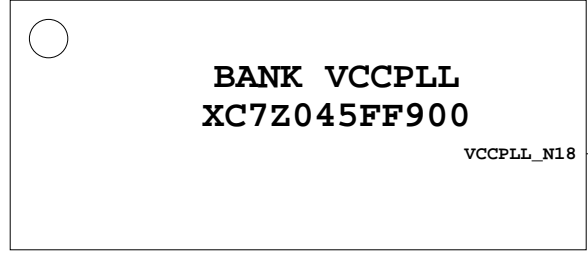
U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD

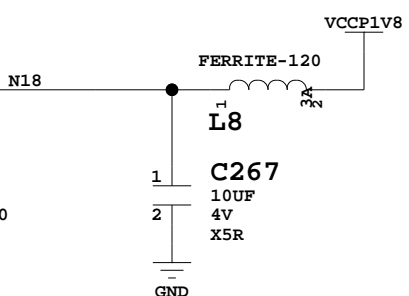


U1 SOC_IRONWOOD_FF900

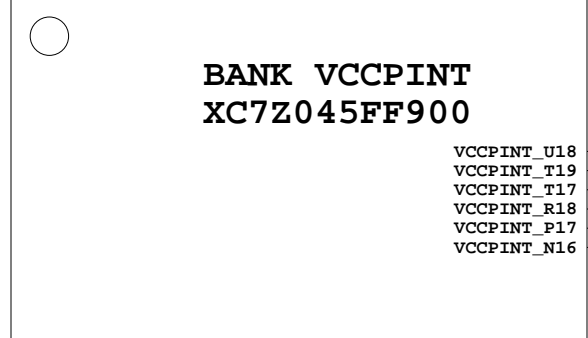
SOC_Z7_FF900_IRONWOOD



U1 SOC_IRONWOOD_FF900

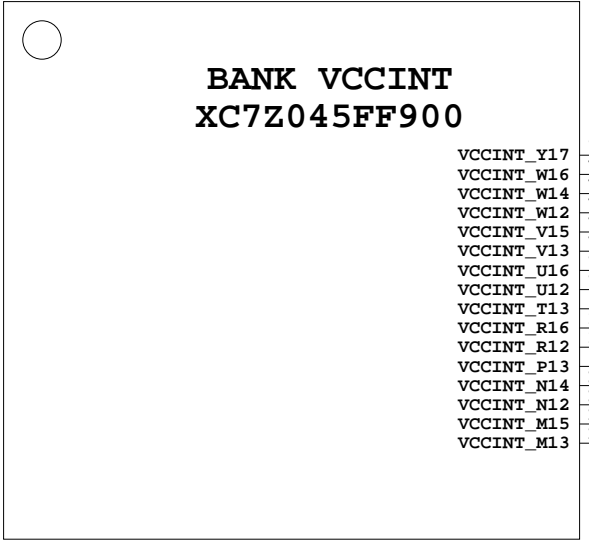


SOC_Z7_FF900_IRONWOOD



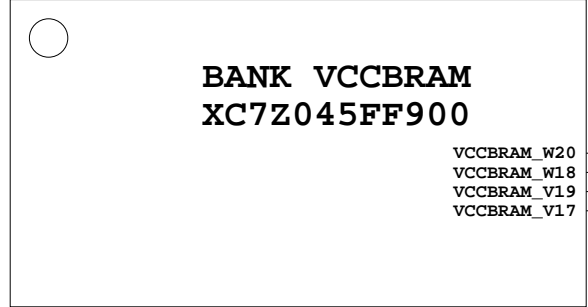
U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD



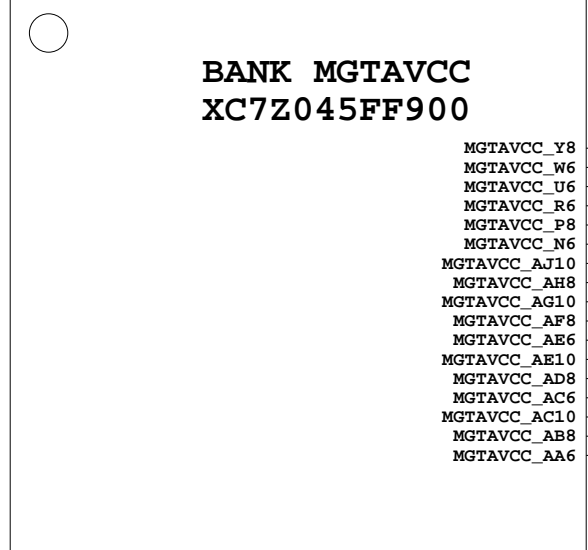
U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD



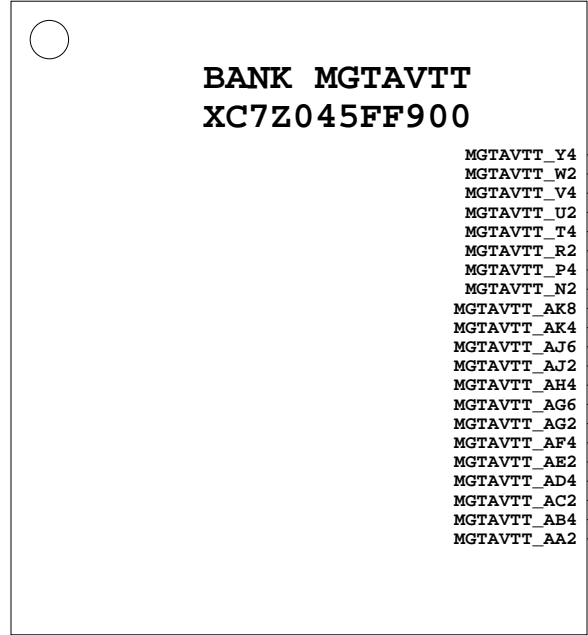
U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD



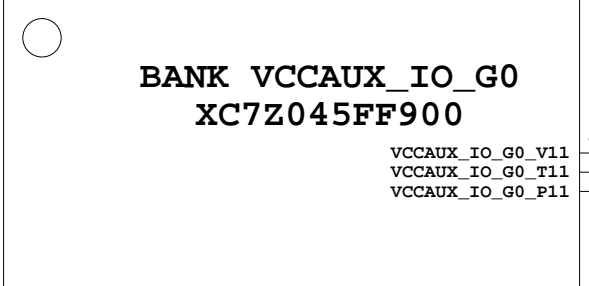
U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD



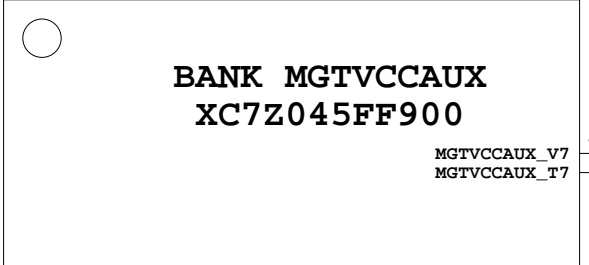
U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD



U1 SOC_IRONWOOD_FF900

SOC_Z7_FF900_IRONWOOD



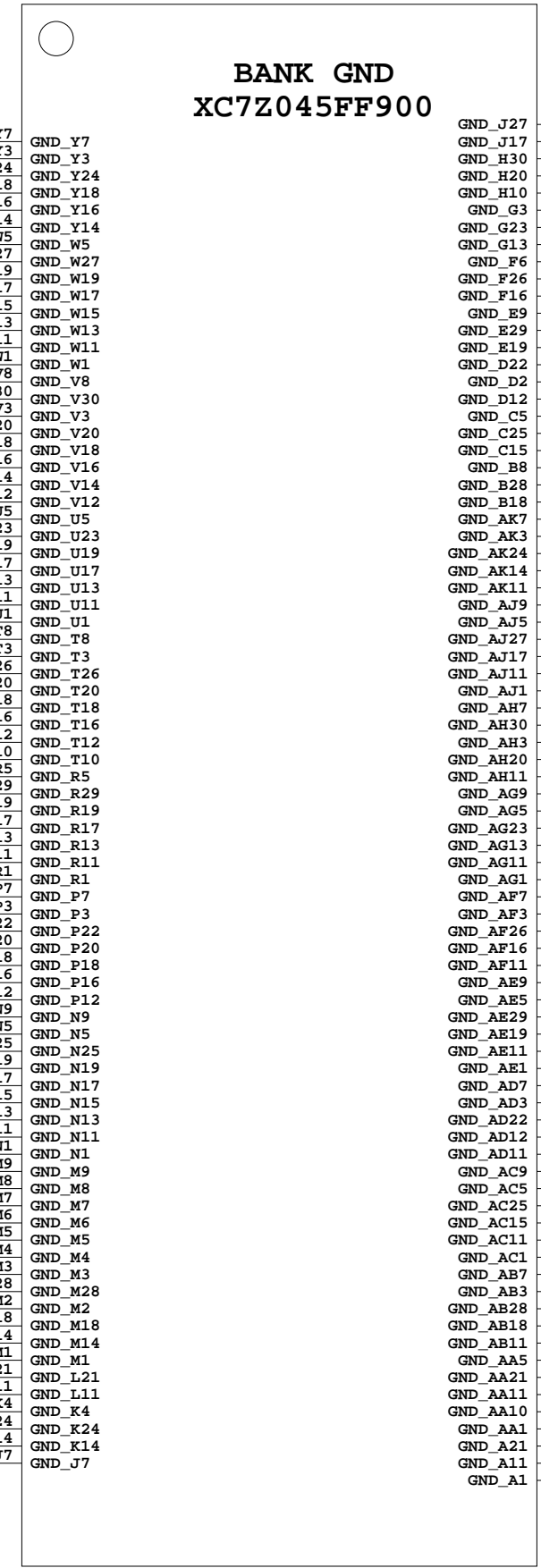
U1 SOC_IRONWOOD_FF900

Zynq Power Pins



Title: Zynq Power Pins SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 11 of 58	Drawn By BF	

SOC_Z7_FF900_IRONWOOD



- Y7 GND_Y7
- Y3 GND_Y3
- Y24 GND_Y24
- Y18 GND_Y18
- Y16 GND_Y16
- Y14 GND_Y14
- W5 GND_W5
- W27 GND_W27
- W19 GND_W19
- W17 GND_W17
- W15 GND_W15
- W13 GND_W13
- W11 GND_W11
- W1 GND_W1
- V8 GND_V8
- V30 GND_V30
- V3 GND_V3
- V20 GND_V20
- V18 GND_V18
- V16 GND_V16
- V14 GND_V14
- V12 GND_V12
- U5 GND_U5
- U23 GND_U23
- U19 GND_U19
- U17 GND_U17
- U13 GND_U13
- U11 GND_U11
- U1 GND_U1
- T8 GND_T8
- T3 GND_T3
- T26 GND_T26
- T20 GND_T20
- T18 GND_T18
- T16 GND_T16
- T12 GND_T12
- T10 GND_T10
- R5 GND_R5
- R29 GND_R29
- R19 GND_R19
- R17 GND_R17
- R13 GND_R13
- R11 GND_R11
- R1 GND_R1
- P7 GND_P7
- P3 GND_P3
- P22 GND_P22
- P20 GND_P20
- P18 GND_P18
- P16 GND_P16
- P12 GND_P12
- N9 GND_N9
- N5 GND_N5
- N25 GND_N25
- N19 GND_N19
- N17 GND_N17
- N15 GND_N15
- N13 GND_N13
- N11 GND_N11
- N1 GND_N1
- M9 GND_M9
- M8 GND_M8
- M7 GND_M7
- M6 GND_M6
- M5 GND_M5
- M4 GND_M4
- M3 GND_M3
- M28 GND_M28
- M2 GND_M2
- M18 GND_M18
- M14 GND_M14
- M1 GND_M1
- L21 GND_L21
- L11 GND_L11
- K4 GND_K4
- K24 GND_K24
- K14 GND_K14
- J7 GND_J7

- GND_J27
- GND_J17
- GND_H30
- GND_H20
- GND_H10
- GND_G3
- GND_G23
- GND_G13
- GND_F6
- GND_F26
- GND_F16
- GND_E9
- GND_E29
- GND_E19
- GND_D22
- GND_D2
- GND_D12
- GND_C5
- GND_C25
- GND_C15
- GND_B8
- GND_B28
- GND_B18
- GND_AK7
- GND_AK3
- GND_AK24
- GND_AK14
- GND_AK11
- GND_AJ9
- GND_AJ5
- GND_AJ27
- GND_AJ17
- GND_AJ11
- GND_AJ1
- GND_AH7
- GND_AH30
- GND_AH3
- GND_AH20
- GND_AH11
- GND_AG9
- GND_AG5
- GND_AG23
- GND_AG13
- GND_AG11
- GND_AG1
- GND_AF7
- GND_AF3
- GND_AF26
- GND_AF16
- GND_AF11
- GND_AE9
- GND_AE5
- GND_AE29
- GND_AE19
- GND_AE11
- GND_AE1
- GND_AD7
- GND_AD3
- GND_AD22
- GND_AD12
- GND_AD11
- GND_AC9
- GND_AC5
- GND_AC25
- GND_AC15
- GND_AC11
- GND_AC1
- GND_AB7
- GND_AB3
- GND_AB28
- GND_AB18
- GND_AB11
- GND_AA5
- GND_AA21
- GND_AA11
- GND_AA10
- GND_AA1
- GND_A21
- GND_A11
- GND_A1

- J27
- J17
- H30
- H20
- H10
- G3
- G23
- G13
- F6
- F26
- F16
- E9
- E29
- E19
- D22
- D2
- D12
- C5
- C25
- C15
- B8
- B28
- B18
- AK7
- AK3
- AK24
- AK14
- AK11
- AJ9
- AJ5
- AJ27
- AJ17
- AJ11
- AJ1
- AH7
- AH30
- AH3
- AH20
- AH11
- AG9
- AG5
- AG23
- AG13
- AG11
- AG1
- AF7
- AF3
- AF26
- AF16
- AF11
- AE9
- AE5
- AE29
- AE19
- AE11
- AE1
- AD7
- AD3
- AD22
- AD12
- AD11
- AC9
- AC5
- AC25
- AC15
- AC11
- AC1
- AB7
- AB3
- AB28
- AB18
- AB11
- AA5
- AA21
- AA11
- AA10
- AA1
- A21
- A11
- A1

GND

GND

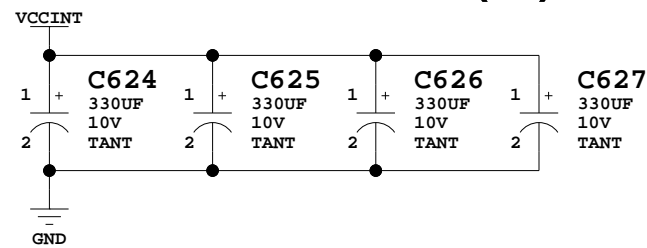
Zynq GND



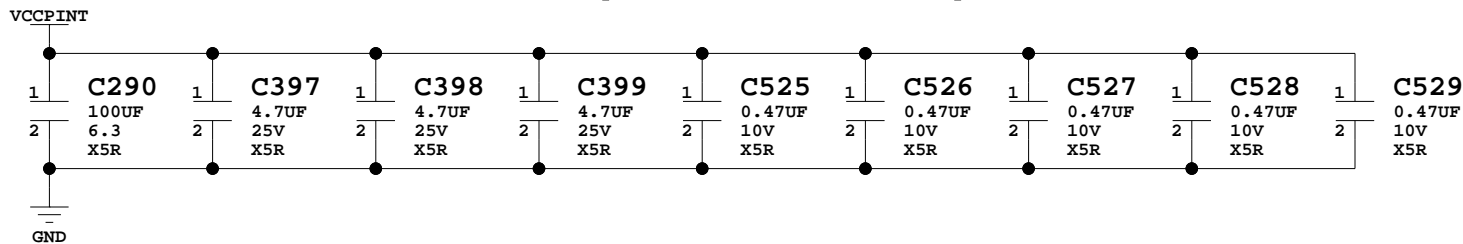
Title: Zynq GND SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 12 of 58	Drawn By BF	

BYPASS CAPACITORS

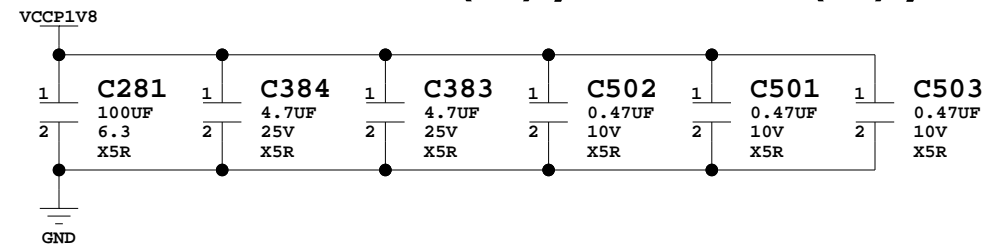
VCCINT 330uF (4)



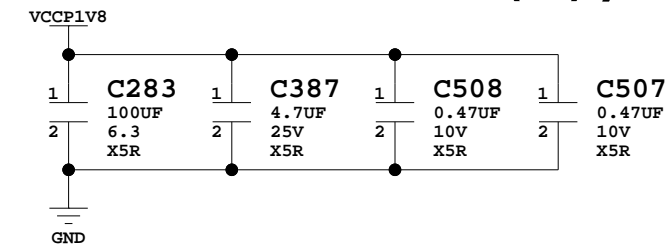
VCCPINT 100uF (1), 4.7uF (3), 0.47uF (5)



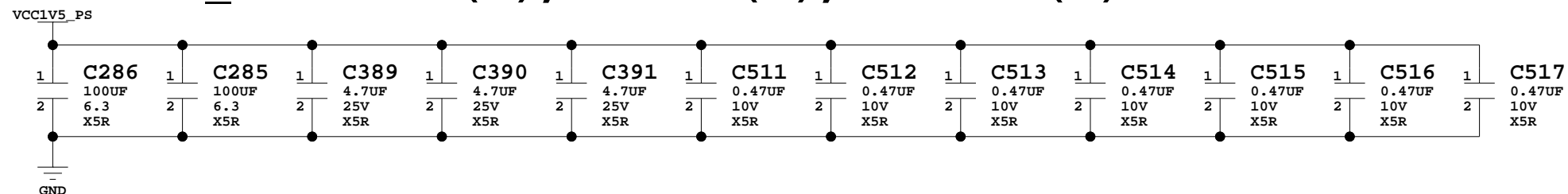
VCCPAUX 100uF (1), 4.7uF (2), 0.47uF (3)



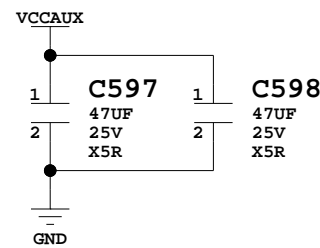
VCC0 PS 100uF (1), 4.7uF (1), 0.47uF (2)



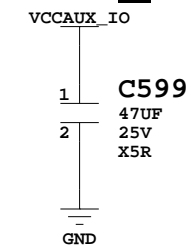
VCC1V5_PS 100uF (2), 4.7uF (3), 0.47uF (7)



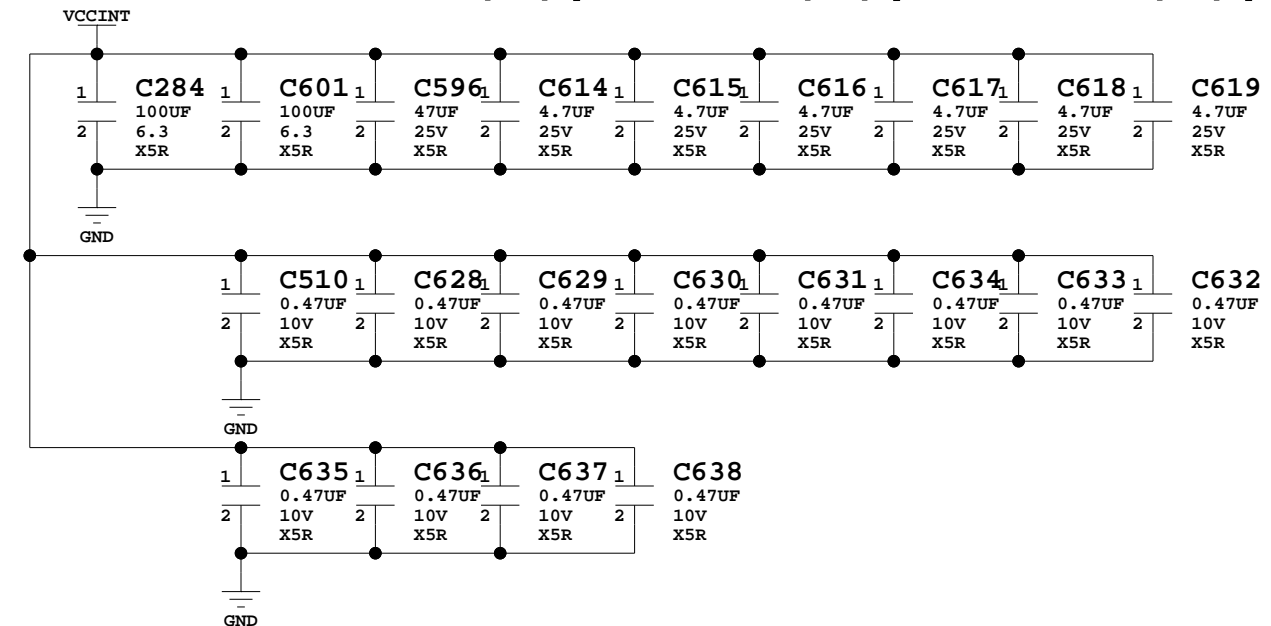
VCCAUX 47uF (2)



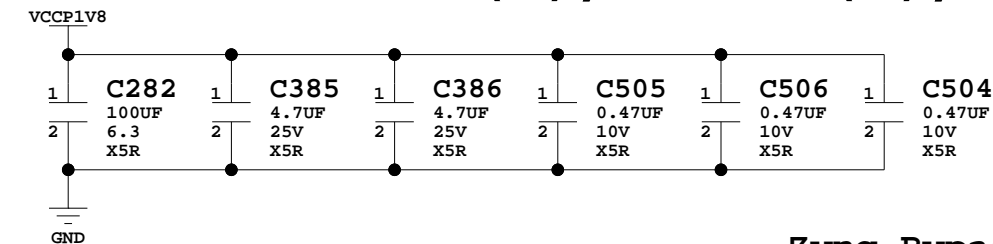
VCCAUX_IO 47uF (1)



VCCBRAM 100uF (2), 47uF (1), 4.7uF (6), 0.47uF (12)



VCCO P1 100uF (1), 4.7uF (2), 0.47uF (3)



Zynq Bypass Capacitors Page 1

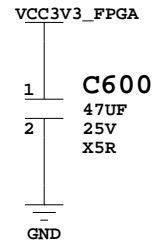


Title: Zynq Bypass Capacitors Page 1
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

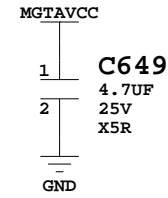
ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	13 of 58	Drawn By	BF

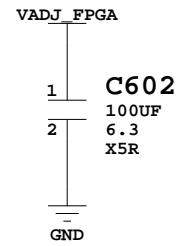
Bank 0 VCC3V3 100uF (1)



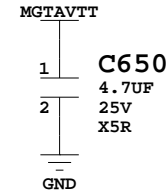
MGTAVCC 4.7uF (1)



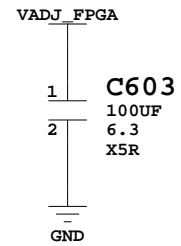
Bank 9 VADJ_FPGA 100uF (1)



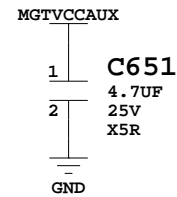
MGTAVTT 4.7uF (1)



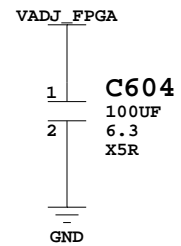
Bank 10 VADJ_FPGA 100uF (1)



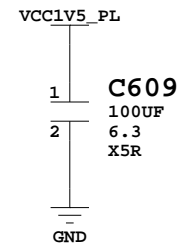
MGTVCCAUX 4.7uF (1)



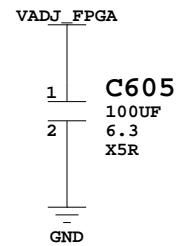
Bank 11 VADJ_FPGA 100uF (1)



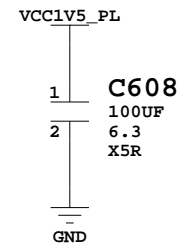
Bank 33 VCC1V5_PL 100uF (1)



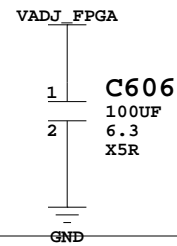
Bank 12 VADJ_FPGA 100uF (1)



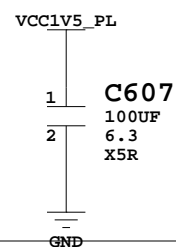
Bank 34 VCC1V5_PL 100uF (1)



Bank 13 VADJ_FPGA 100uF (1)



Bank 35 VCC1V5_PL 100uF (1)



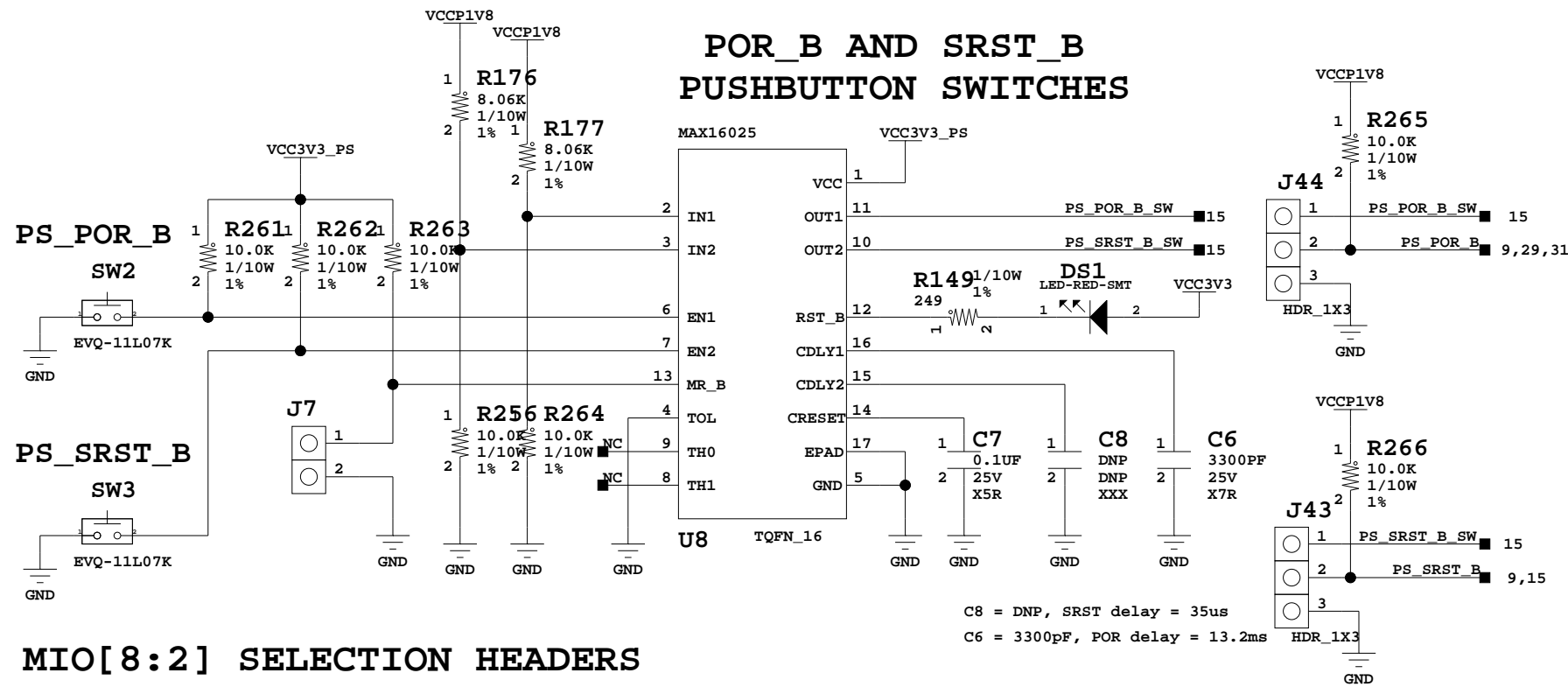
Zynq Bypass Capacitors Page 2



Title: Zynq Bypass Capacitors Page 2 ASSY P/N: 0431760
SCHEM, ROHS COMPLIANT PCB P/N: 1280681
ZC706 EVALUATION PLATFORM SCH P/N: 0381513

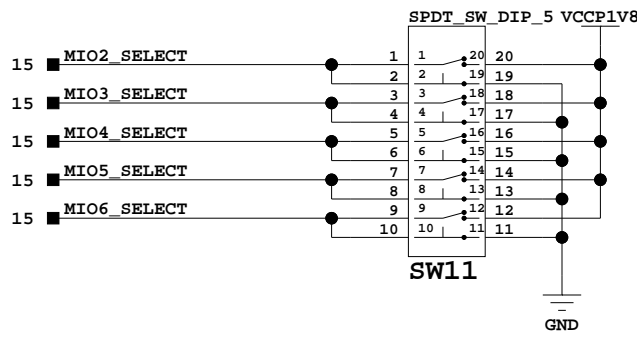
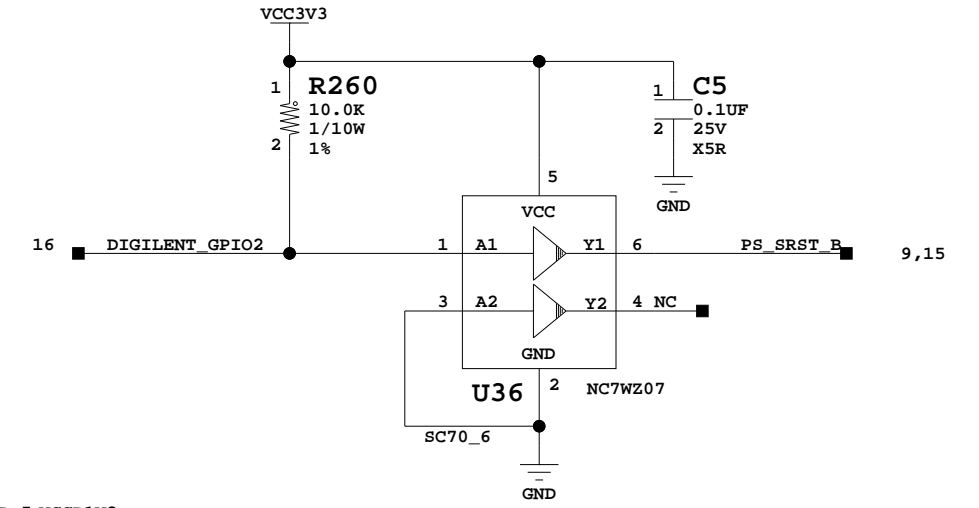
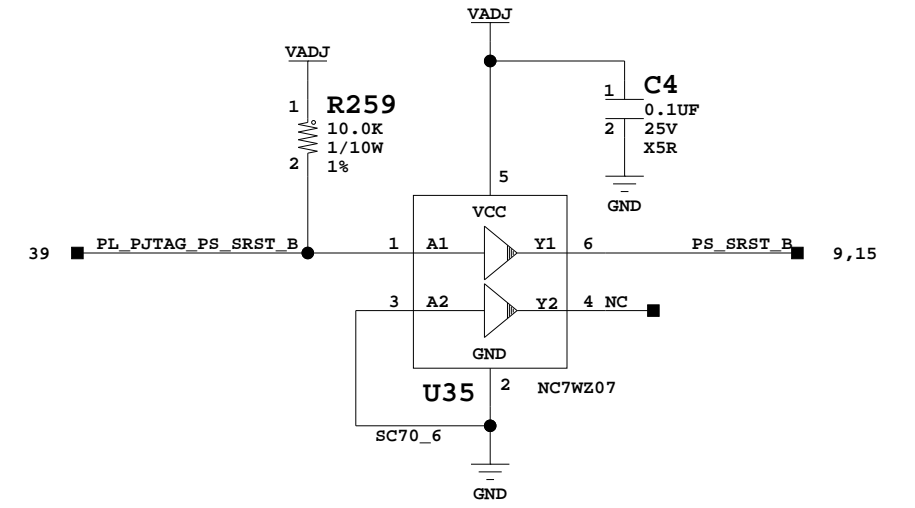
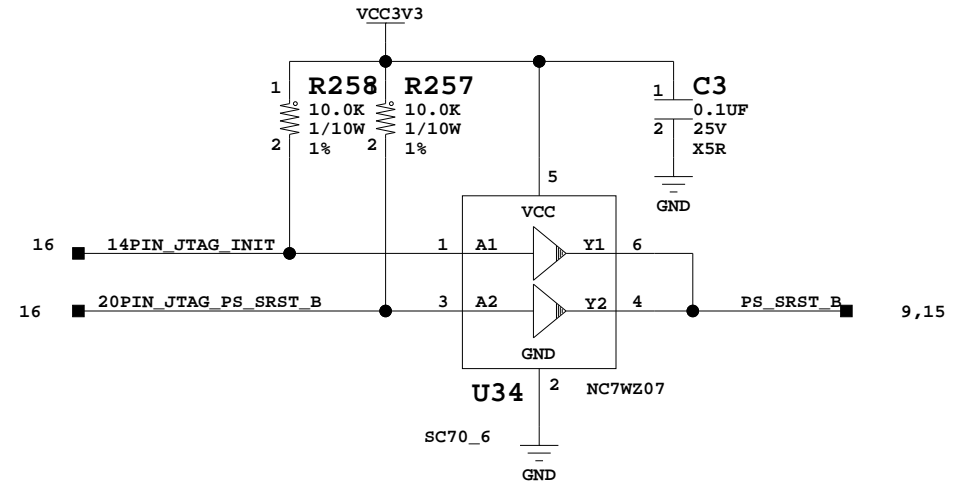
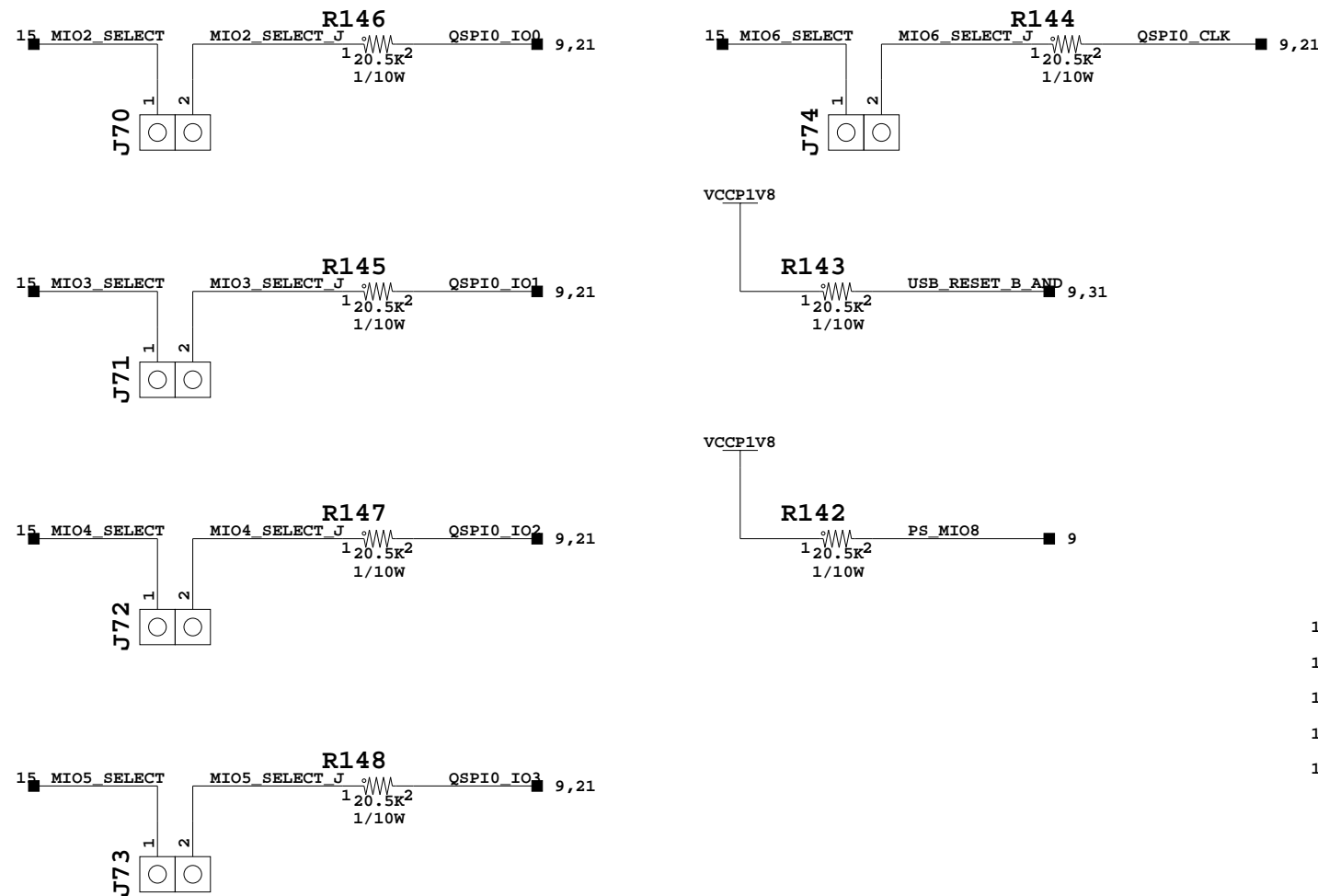
Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	14 of 58	Drawn By	BF

POR_B AND SRST_B PUSHBUTTON SWITCHES



MIO[8:2] SELECTION HEADERS

20.5K resistors must be placed near middle of QSPI traces

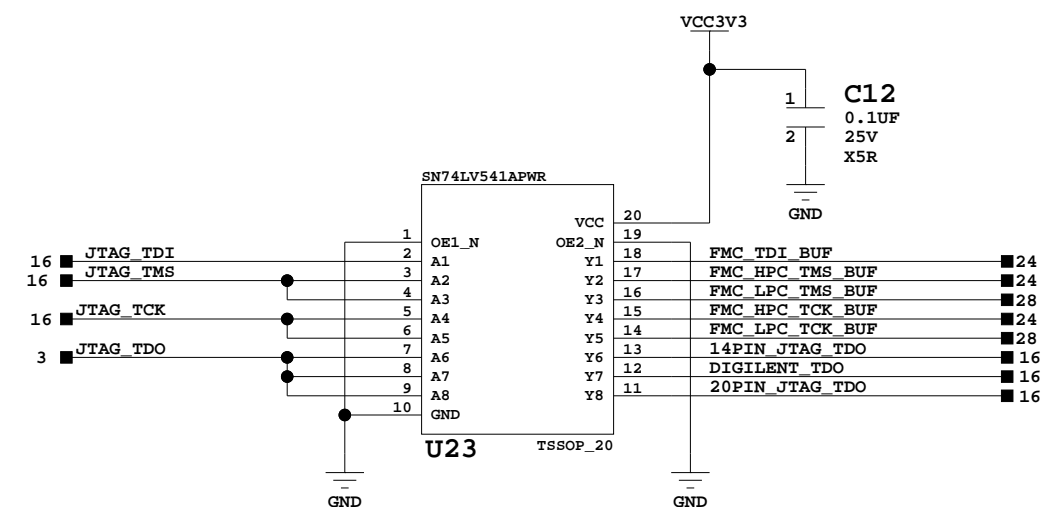
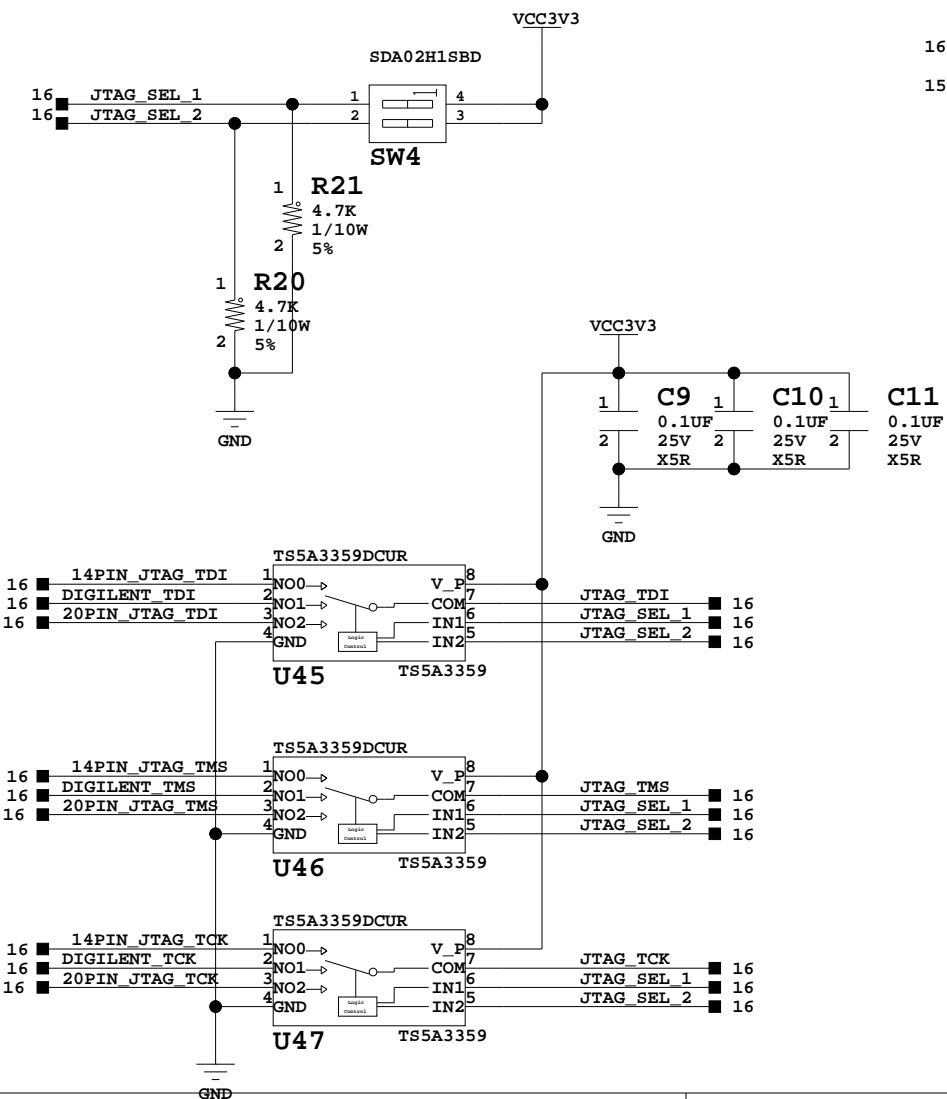
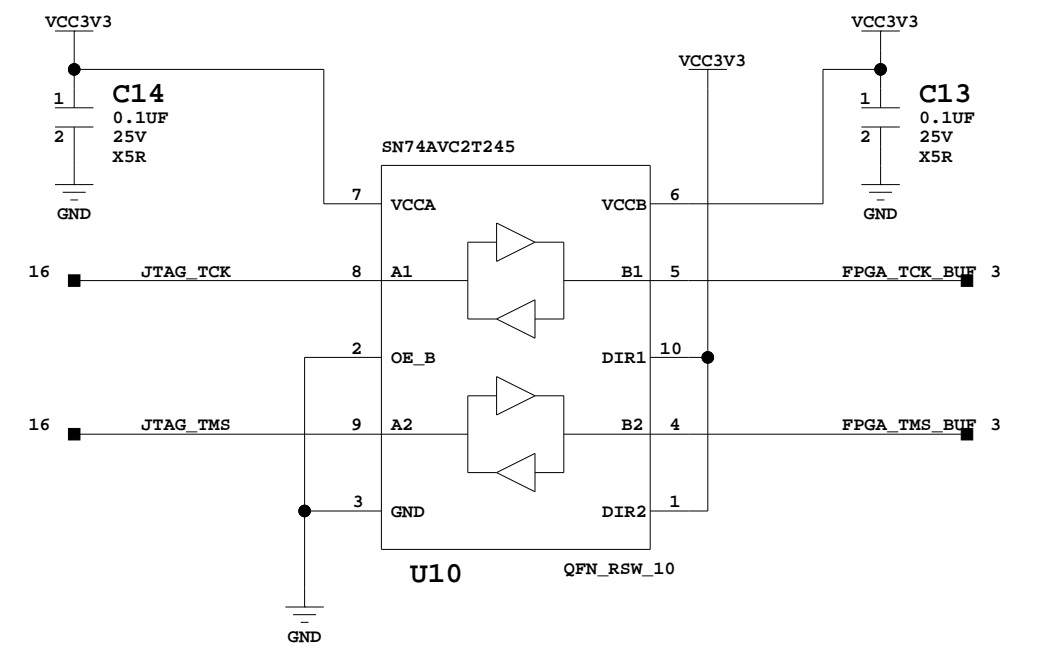
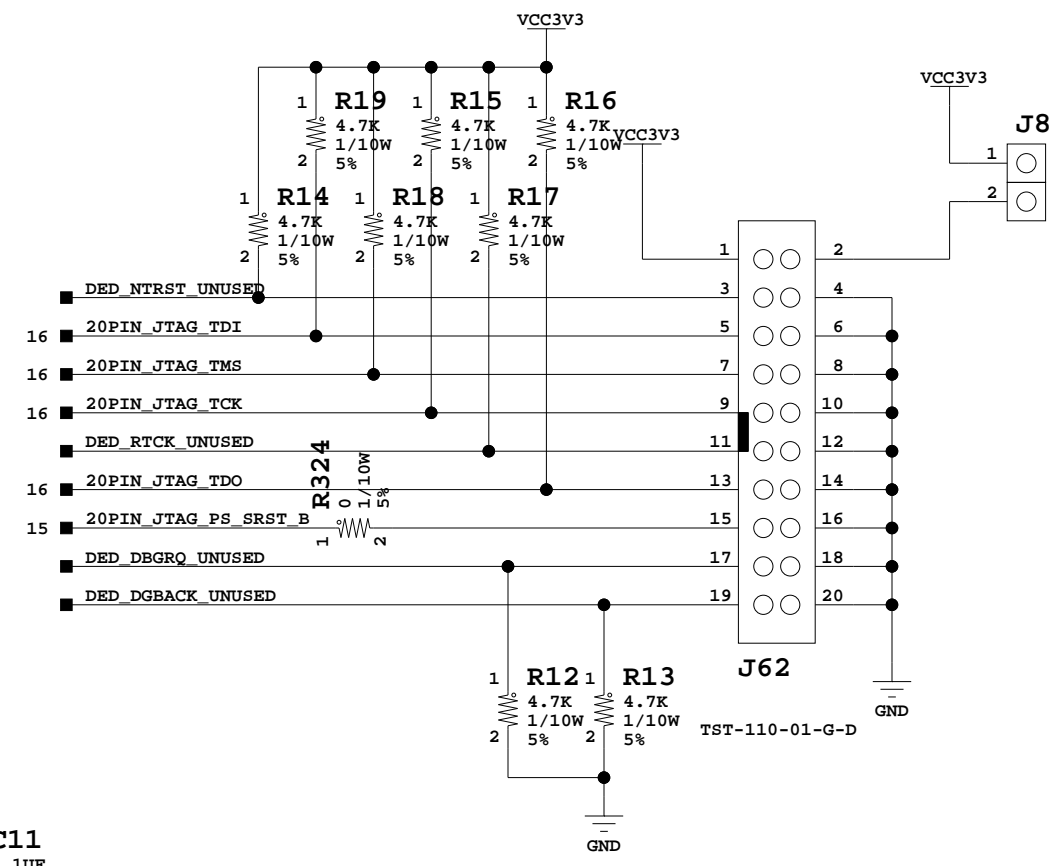
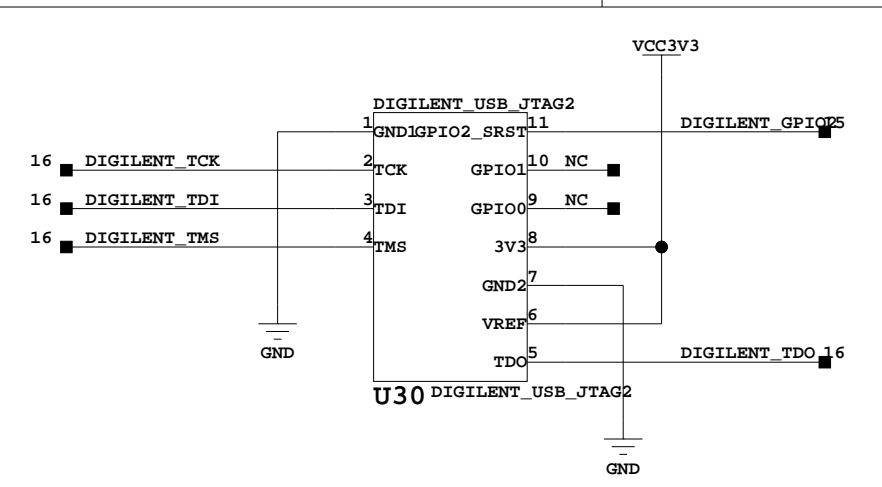
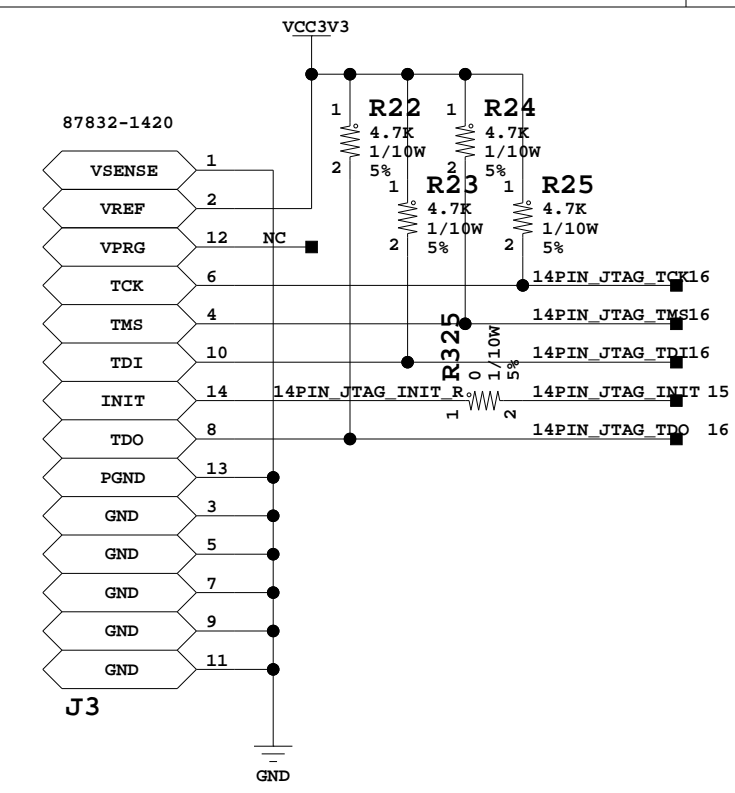


Power Supervisor, Zynq Config Pins, ResetASSY P/N: 0431760



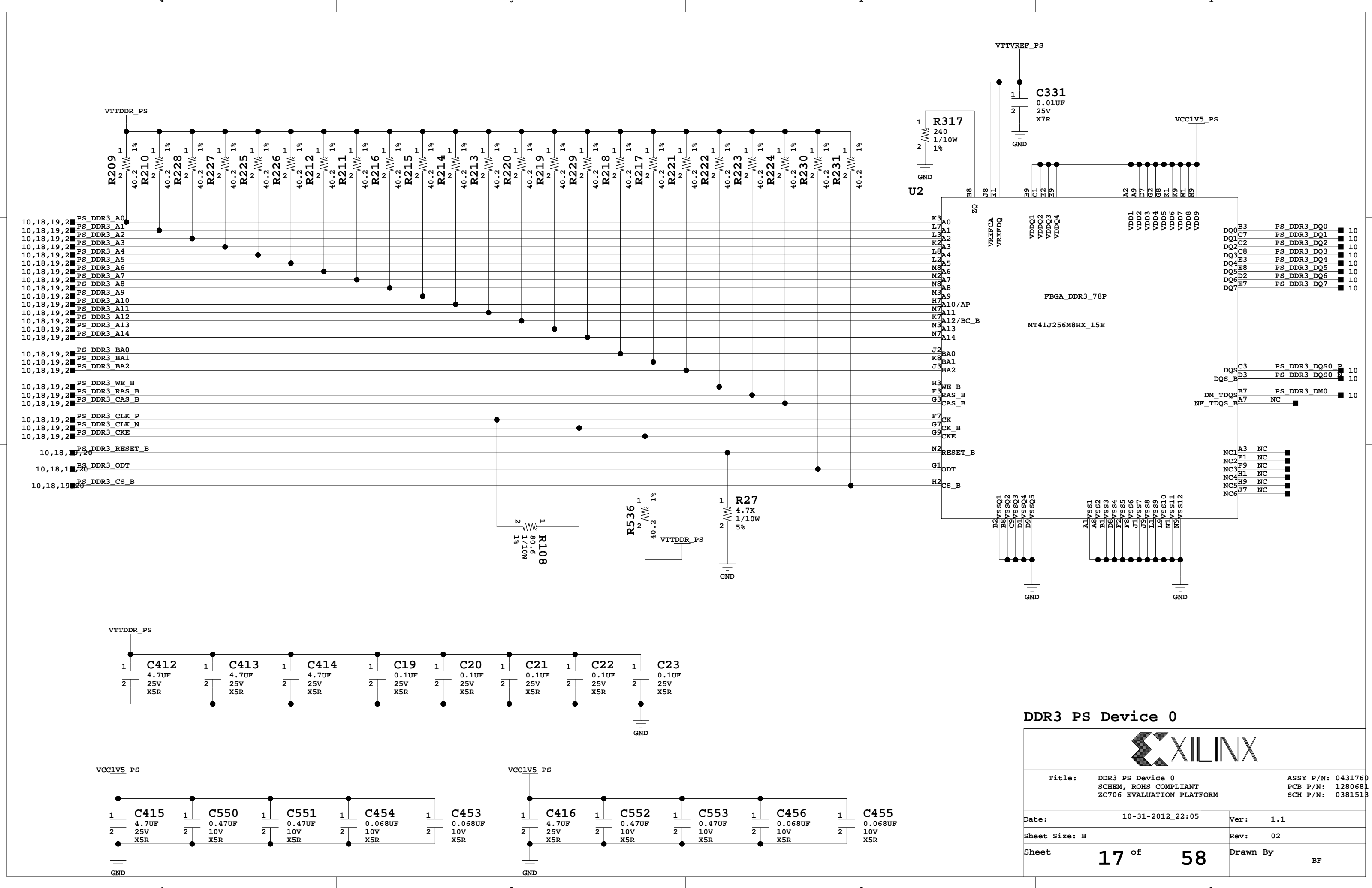
Title: Power Supervisor, Zynq Config Pins, ResetASSY P/N: 0431760
 SCHEM, ROHS COMPLIANT PCB P/N: 1280681
 ZC706 EVALUATION PLATFORM SCH P/N: 0381513

Date:	11-1-2012_18:19	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	15 of 58	Drawn By	BF



JTAG Buffer, USB JTAG Module, JTAG Hdr

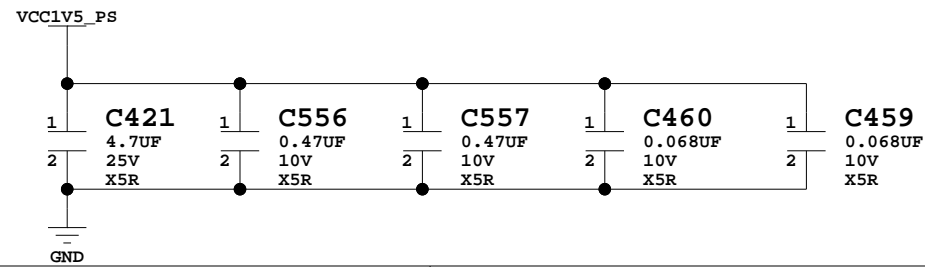
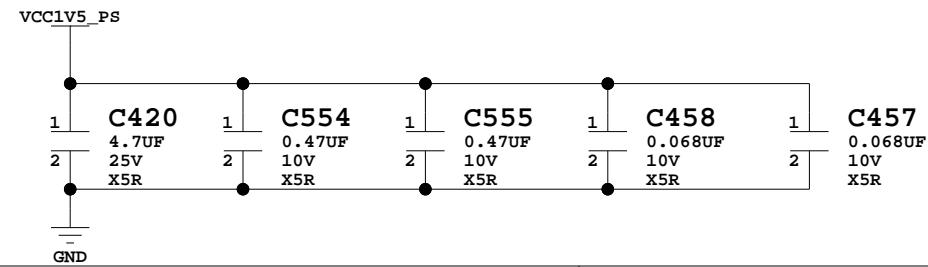
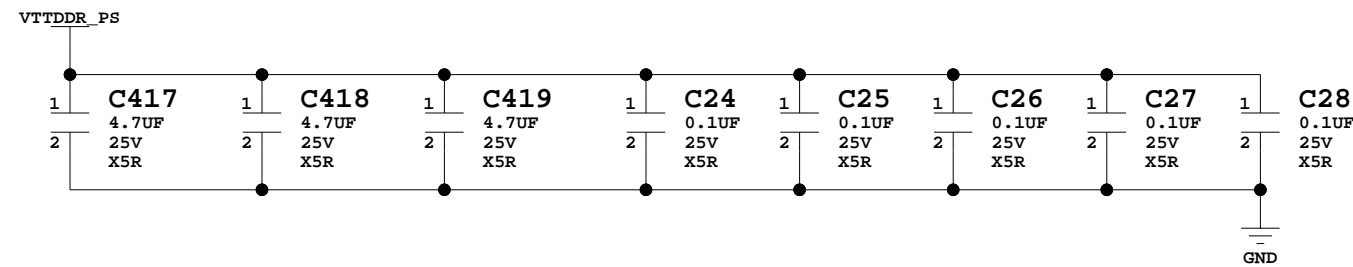
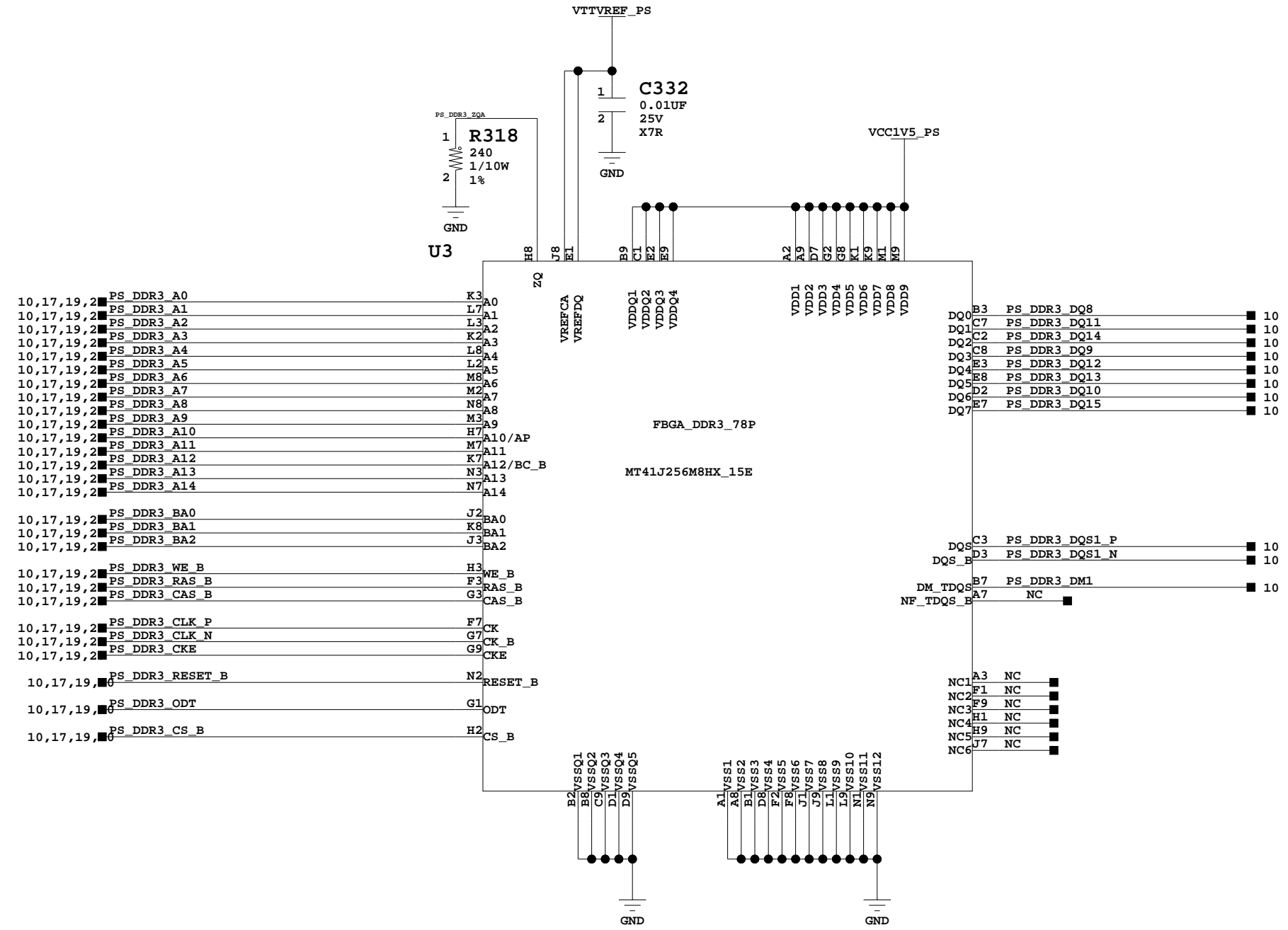
Title: JTAG Buffer, USB JTAG Module, JTAG Hdr ASSY P/N: 0431760 SCHEM, ROHS COMPLIANT PCB P/N: 1280681 ZC706 EVALUATION PLATFORM SCH P/N: 0381513	
Date: 10-31-2012_22:05	Ver: 1.1
Sheet Size: B	Rev: 02
Sheet 16 of 58	Drawn By BF



DDR3 PS Device 0



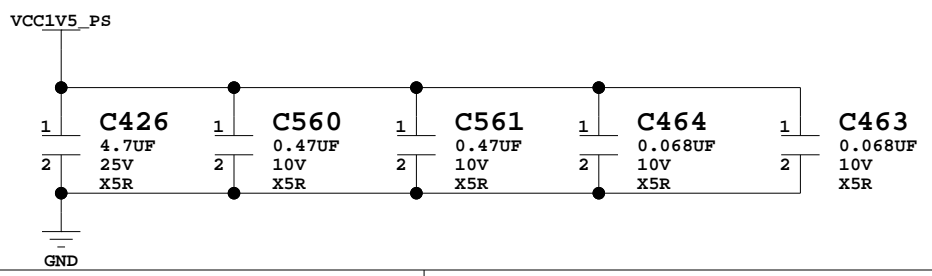
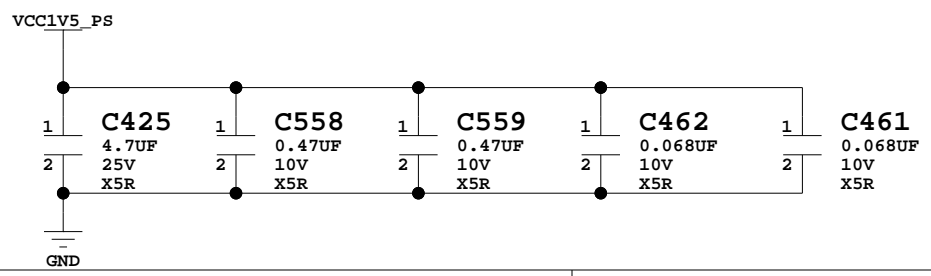
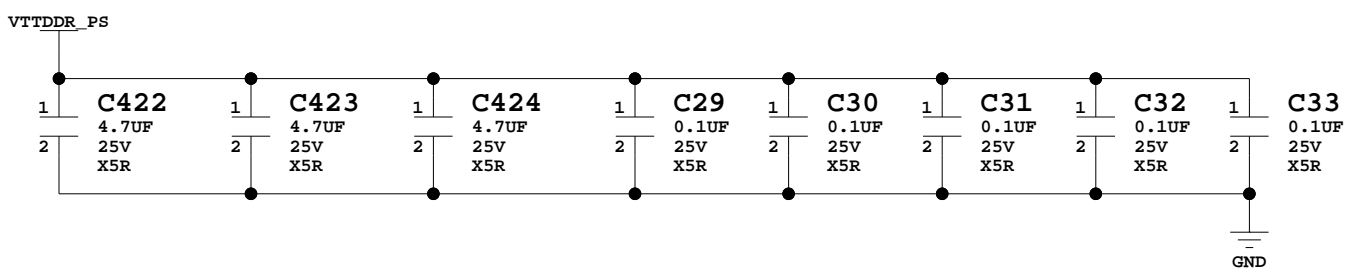
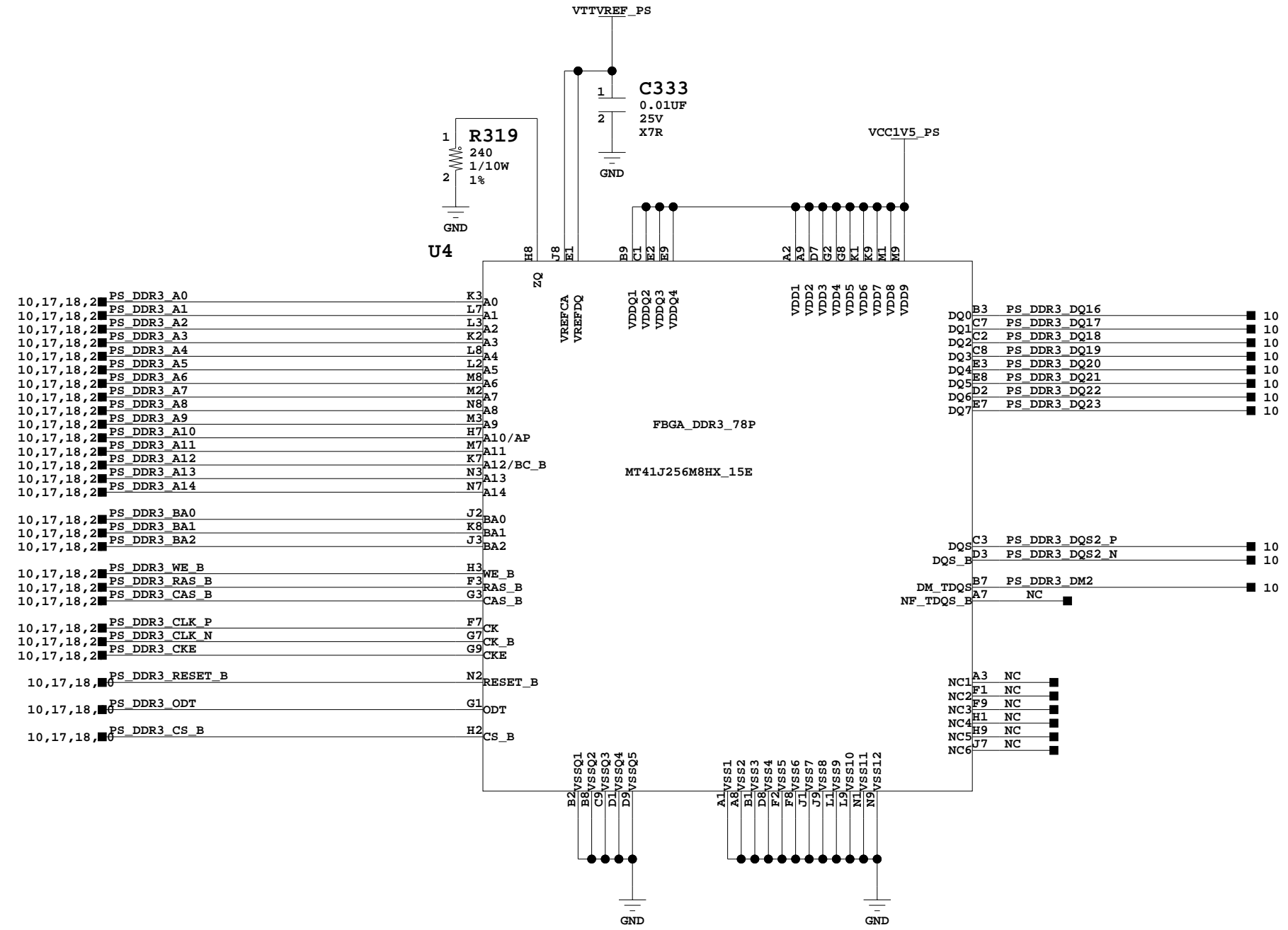
Title: DDR3 PS Device 0 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 17 of 58	Drawn By BF	



DDR3 PS Device 1



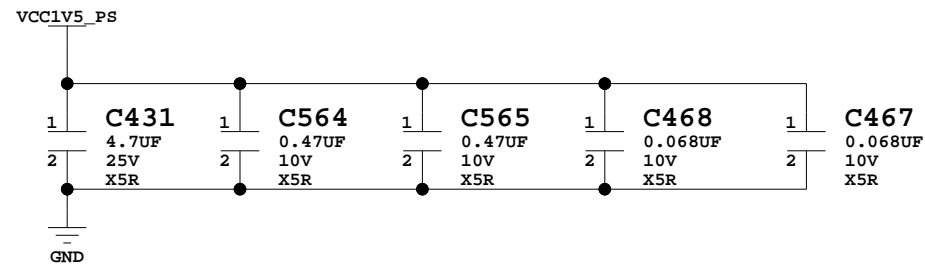
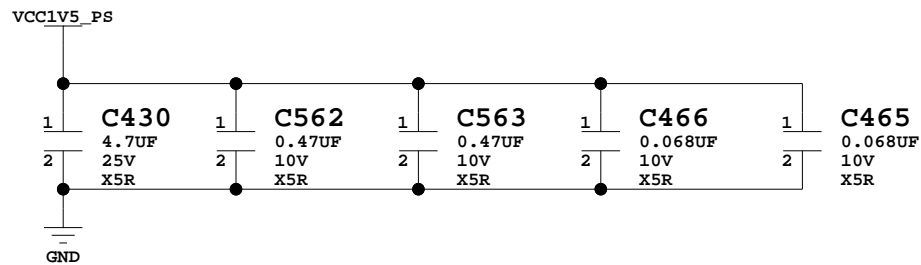
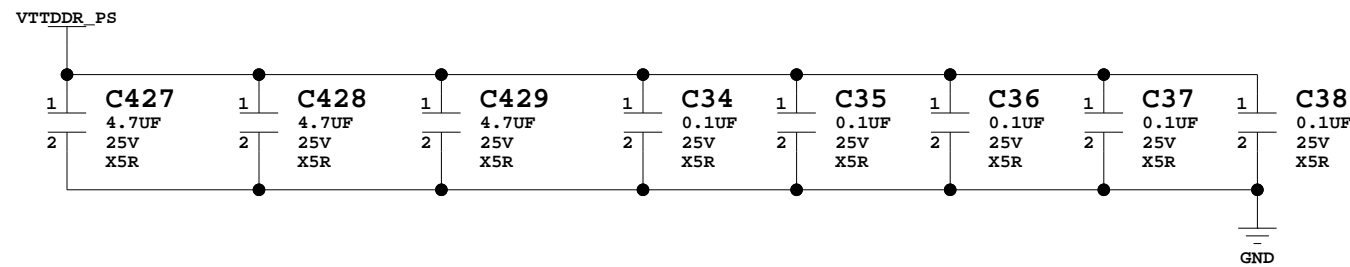
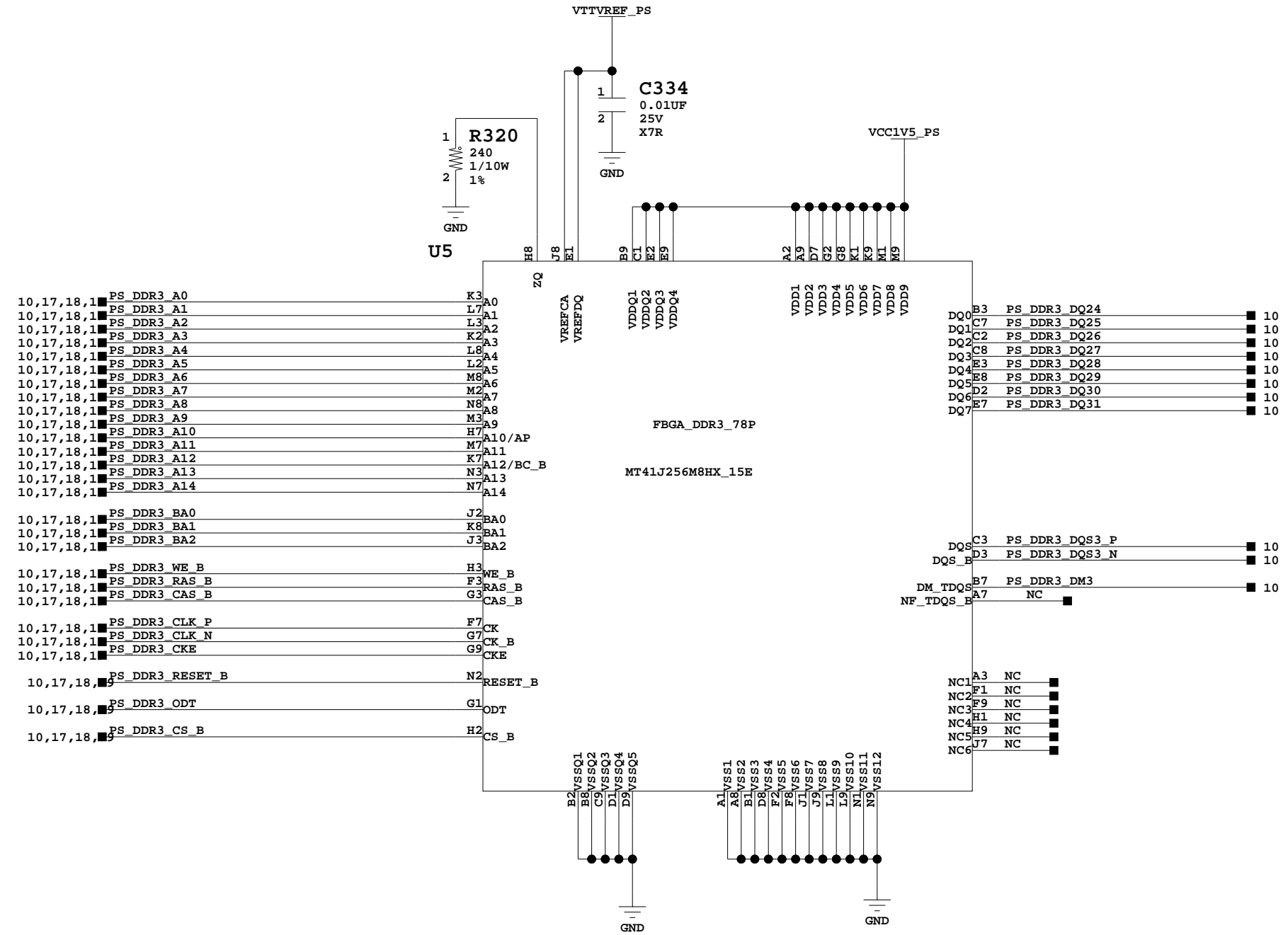
Title: DDR3 PS Device 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 18 of 58	Drawn By BF	



DDR3 PS Device 2



Title: DDR3 PS Device 2 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 19 of 58	Drawn By BF	



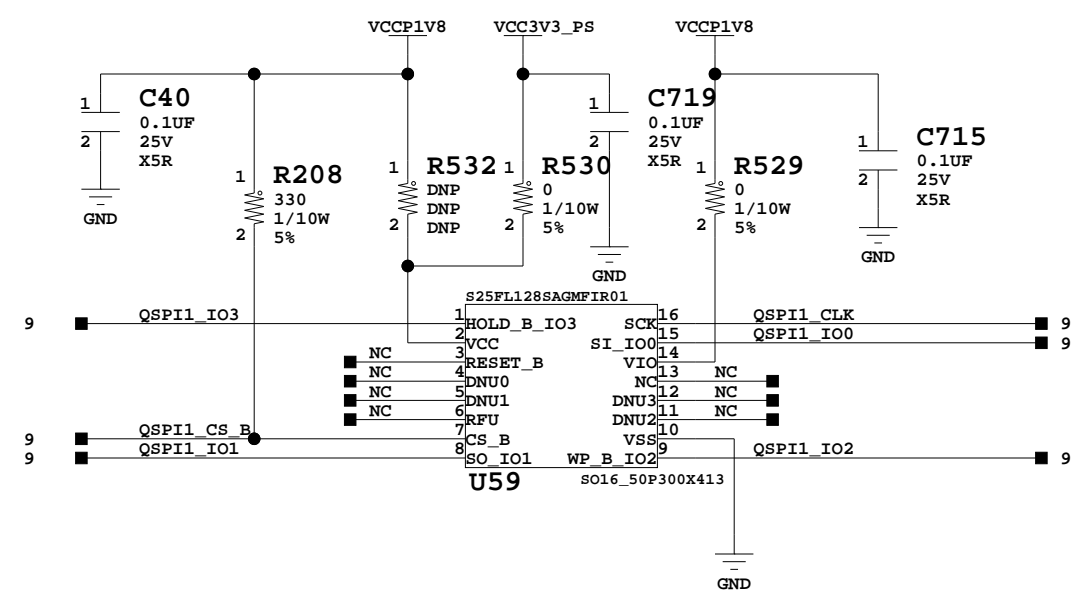
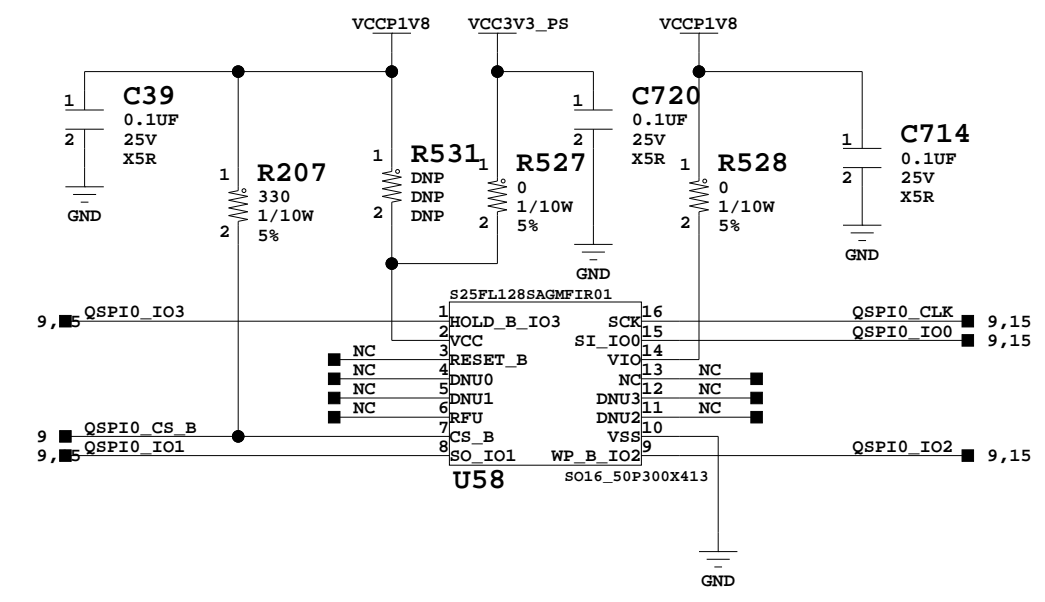
DDR3 PS Device 3



Title: DDR3 PS Device 3
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	20 of 58	Drawn By	BF

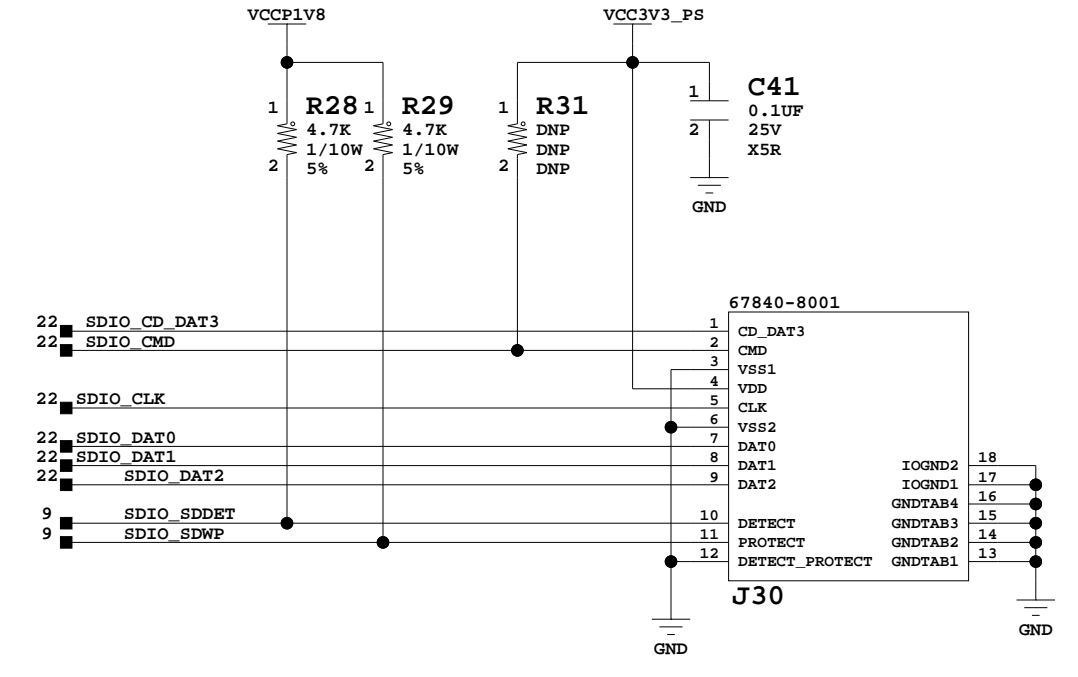
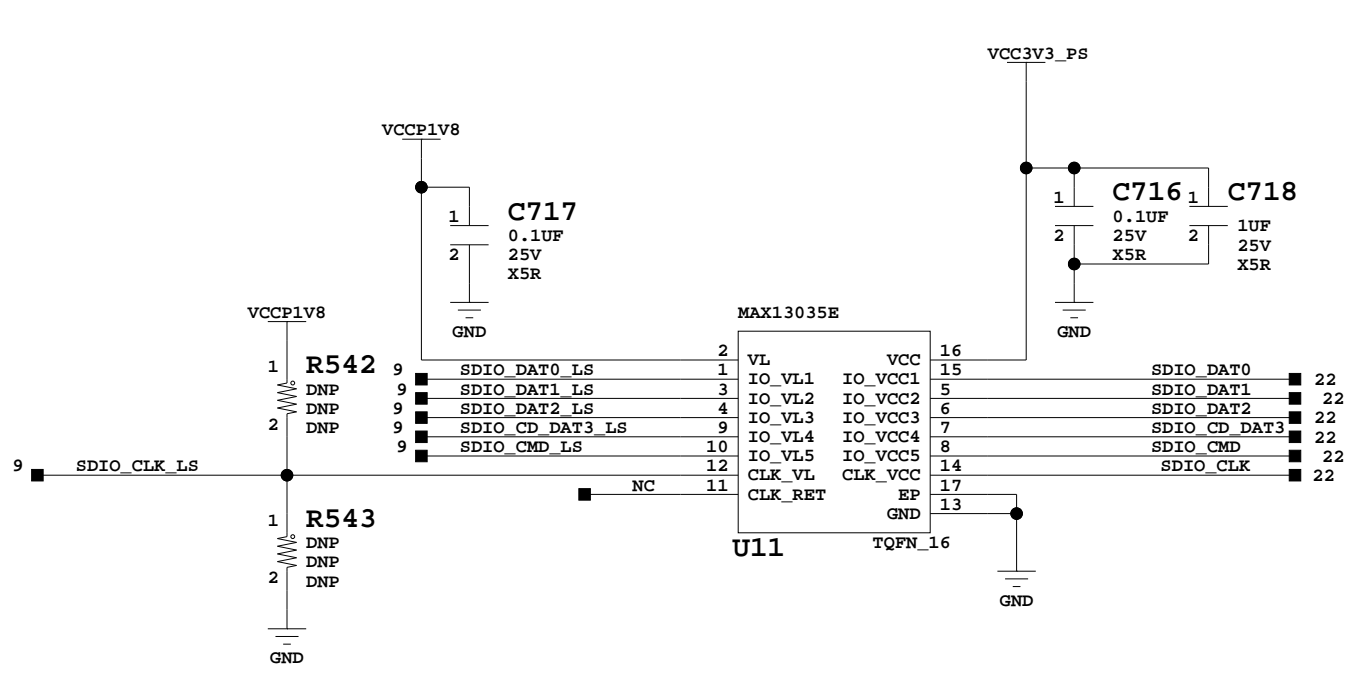


Dual Quad SPIs

Dual Quad SPIs



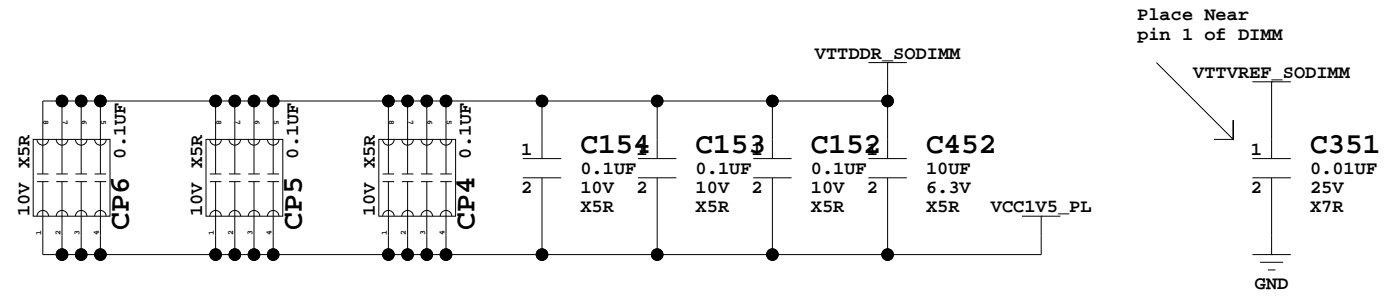
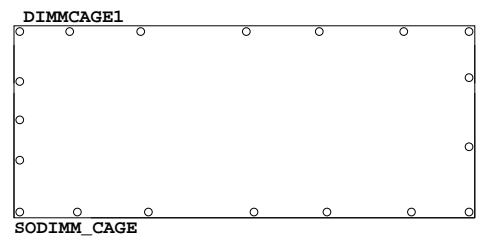
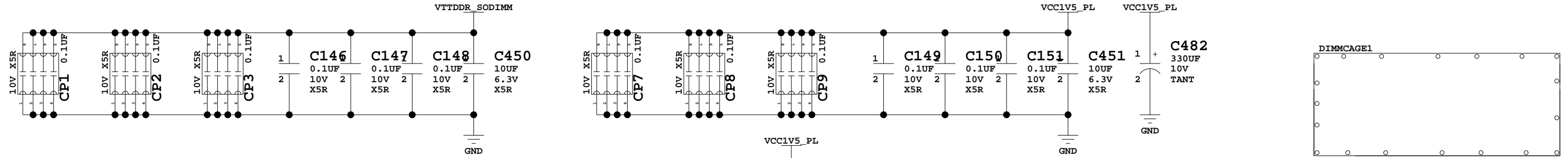
Title: Dual Quad SPIs SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 21 of 58	Drawn By BF	



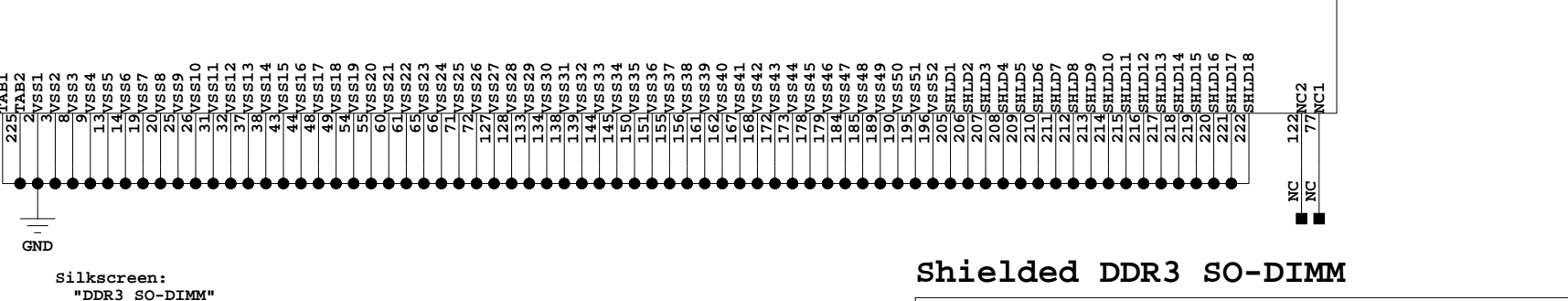
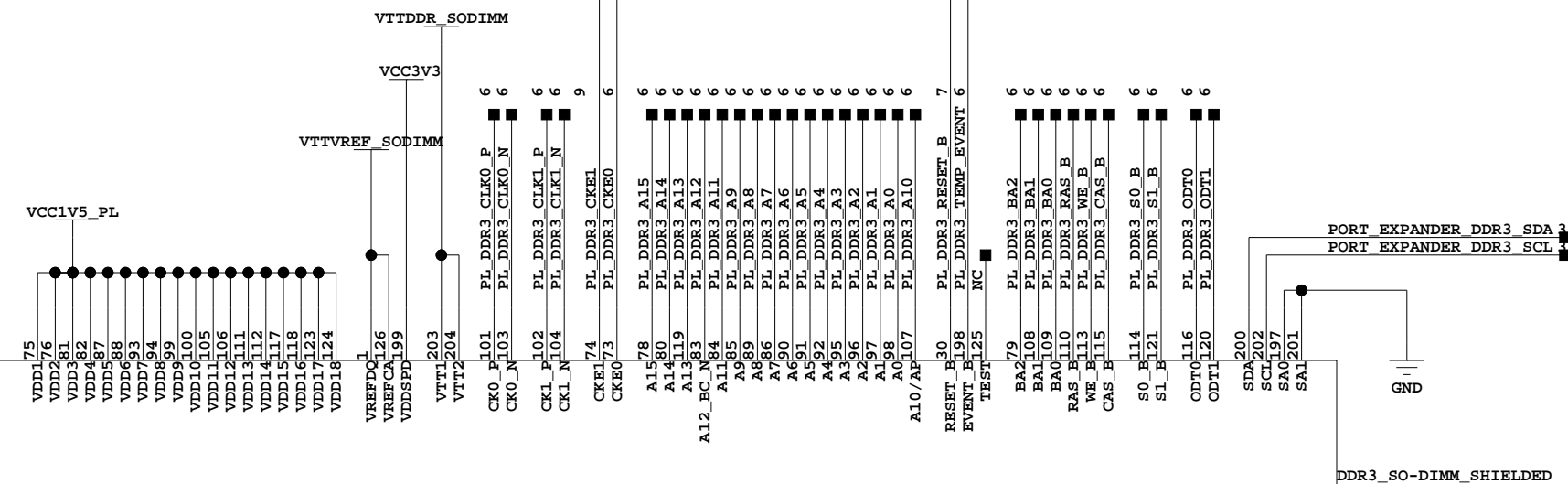
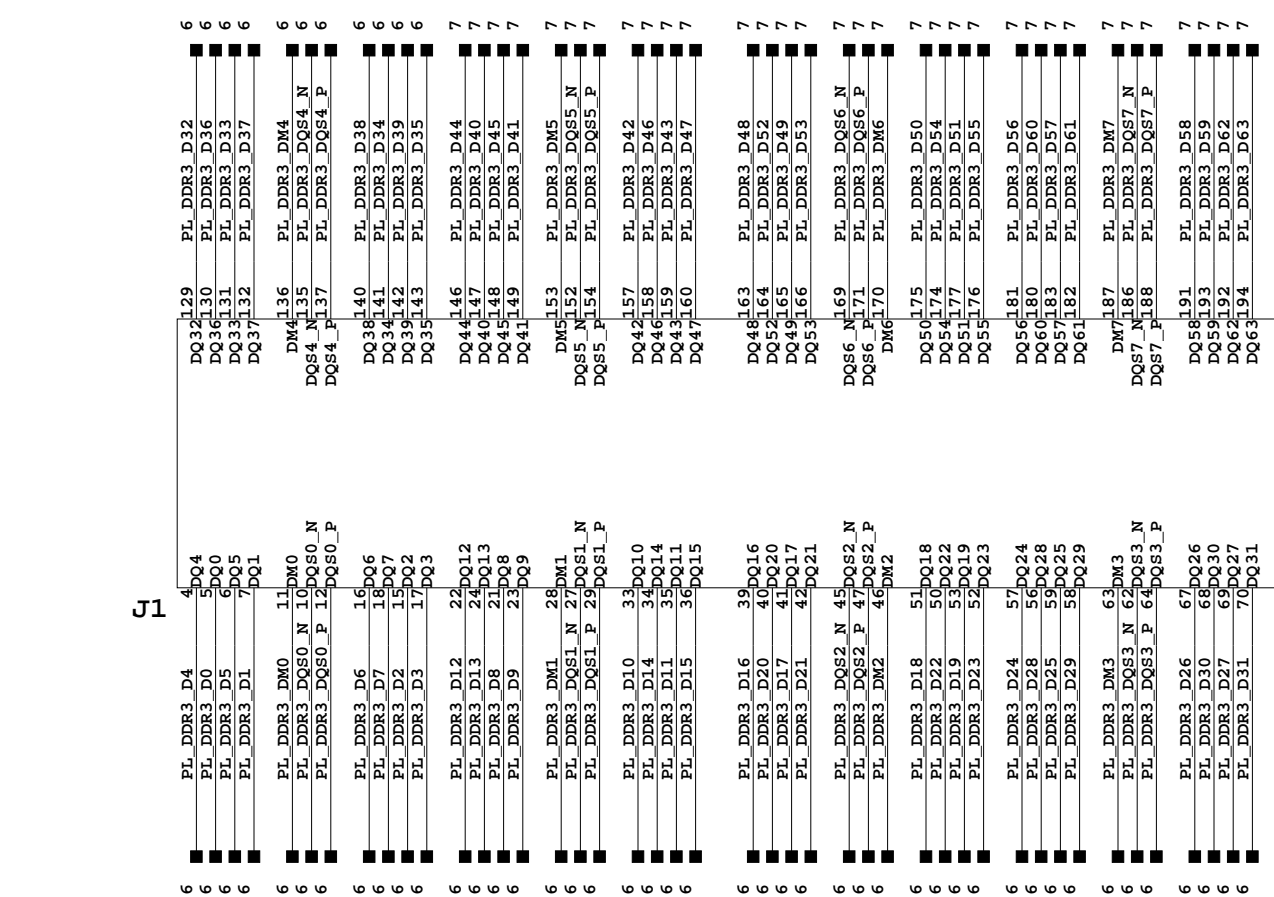
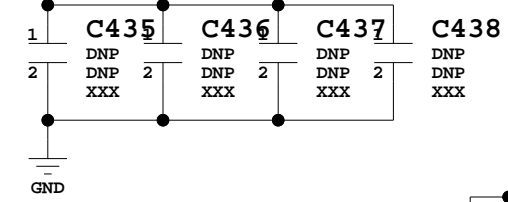
SD Card Connector



Title: SD Card Connector SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 11-13-2012_11:18	Ver: 1.1	
Sheet Size: B	Rev: 02	
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Place Near pin 1 of DIMM

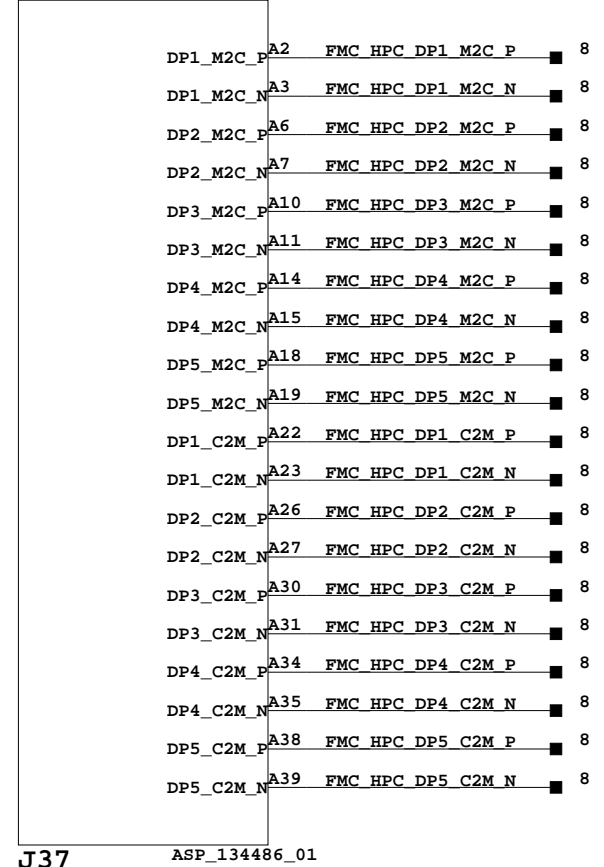


Silkscreen:
"DDR3 SO-DIMM"

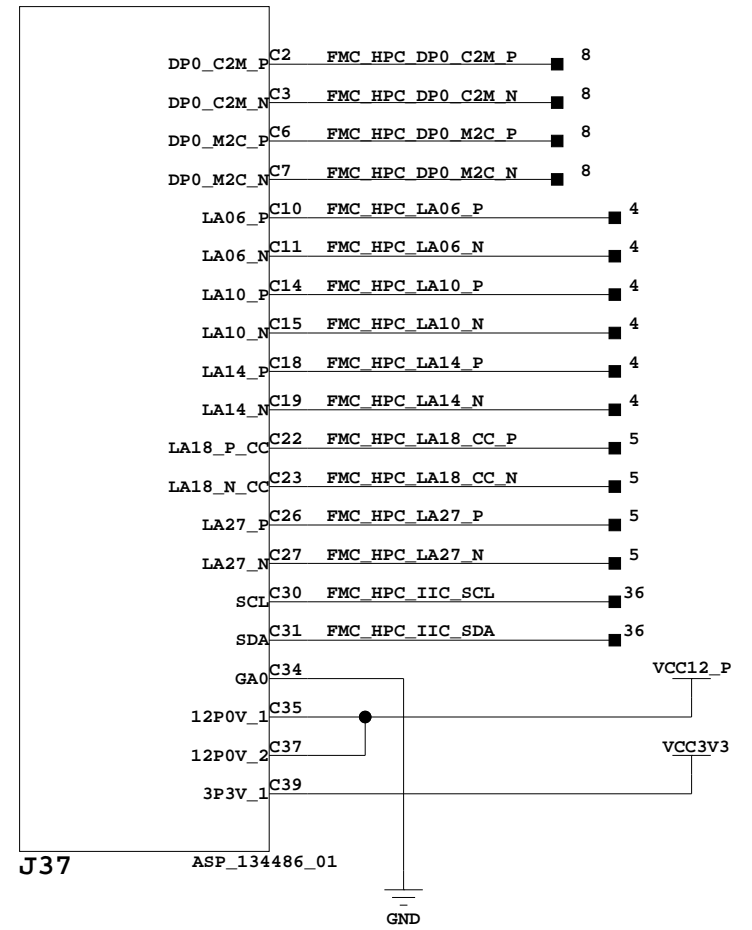
Shielded DDR3 SO-DIMM



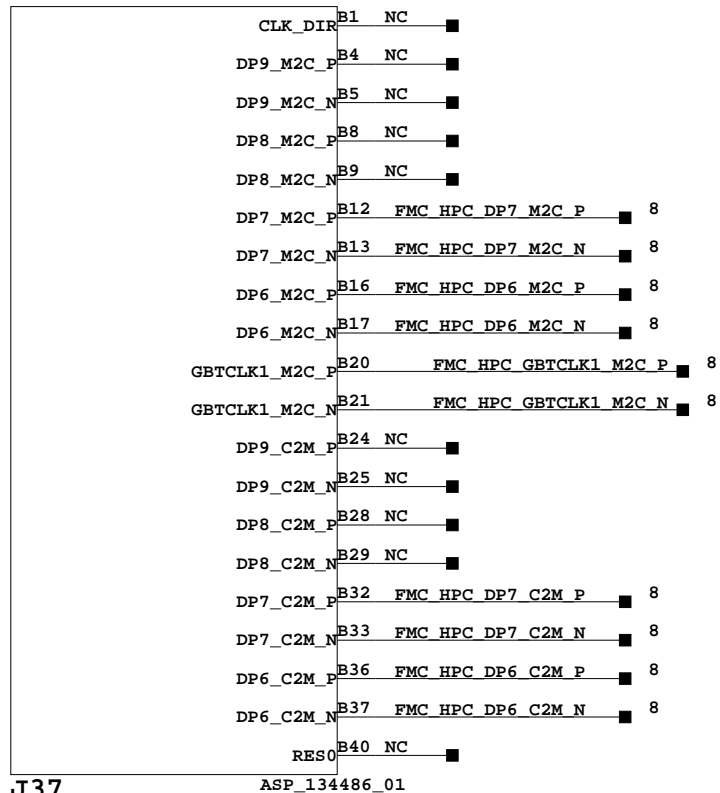
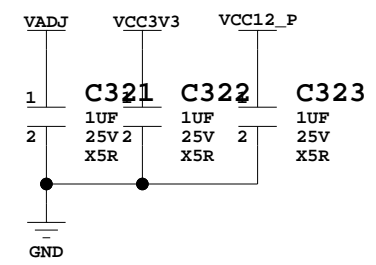
Title: Shielded DDR3 SO-DIMM SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 23 of 58	Drawn By BF	



J37 ASP_134486_01

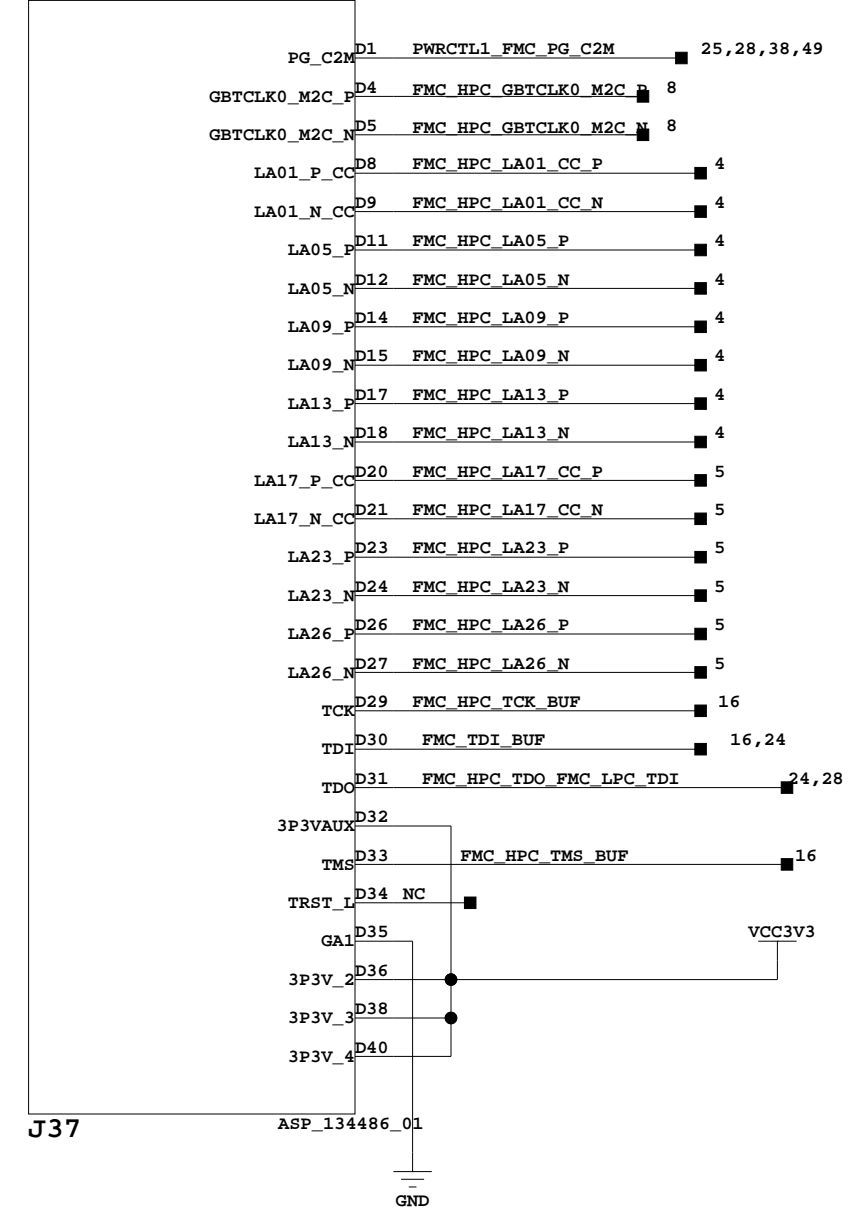
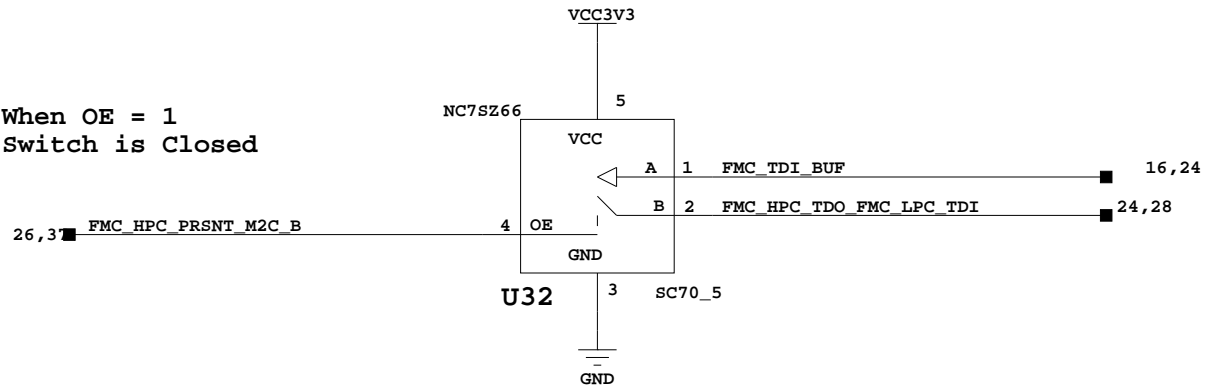


J37 ASP_134486_01



J37 ASP_134486_01

When OE = 1
Switch is Closed

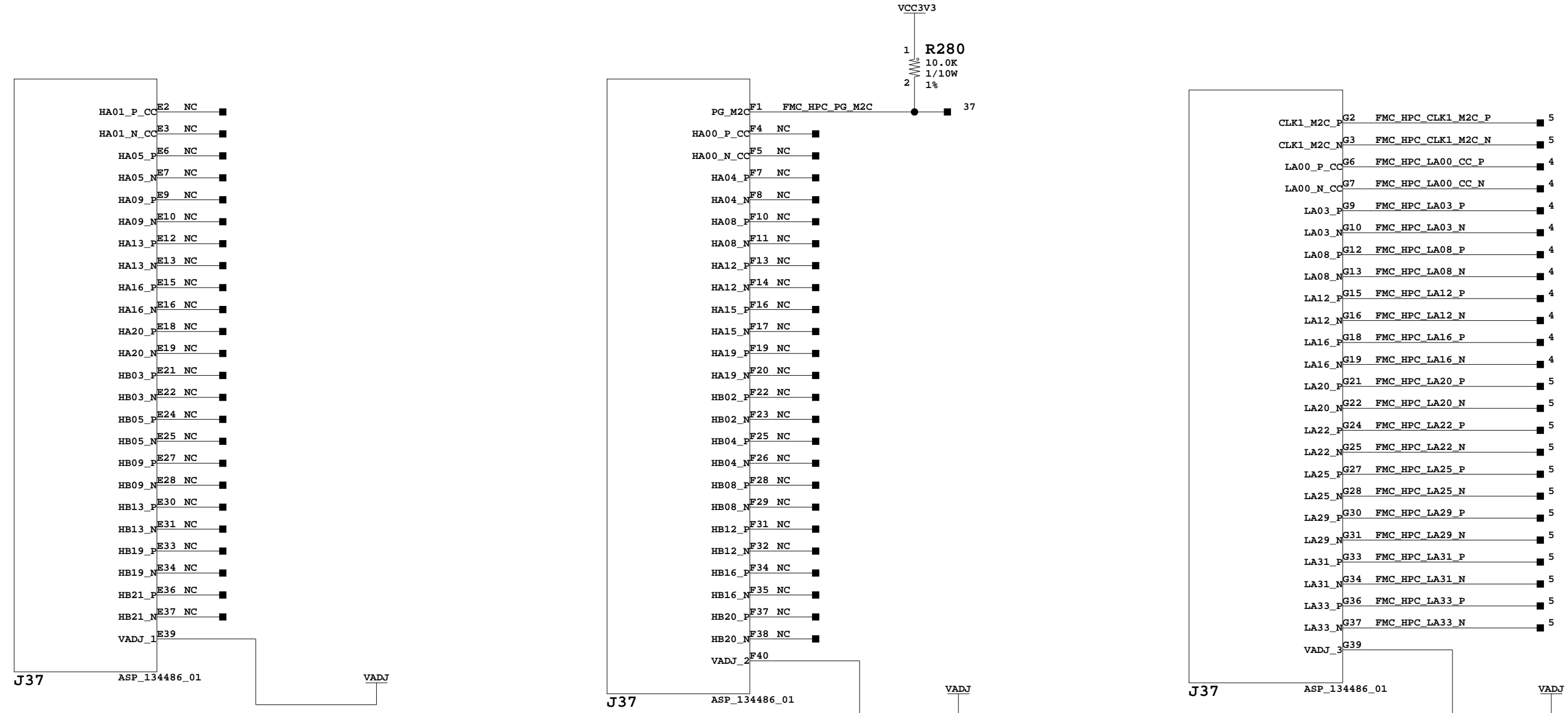


J37 ASP_134486_01

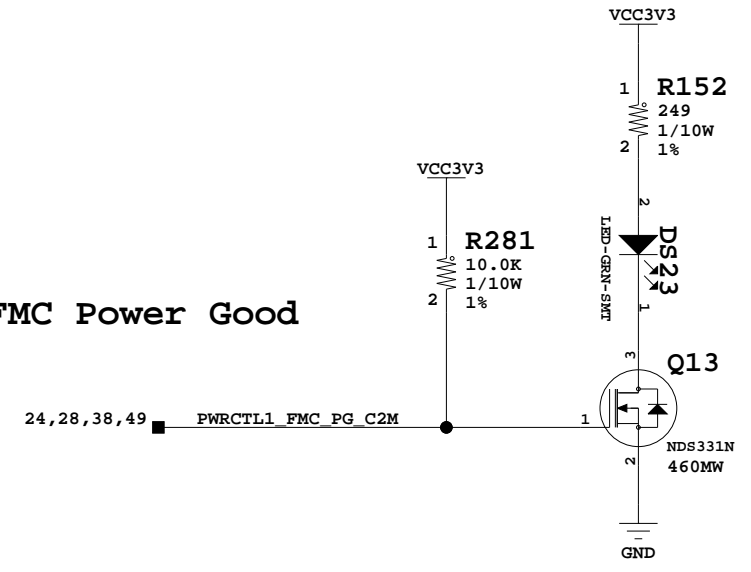
ANSI/VITA 57.1 - Revised 2010 FMC HPC Header, Rows A, B, C, D



Title: FMC HPC Header, Rows A, B, C, D		ASSY P/N: 0431760
SCHEM, ROHS COMPLIANT		PCB P/N: 1280681
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 24 of 58	Drawn By BF	



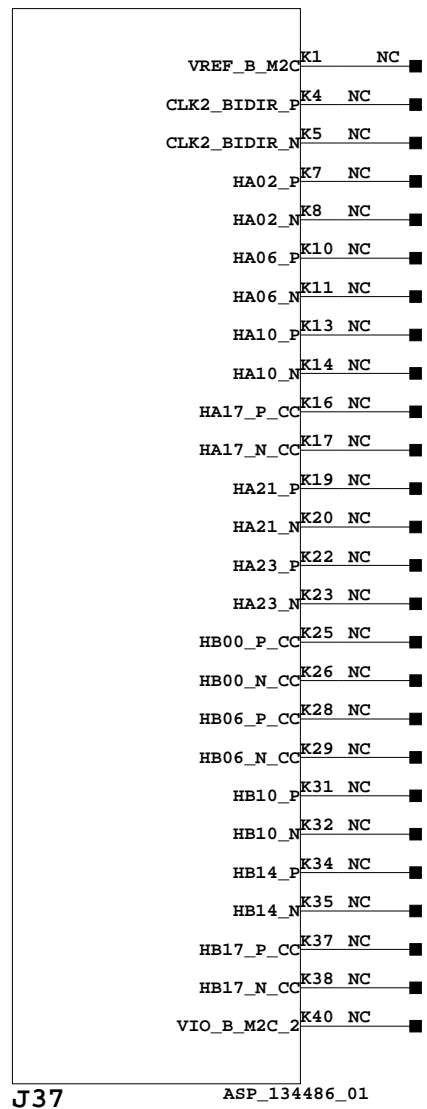
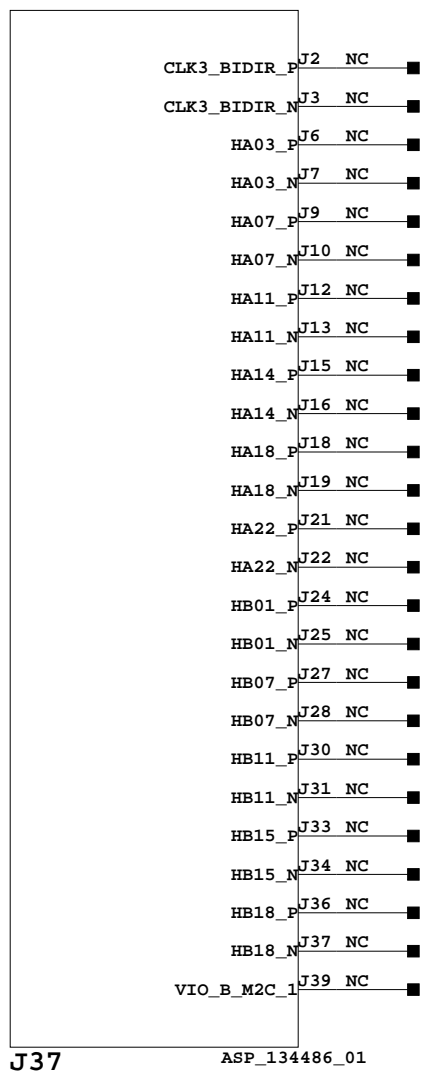
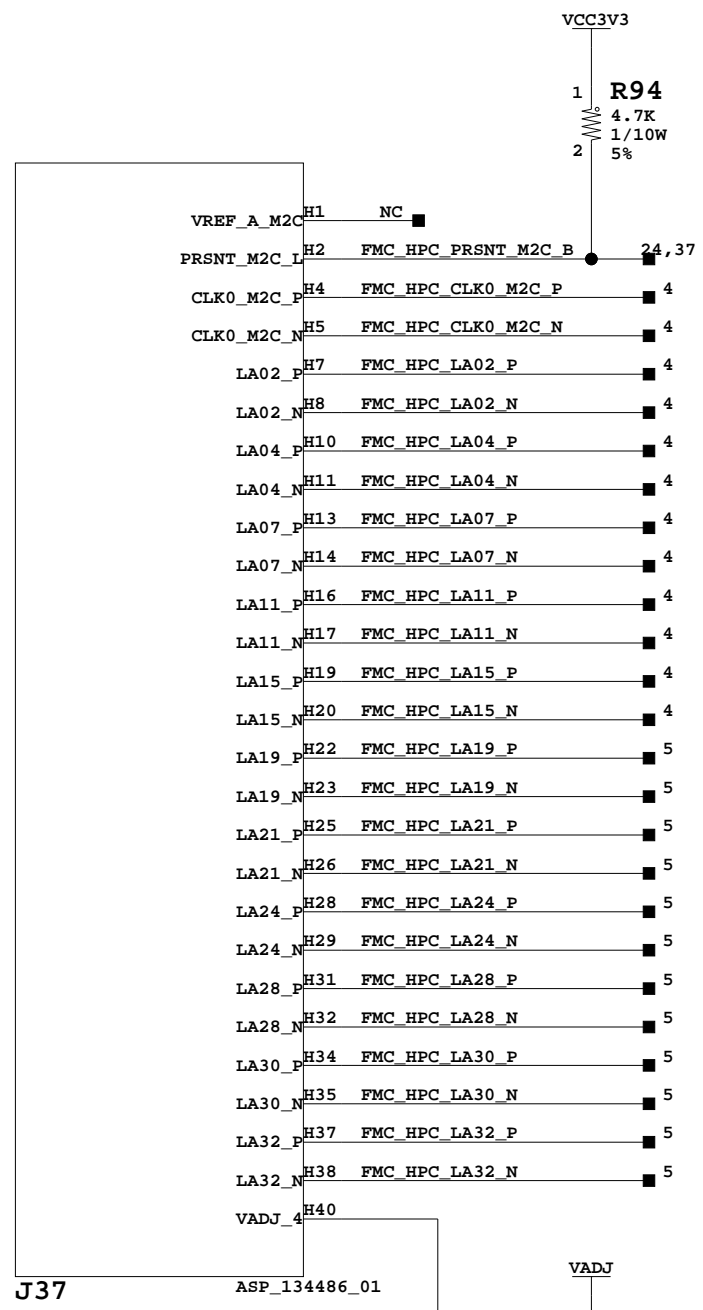
FMC Power Good



ANSI/VITA 57.1 - Revised 2010 FMC HPC Header, Rows E, F, G



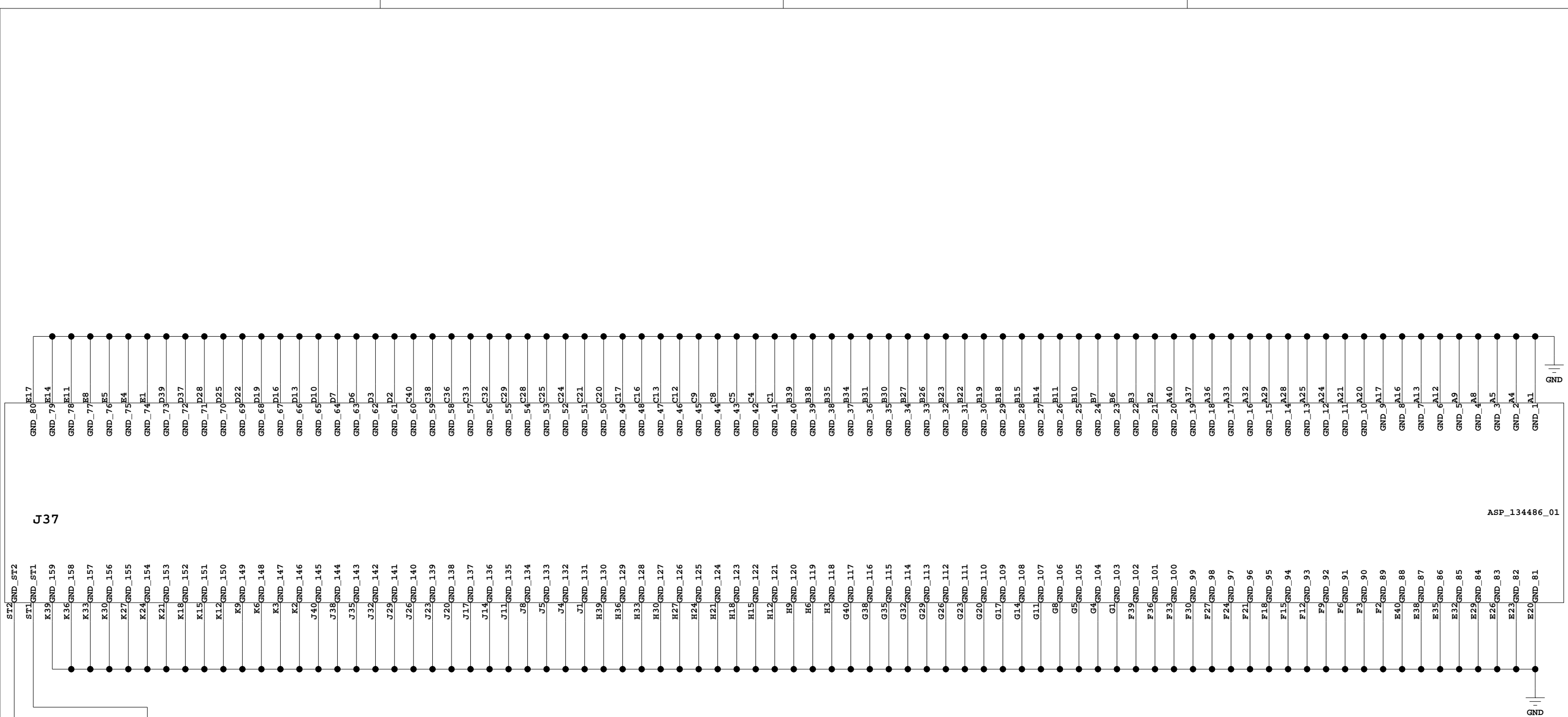
Title: FMC HPC Header, Rows E, F, G SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 25 of 58	Drawn By BF	



ANSI/VITA 57.1 - Revised 2010
FMC HPC Header, Rows H, J, K

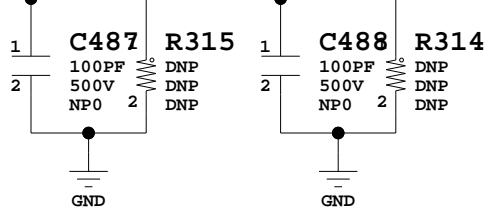


Title: FMC HPC Header, Rows H, J, K SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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J37

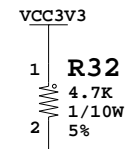
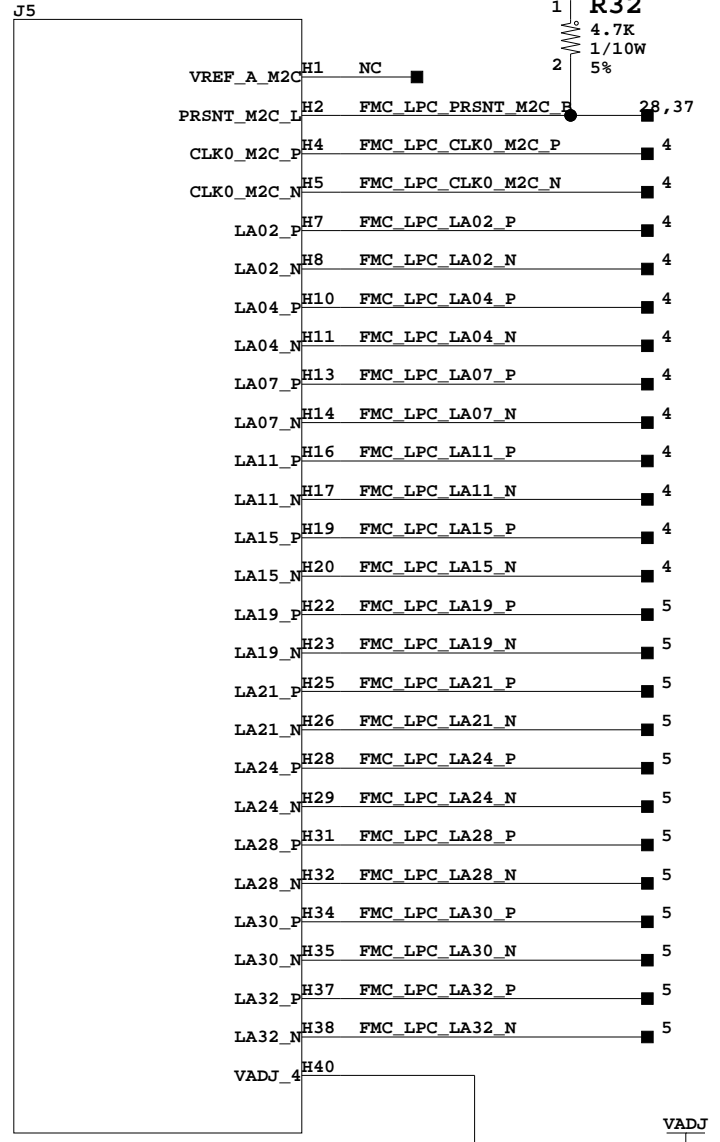
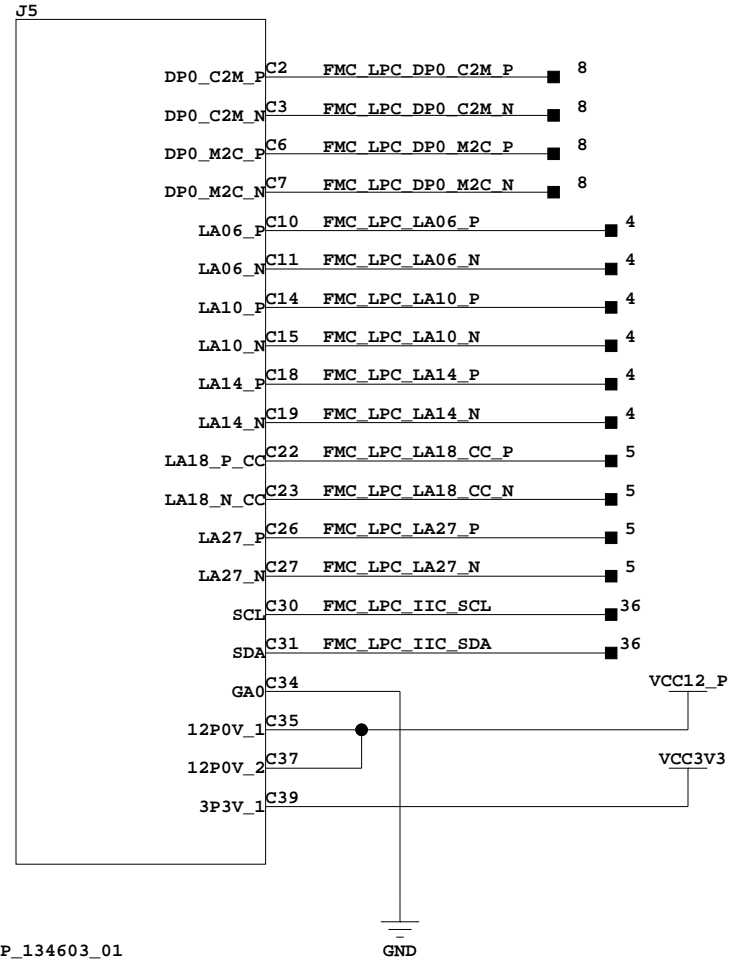
ASP_134486_01



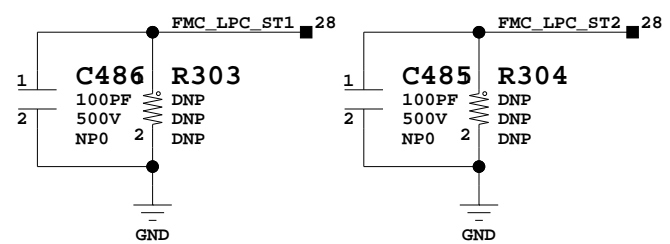
**ANSI/VITA 57.1 - Revised 2010
FMC HPC Header, GND**



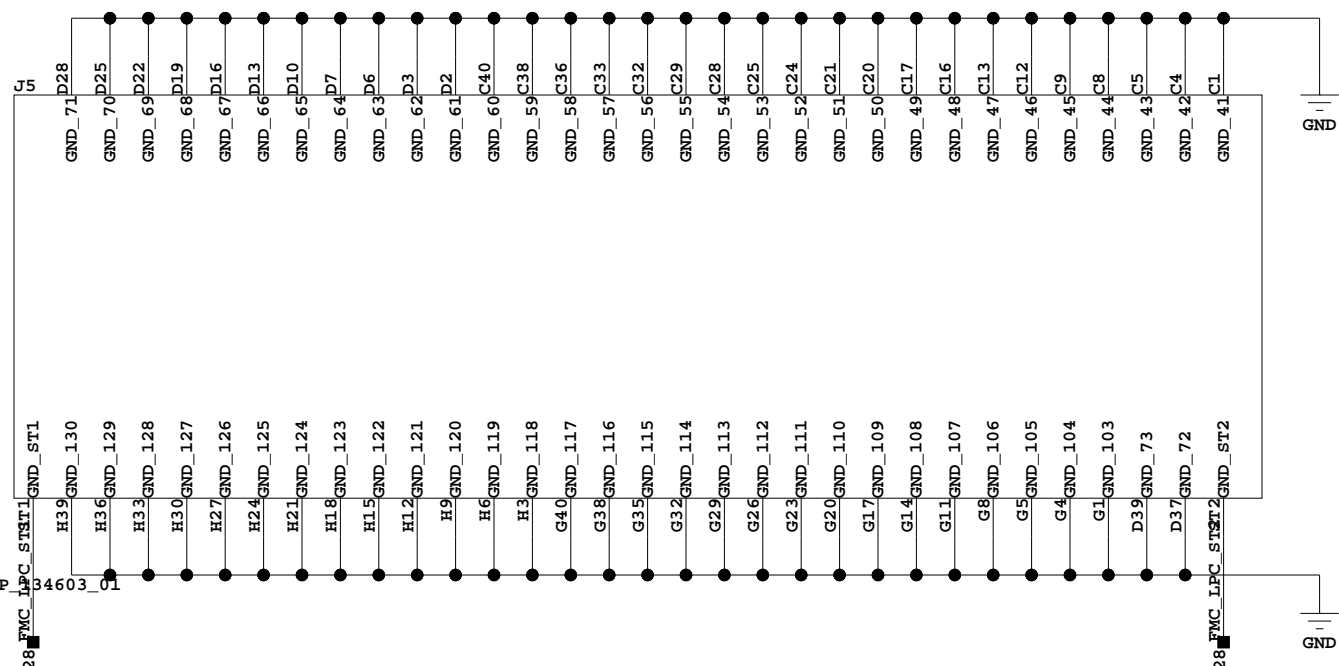
Title: FMC HPC Header, GND SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date:	10-31-2012_22:05	Ver: 1.1
Sheet Size:	B	Rev: 02
Sheet	27 of 58	Drawn By: BF



ASP_134603_01

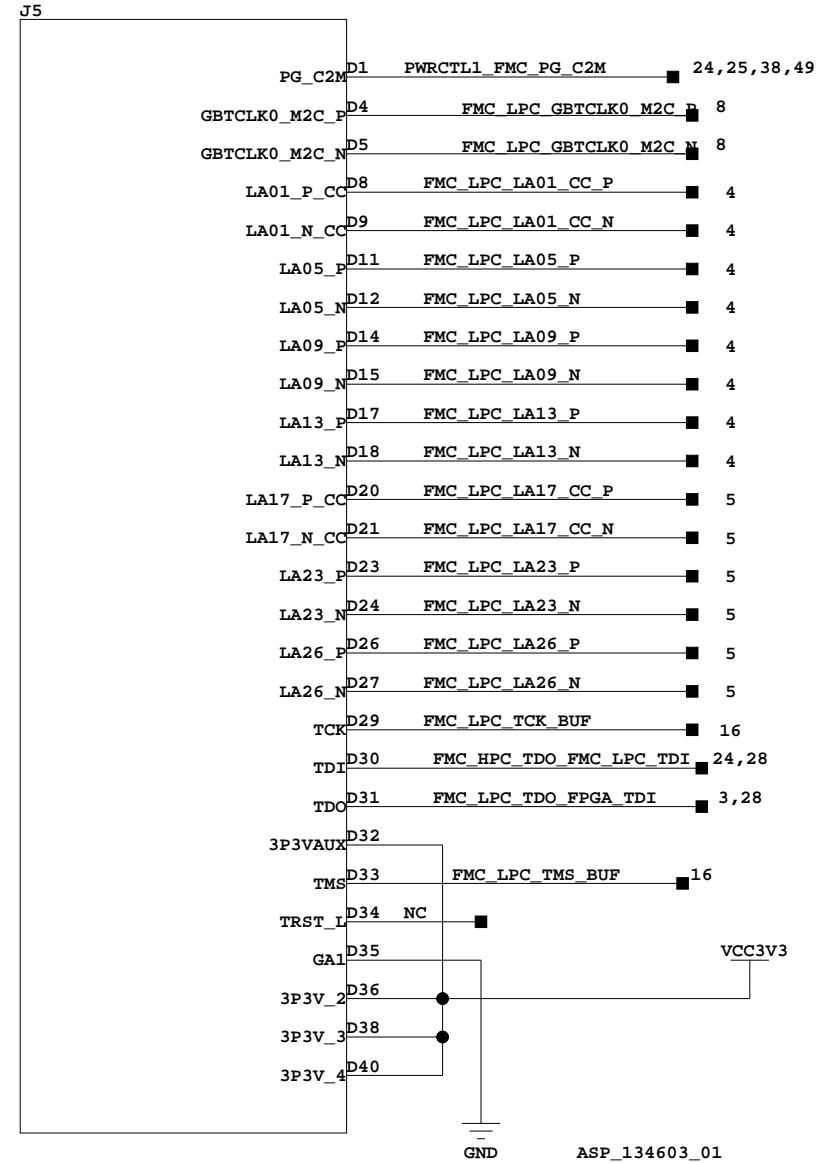


ASP_134603_01



ASP_134603_01

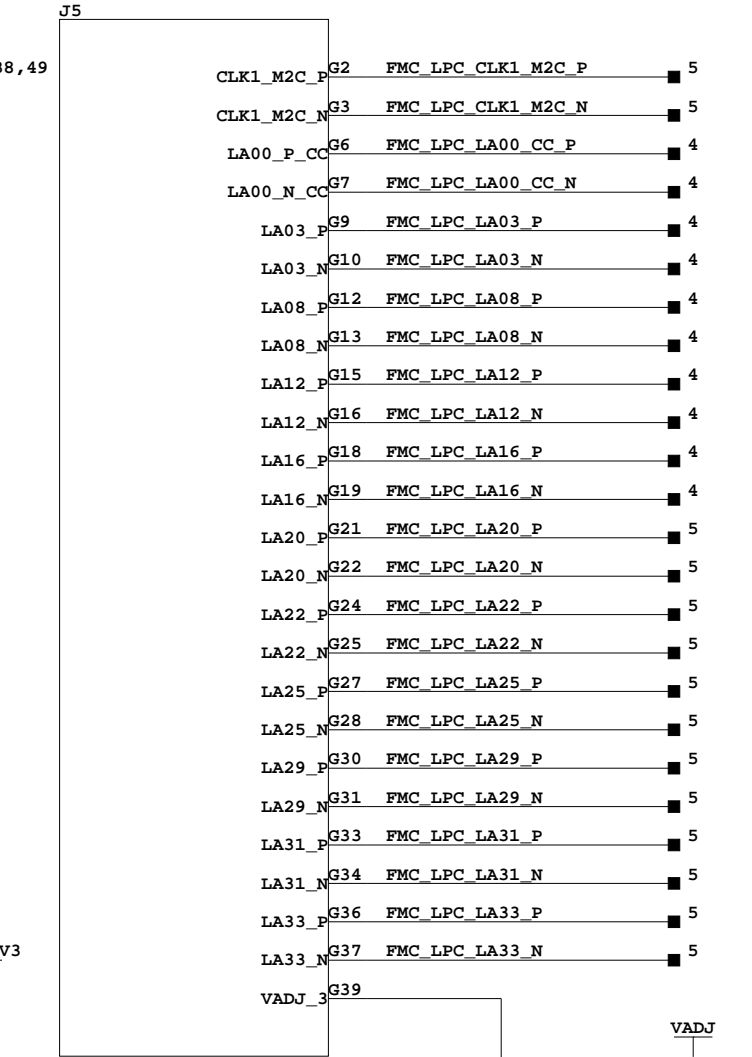
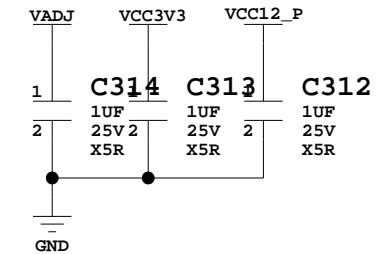
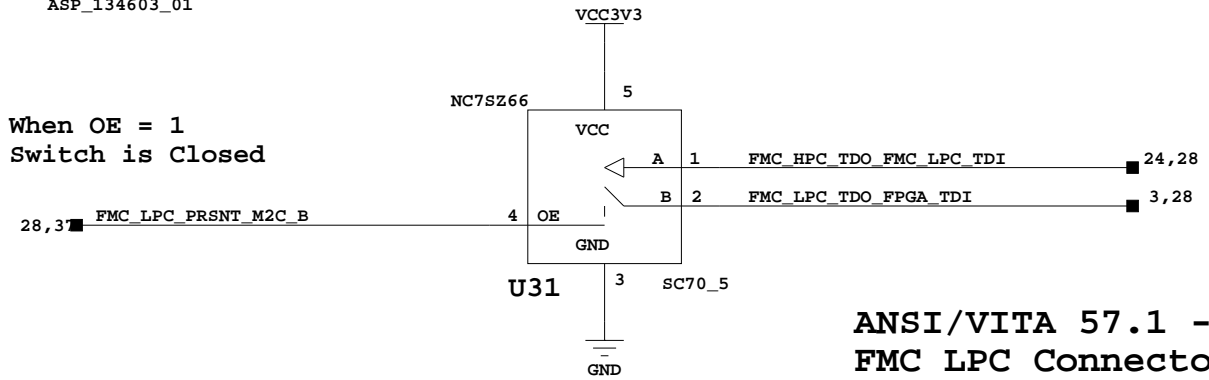
ASP_134603_01



ASP_134603_01

ASP_134603_01

When OE = 1
Switch is Closed



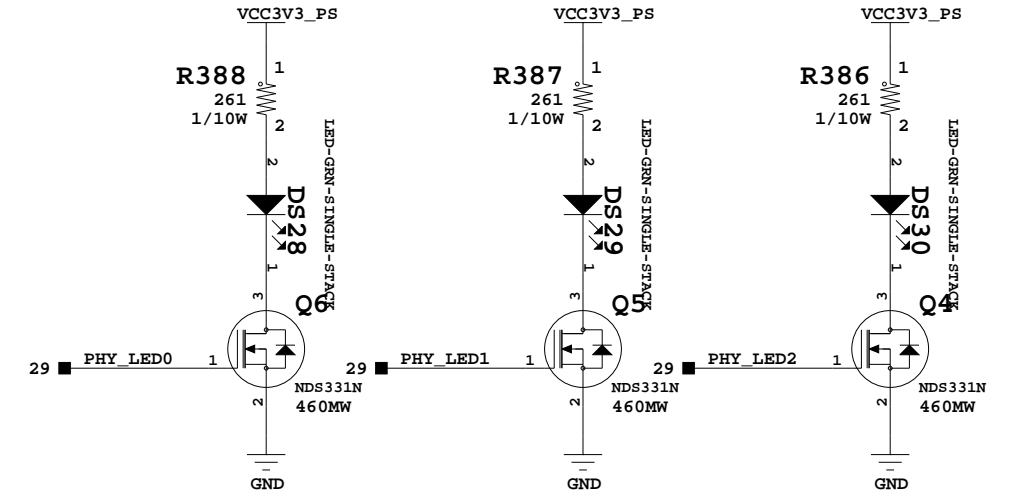
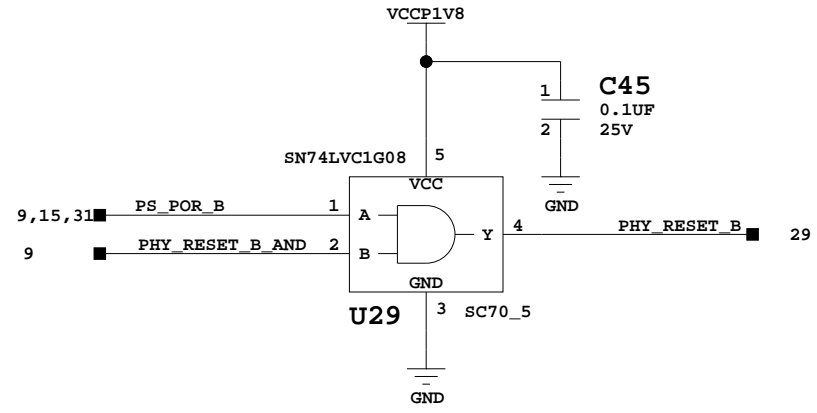
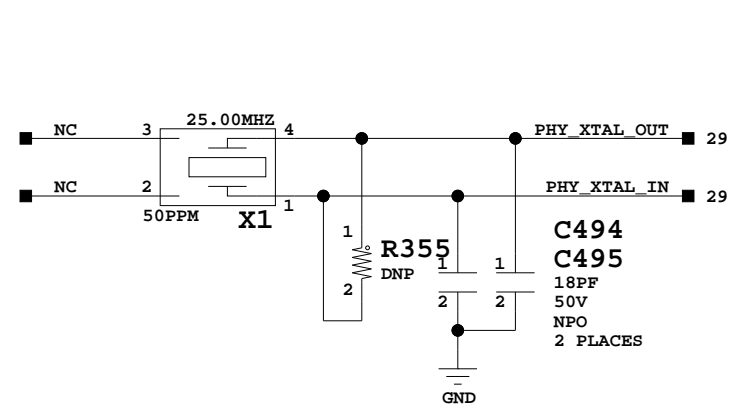
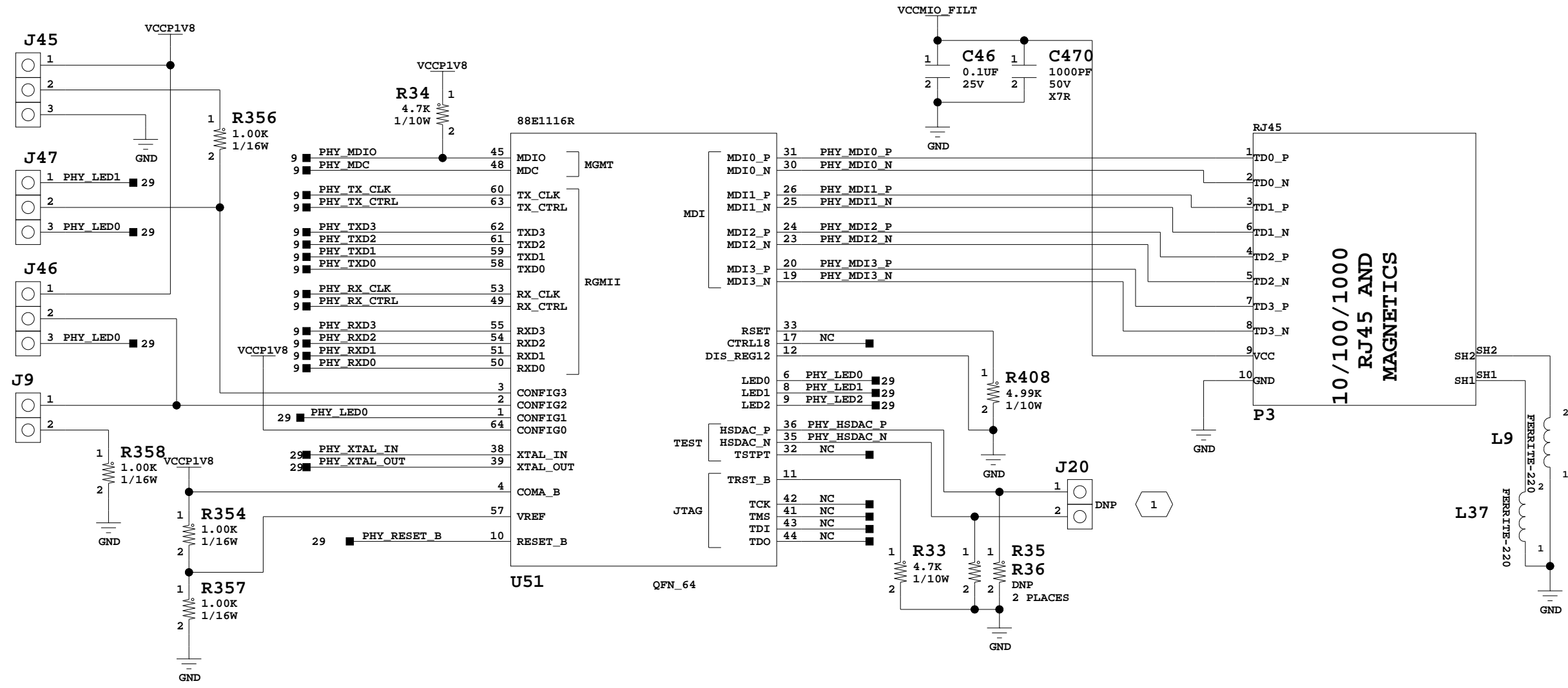
ANSI/VITA 57.1 - Revised 2010 FMC LPC Connector



Title: ANSI/VITA 57.1 - Revised 2010 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 28 of 58	Drawn By BF	

CONFIGURATION MAPPING

PIN	SETTING	CONFIGURATION
CONFIG0	VCCO_MIO1	PHYAD[1]=1 PHYAD[0]=1
CONFIG1	EPHY_LED0	PHYAD[3]=0 PHYAD[2]=1
CONFIG2	GND	ENA_XC=0 PHYAD[4]=0
	EPHY_LED0	ENA_XC=0 PHYAD[4]=1
	VCCO_MIO1	ENA_XC=1 PHYAD[4]=1
CONFIG3	GND	RGMII_TX=0 RGMII_RX=0
	EPHY_LED0	RGMII_TX=0 RGMII_RX=1
	EPHY_LED1	RGMII_TX=1 RGMII_RX=0
	VCCO_MIO1	RGMII_TX=1 RGMII_RX=1



XILINX

Title: GEM / MDIO SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1

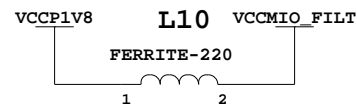
Sheet Size: B Rev: 02

Sheet **29** of **58** Drawn By BF

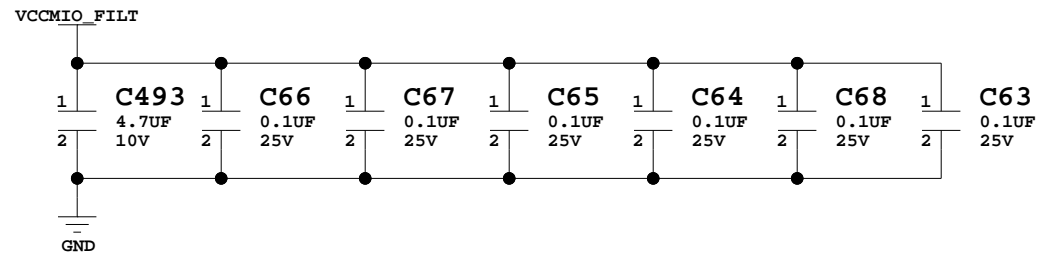
2 SEE CONFIGURATION MAPPING TABLE FOR JUMPER SETTINGS

1 TEST PORT: IF USING THE TEST PORT INSTALL 49.9 OHM PULLDOWN RESISTORS ON HSDAC_P AND HSDAC_N.

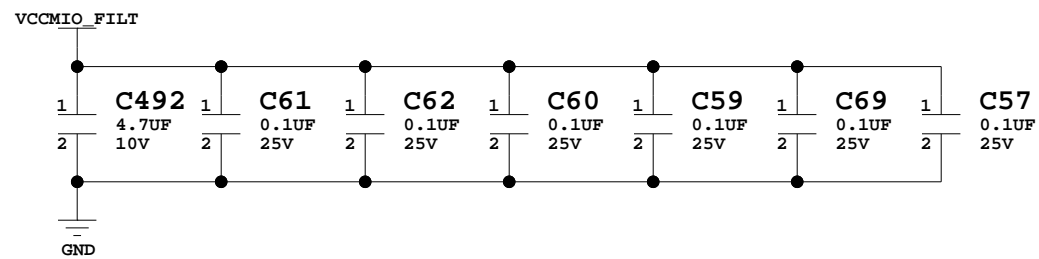
GEM / MDIO - POWER & DECOUPLING



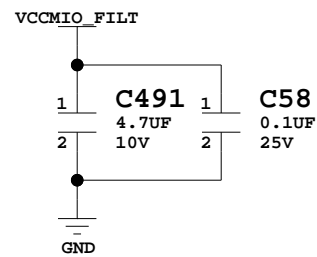
AVDDX, AVDDR, AVDDC



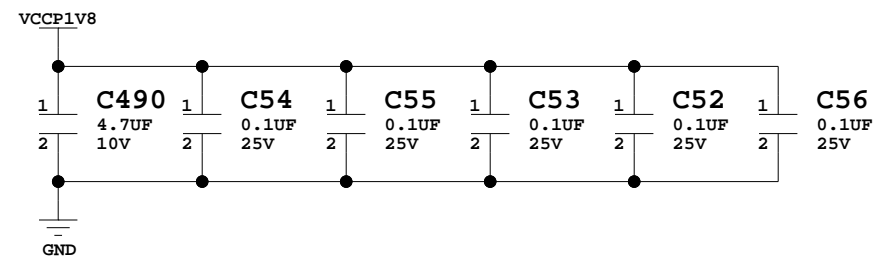
AVDD



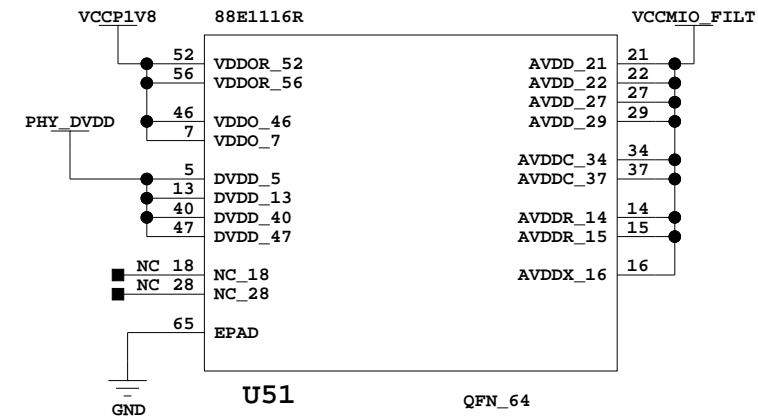
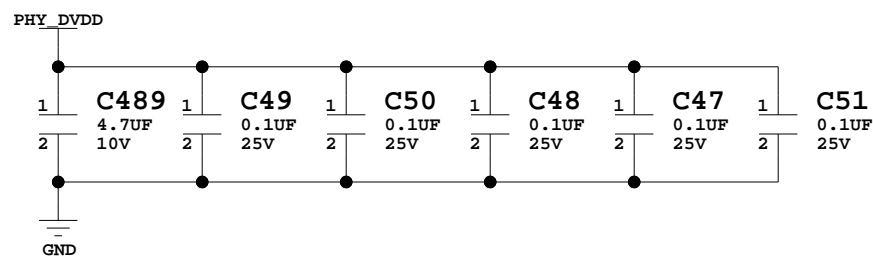
MAGNETICS / RJ45



VDDO, VDDOR



DVDD



GEM / MDIO



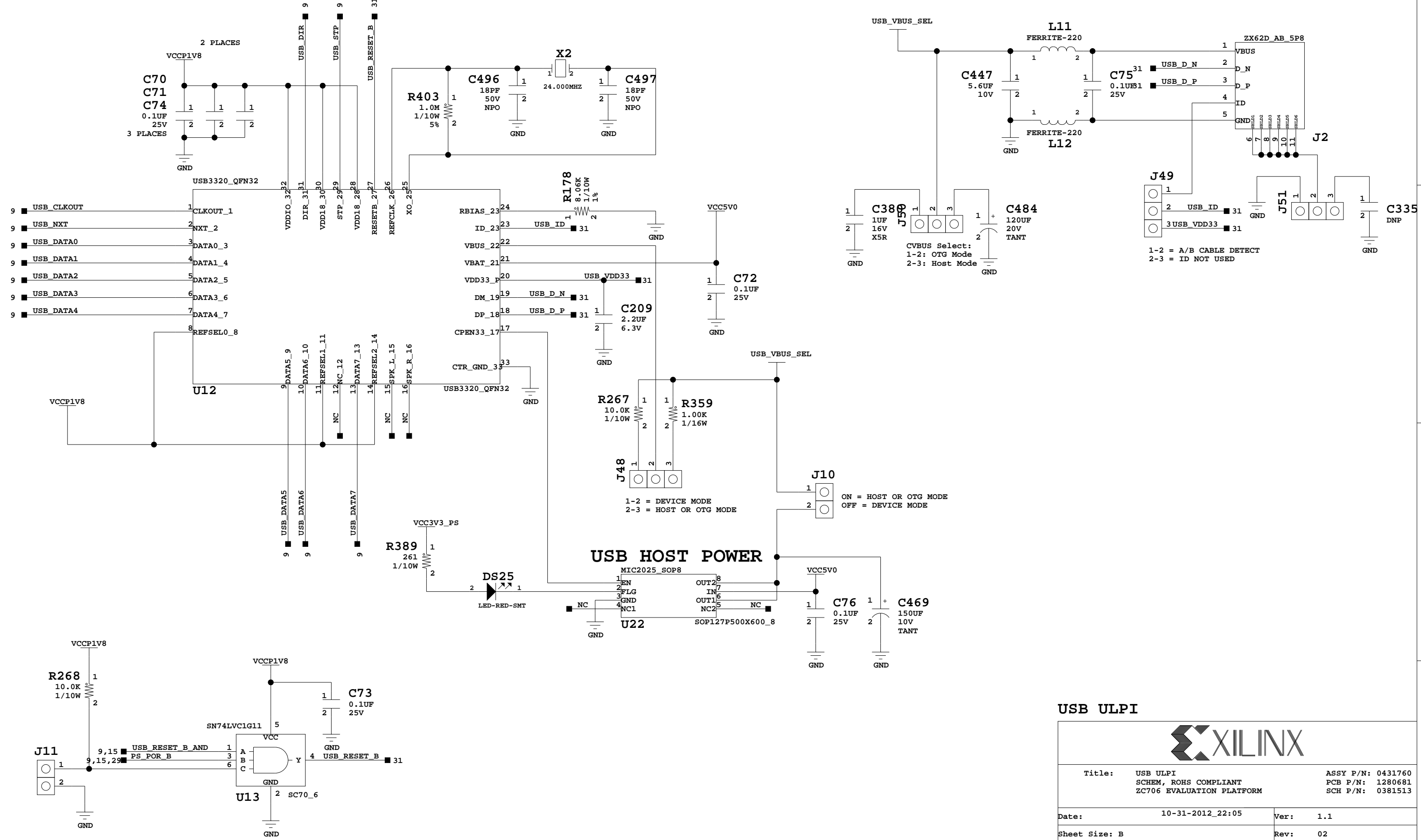
Title: GEM / MDIO SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM
 ASSY P/N: 0431760
 PCB P/N: 1280681
 SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1

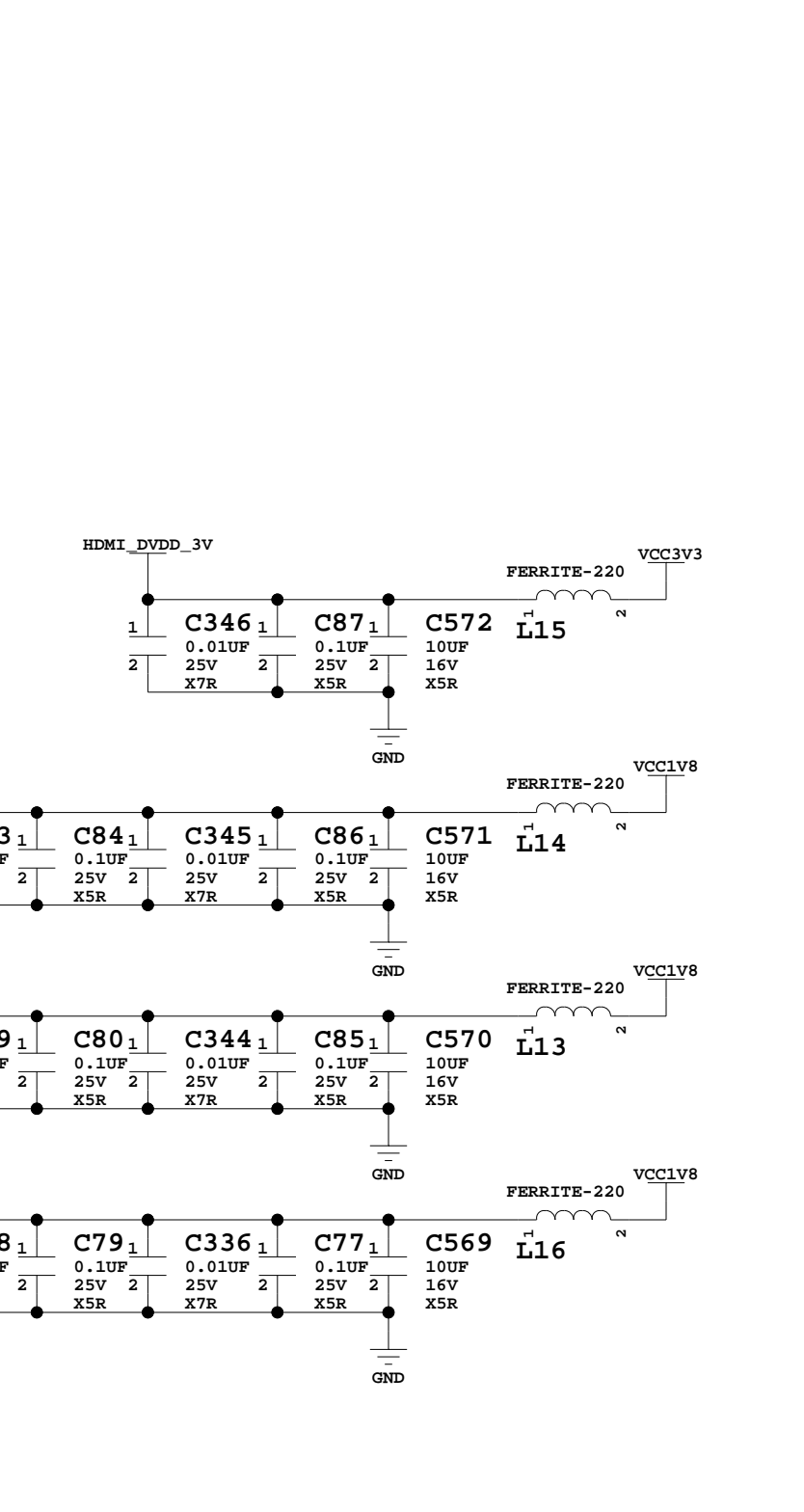
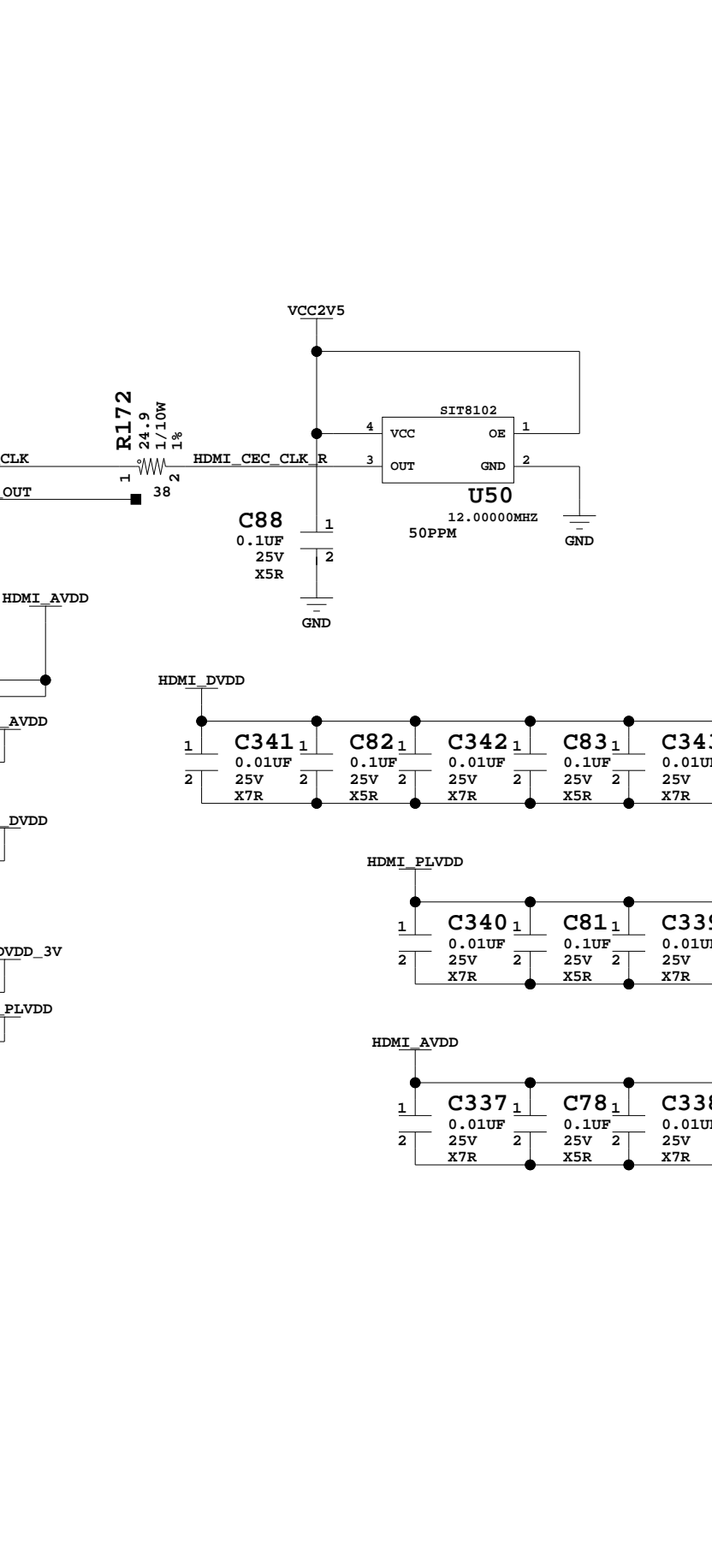
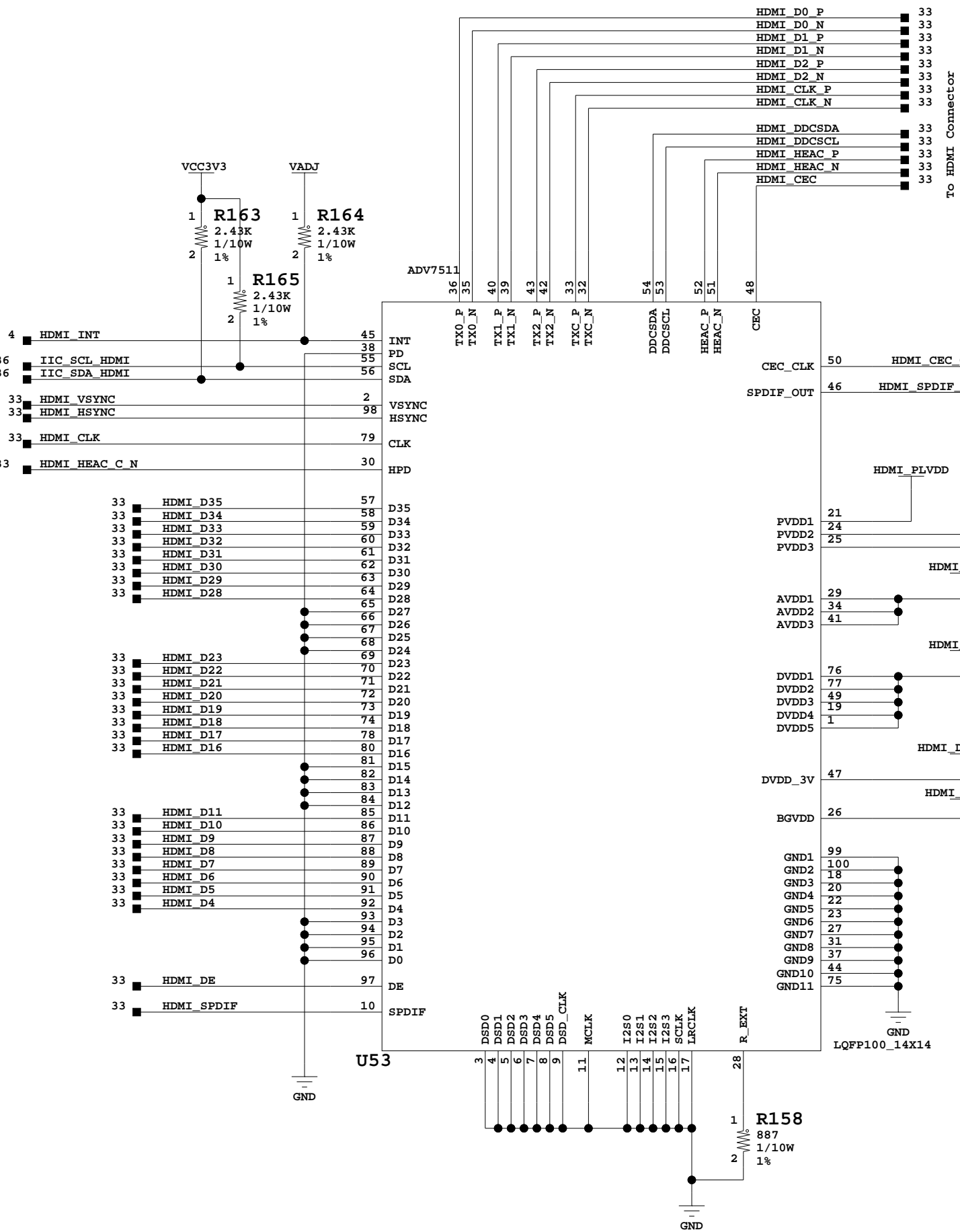
Sheet Size: B Rev: 02

Sheet 30 of 58 Drawn By BF


USB 2.0 ULPI TRANSCEIVER AND CONNECTOR



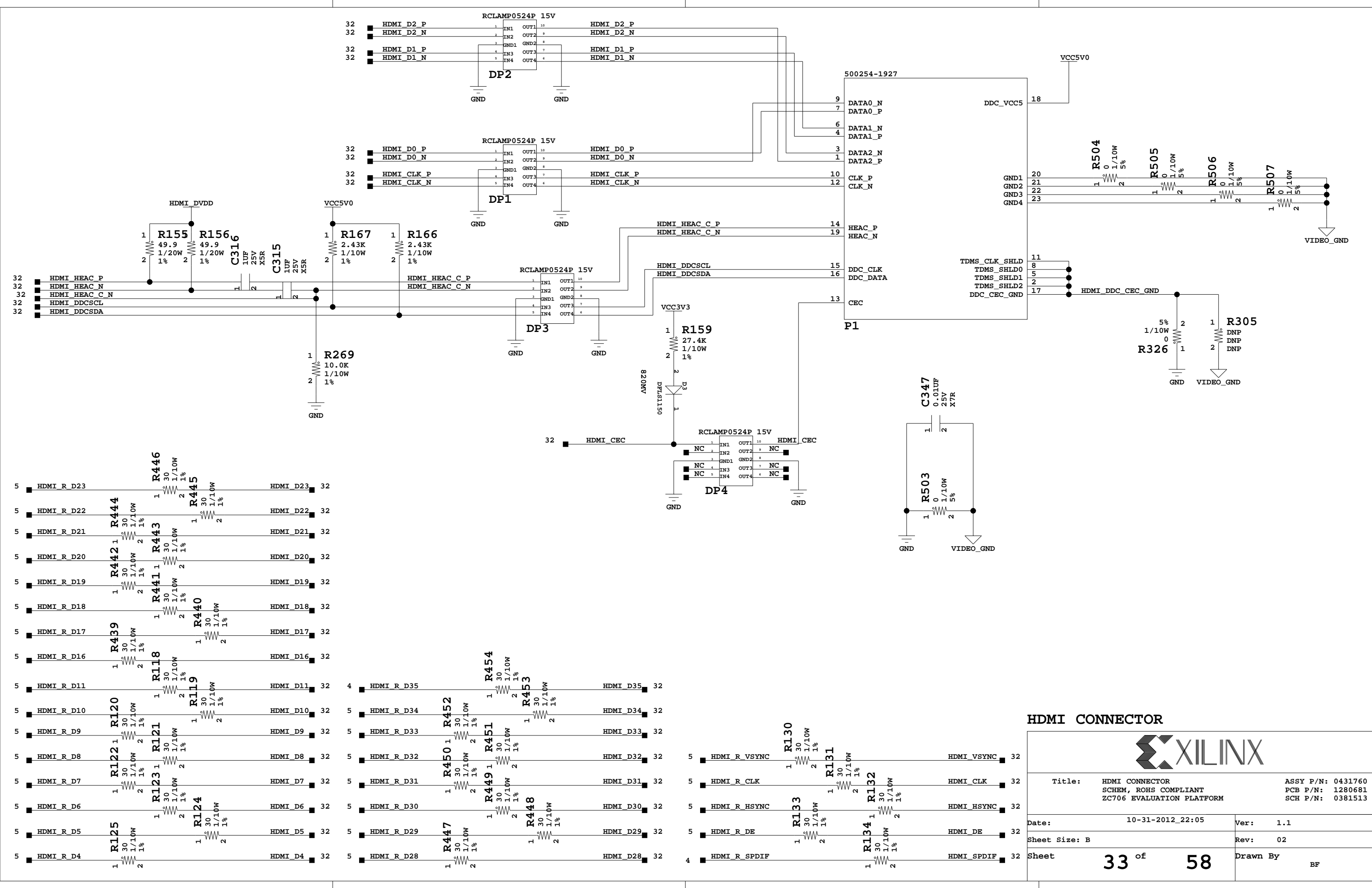
USB ULPI		
Title:	USB ULPI SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date:	10-31-2012_22:05	Ver: 1.1
Sheet Size:	B	Rev: 02
Sheet	31 of 58	Drawn By BF



HDMI CODEC



Title: HDMI CODEC SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 32 of 58	Drawn By BF	

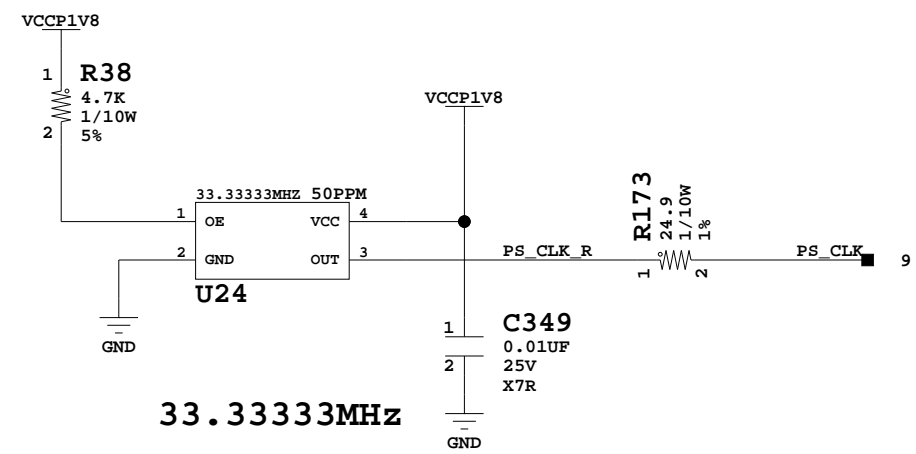
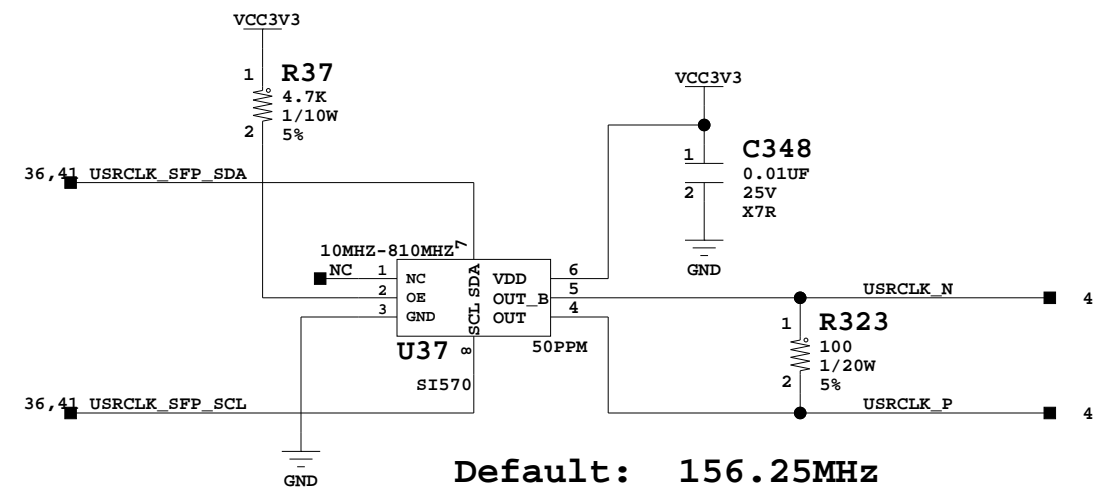
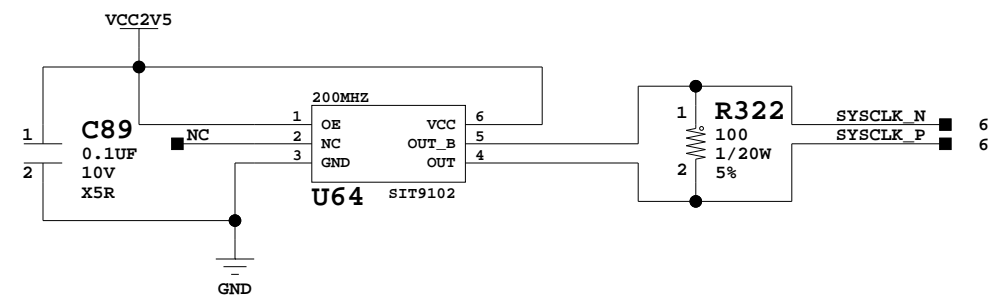


HDMI CONNECTOR



Title: HDMI CONNECTOR SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 33 of 58	Drawn By	BF

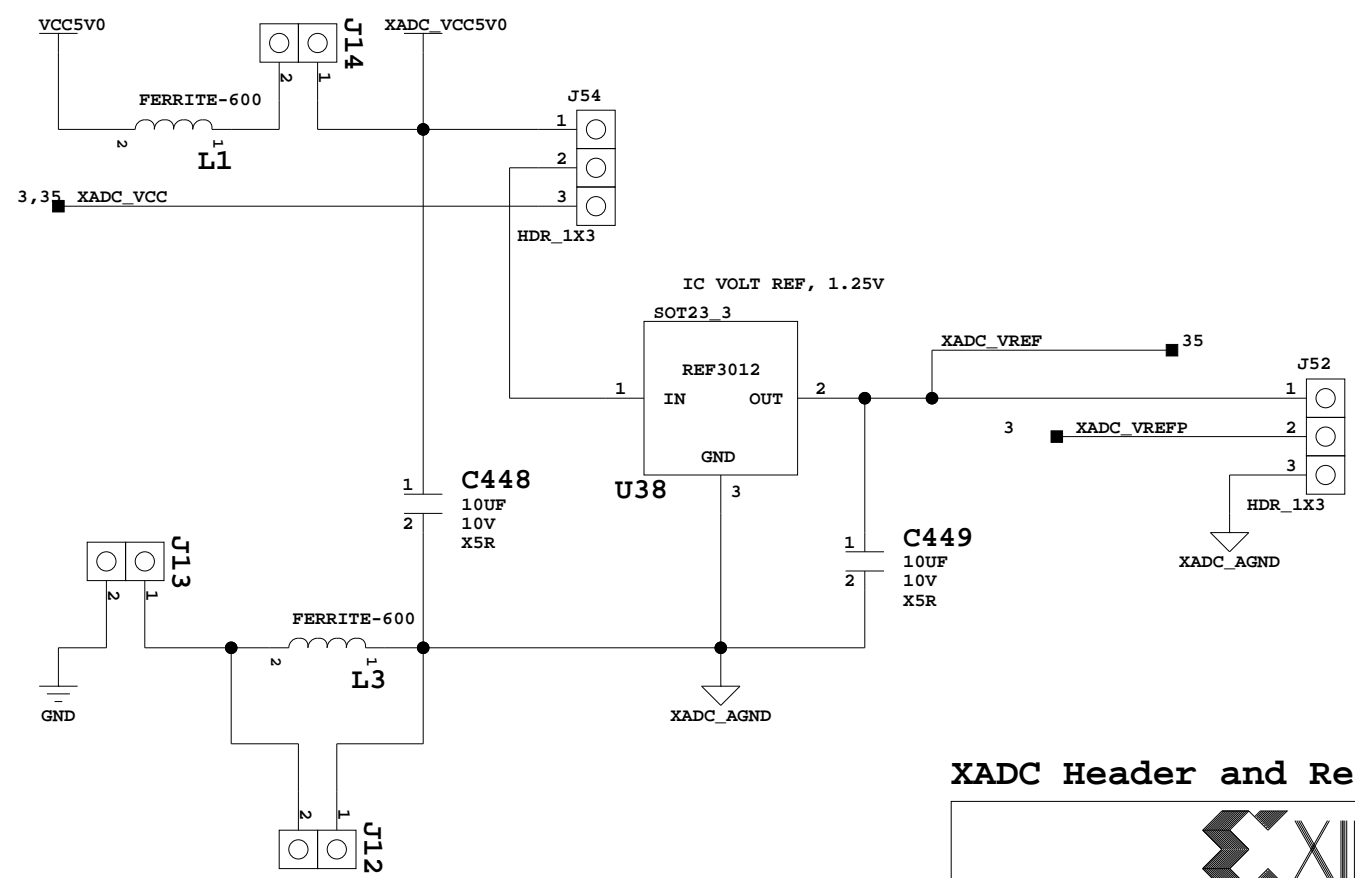
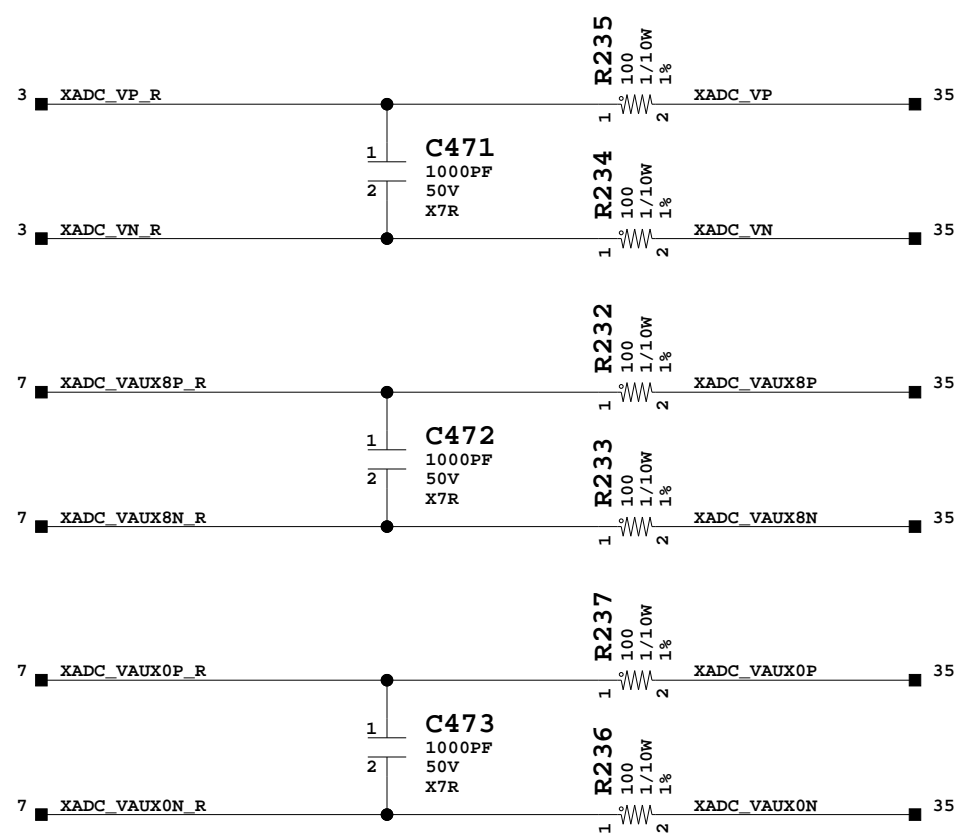
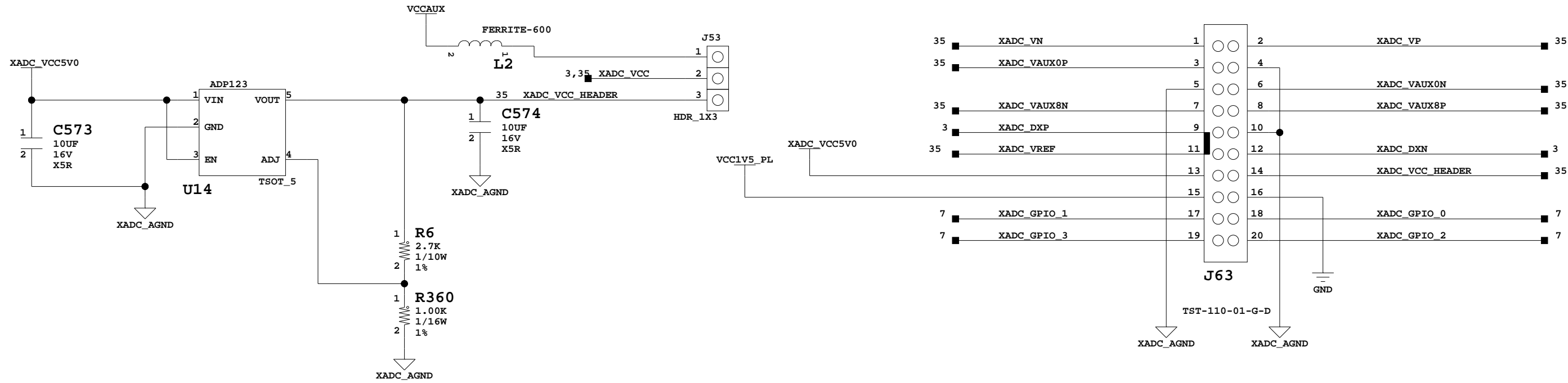
SIT9102AI-243N25E200.0000



Clocks



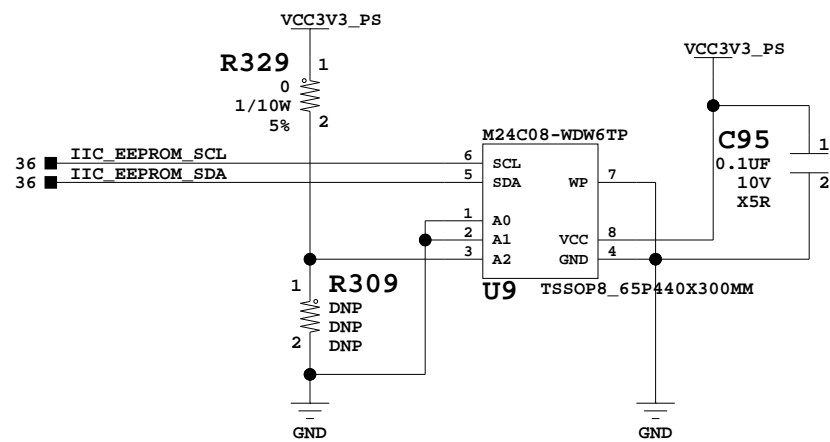
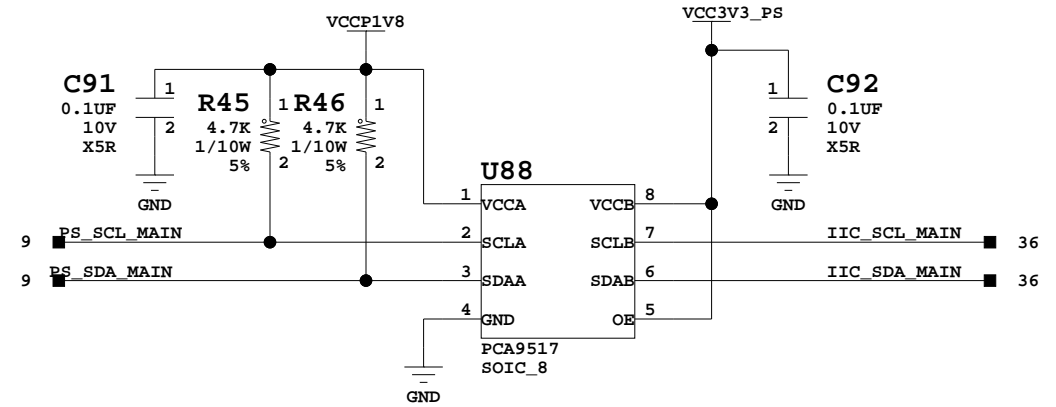
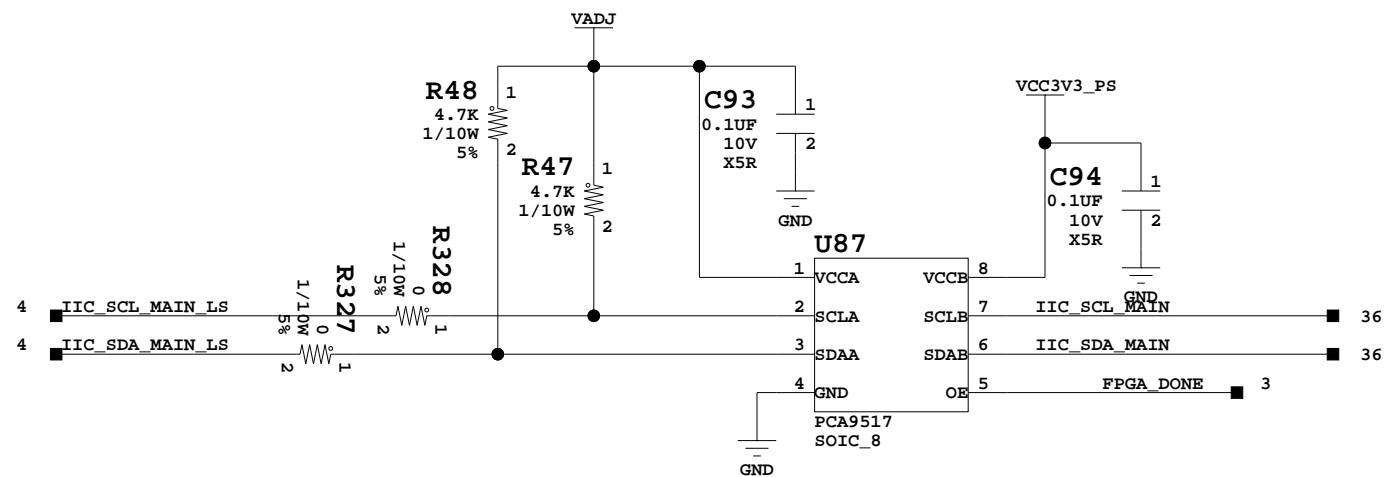
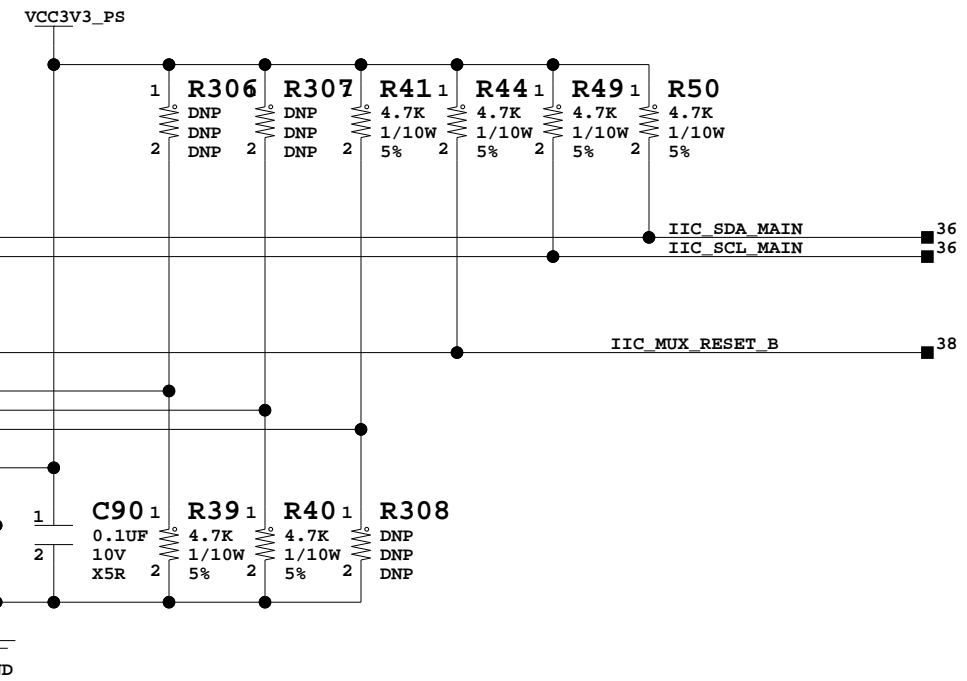
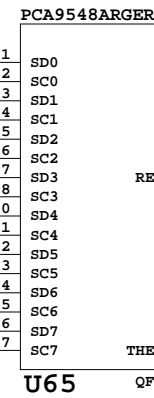
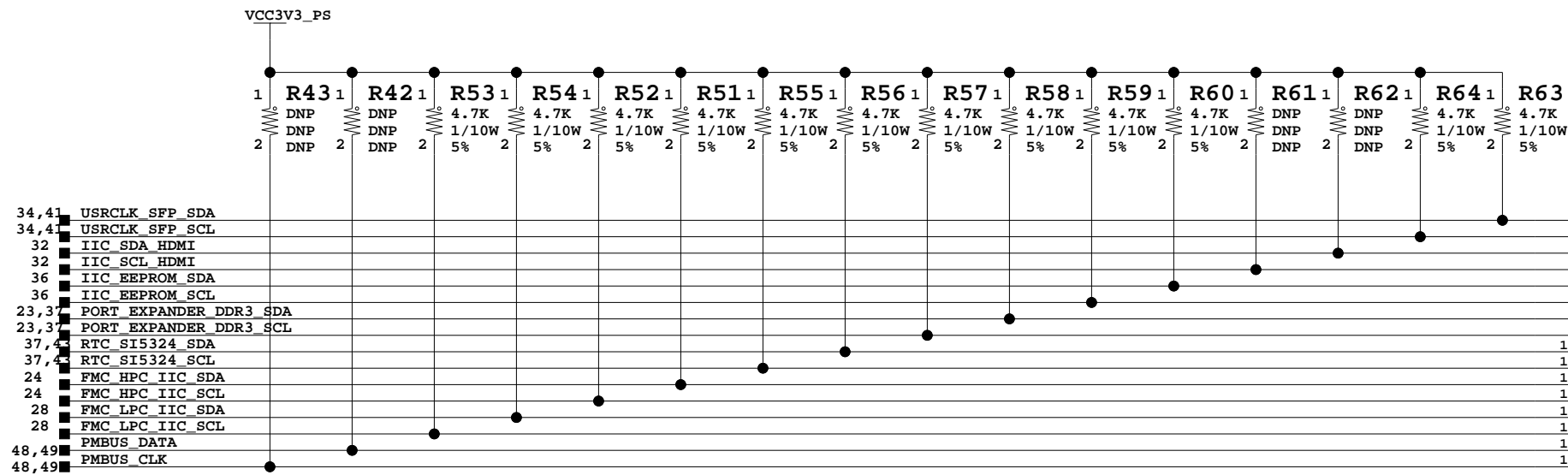
Title: Clocks SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 34 of 58	Drawn By BF	



XADC Header and Reference



Title: XADC Header and Reference SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 35 of 58	Drawn By BF	



IIC MUX, EEPROM



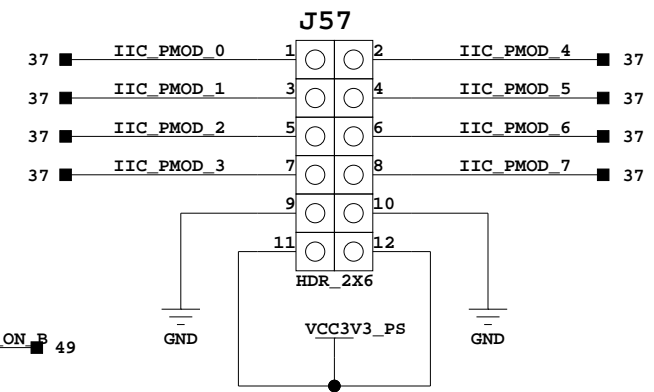
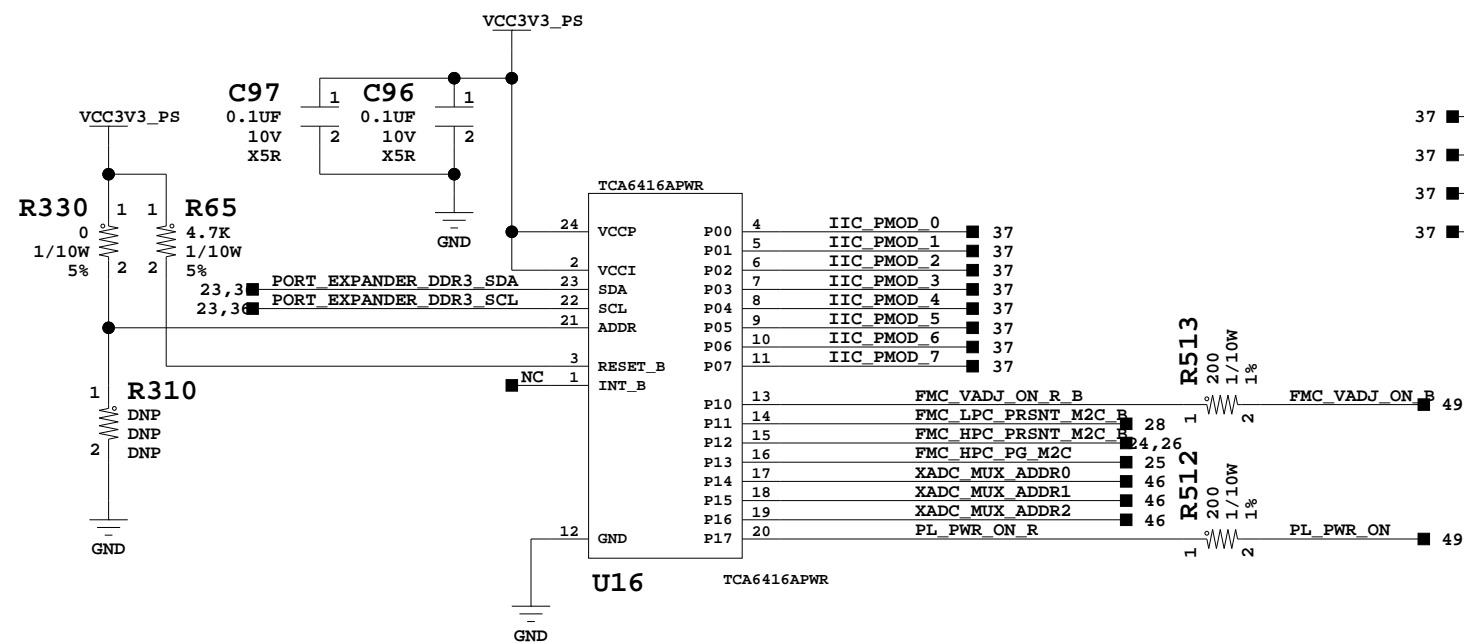
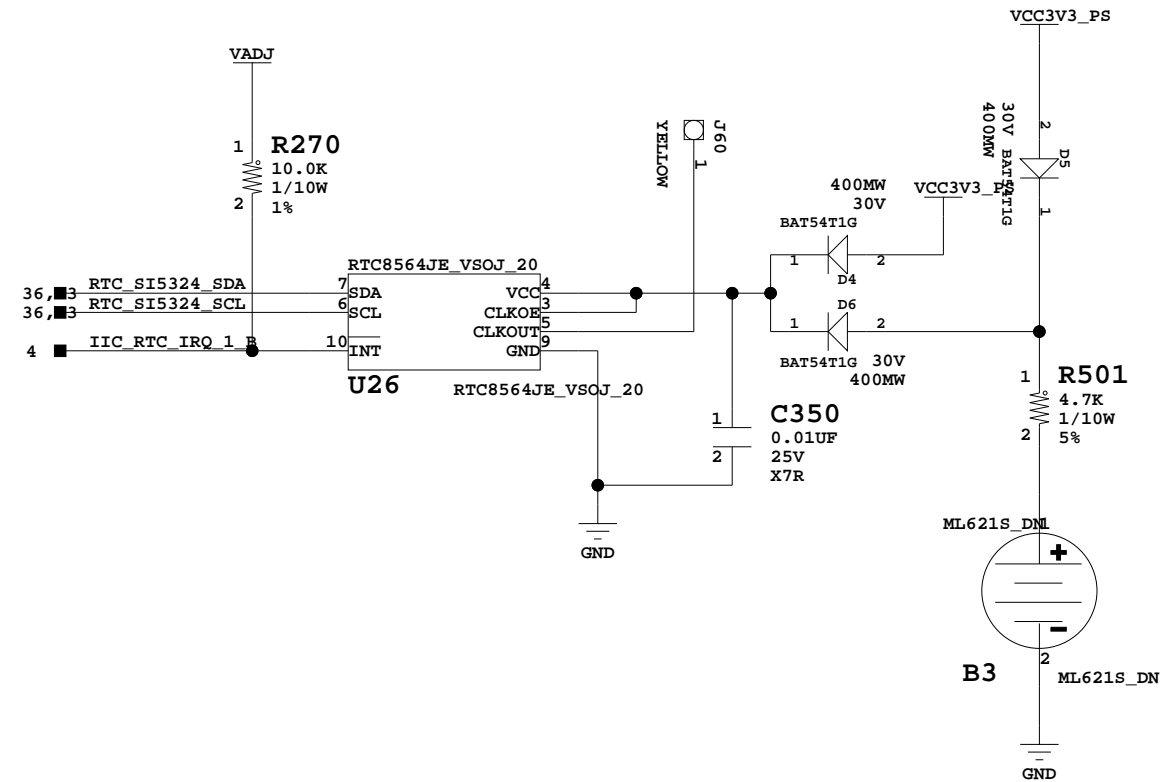
Title: IIC MUX, EEPROM
SCHEM, ROHS COMPLIANT
ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1

Sheet Size: B Rev: 02

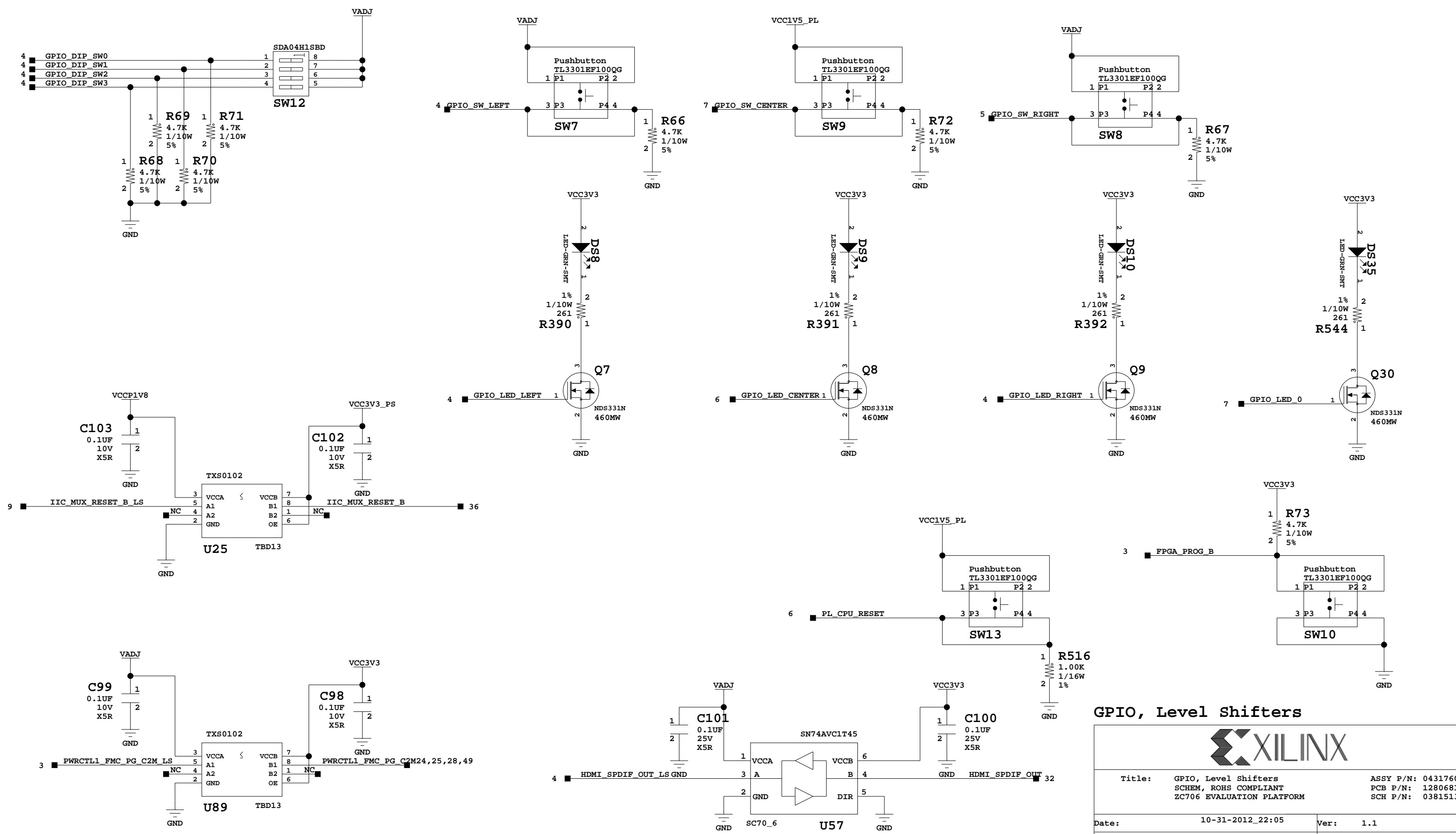
Sheet 36 of 58 Drawn By BF




IIC Real Time Clock, Port Expander



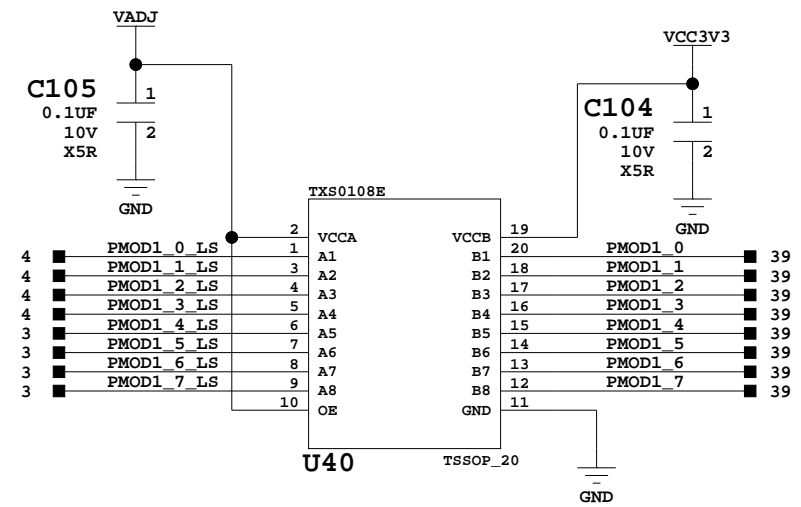
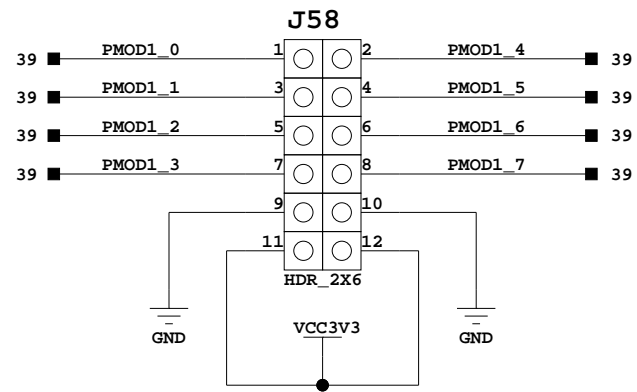
Title: IIC Real Time Clock, Port Expander		ASSY P/N: 0431760
SCHEM, ROHS COMPLIANT		PCB P/N: 1280681
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 37 of 58	Drawn By BF	



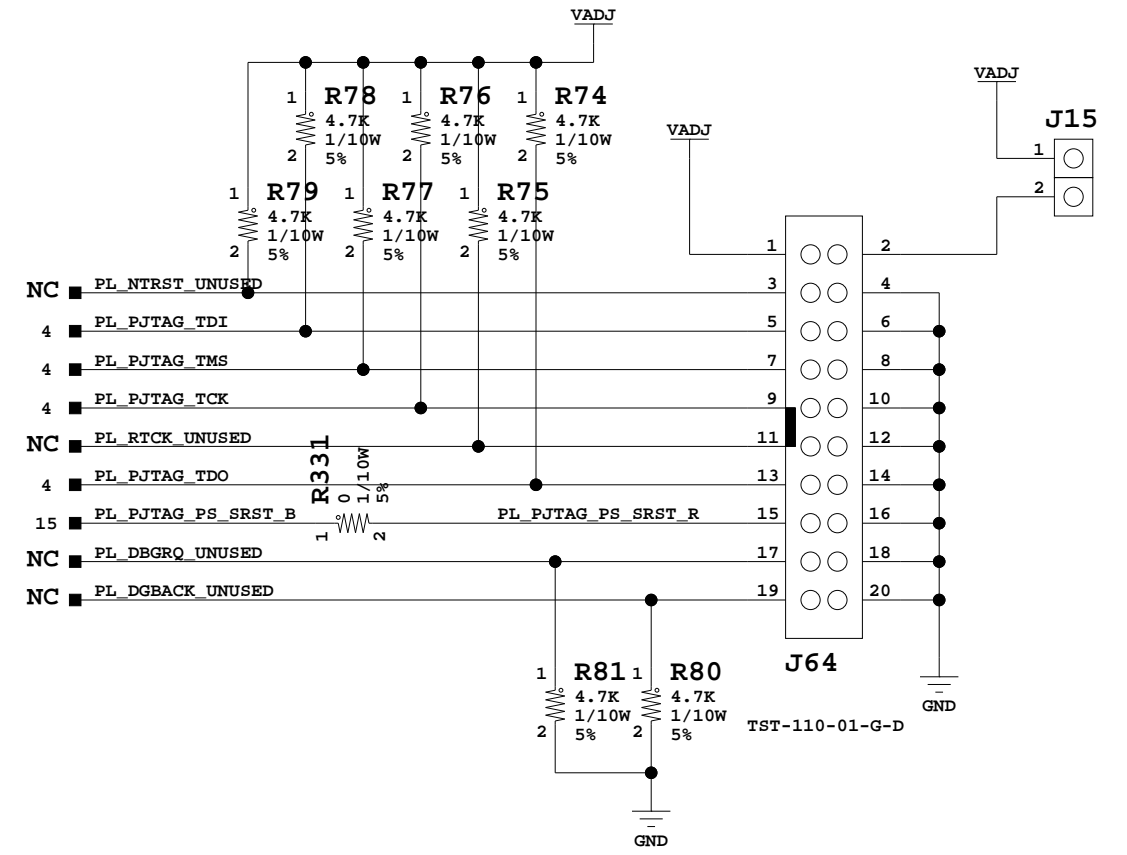
GPIO, Level Shifters



Title: GPIO, Level Shifters		ASSY P/N: 0431760
SCHEM, ROHS COMPLIANT		PCB P/N: 1280681
ZC706 EVALUATION PLATFORM		SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 38 of 58	Drawn By	BF



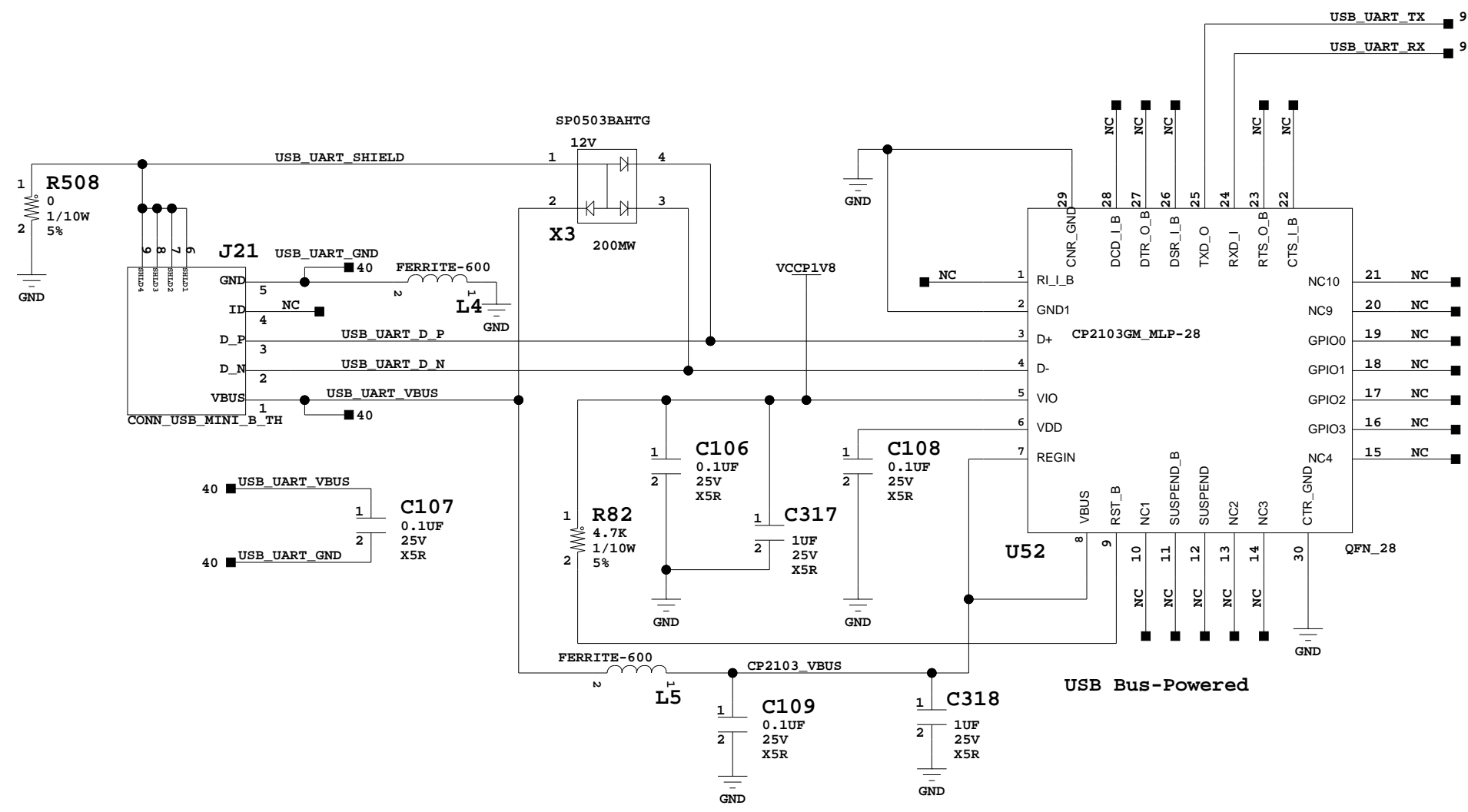
ARM PJTAG Header



ARM PJTAG Header, PMOD1



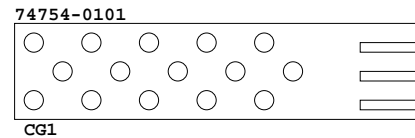
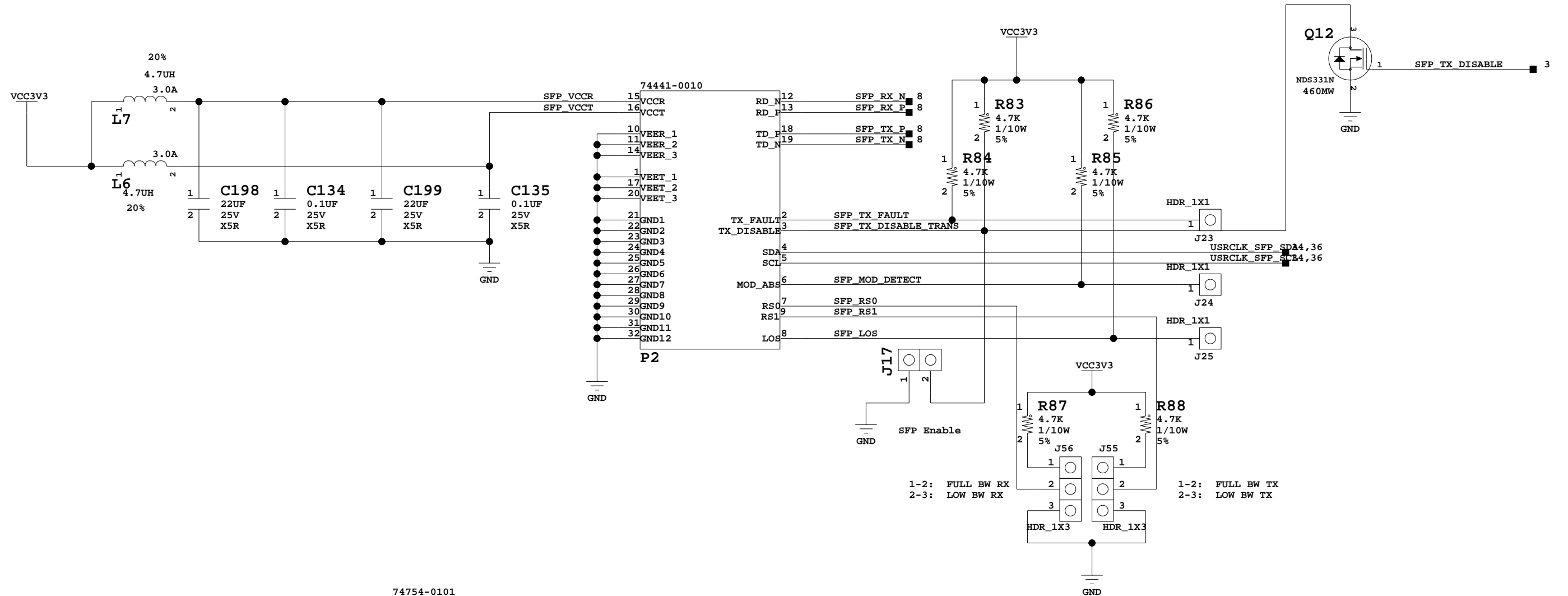
Title: ARM PJTAG Header, PMOD1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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USB UART



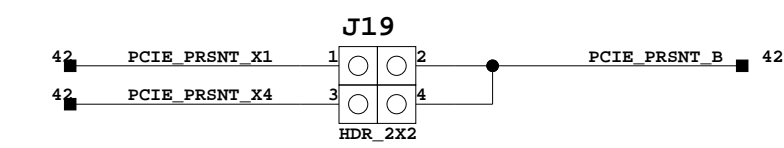
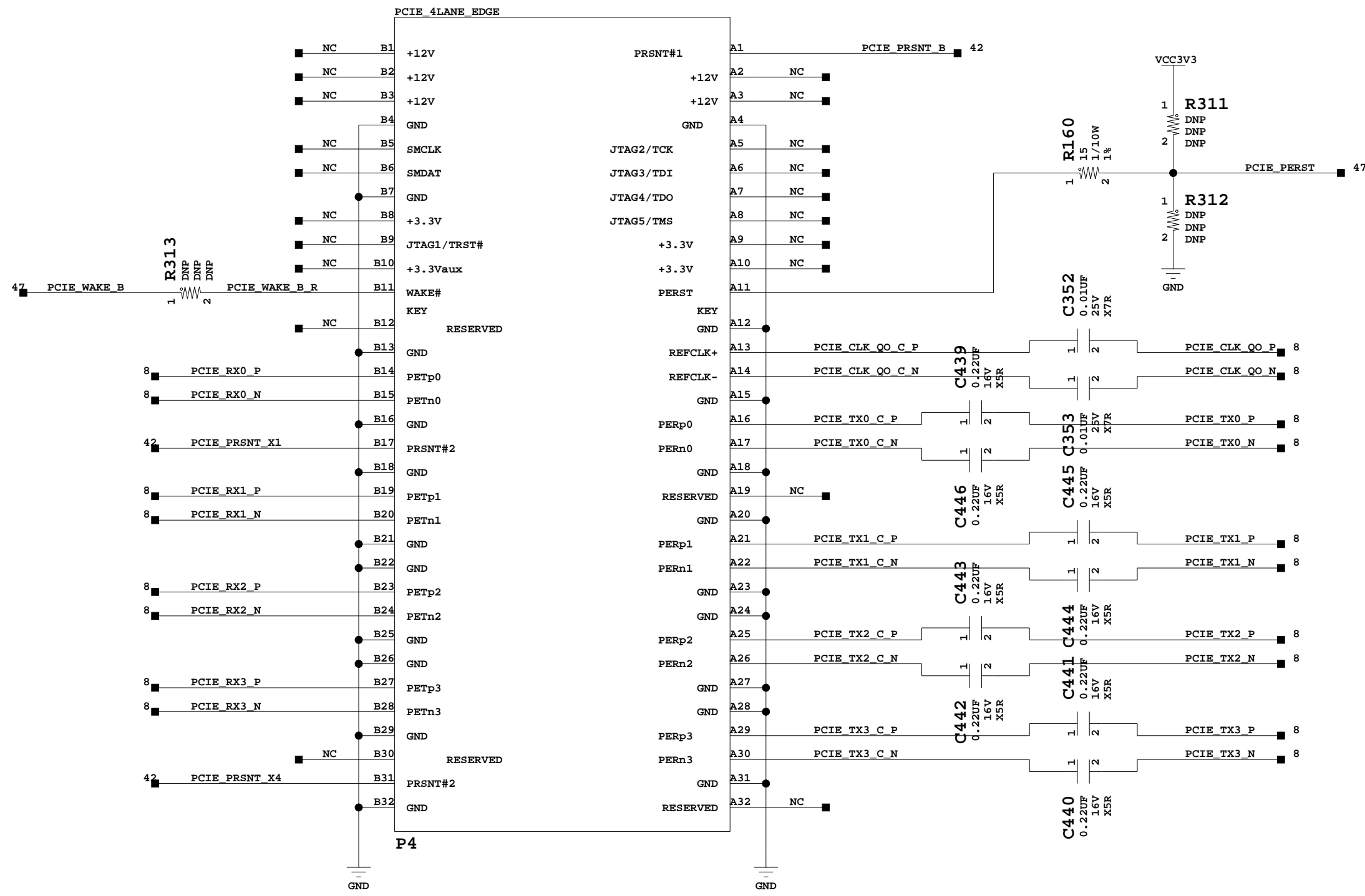
Title: USB UART SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date:	10-31-2012_22:05	Ver: 1.1
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SFP+ Connector and Cage



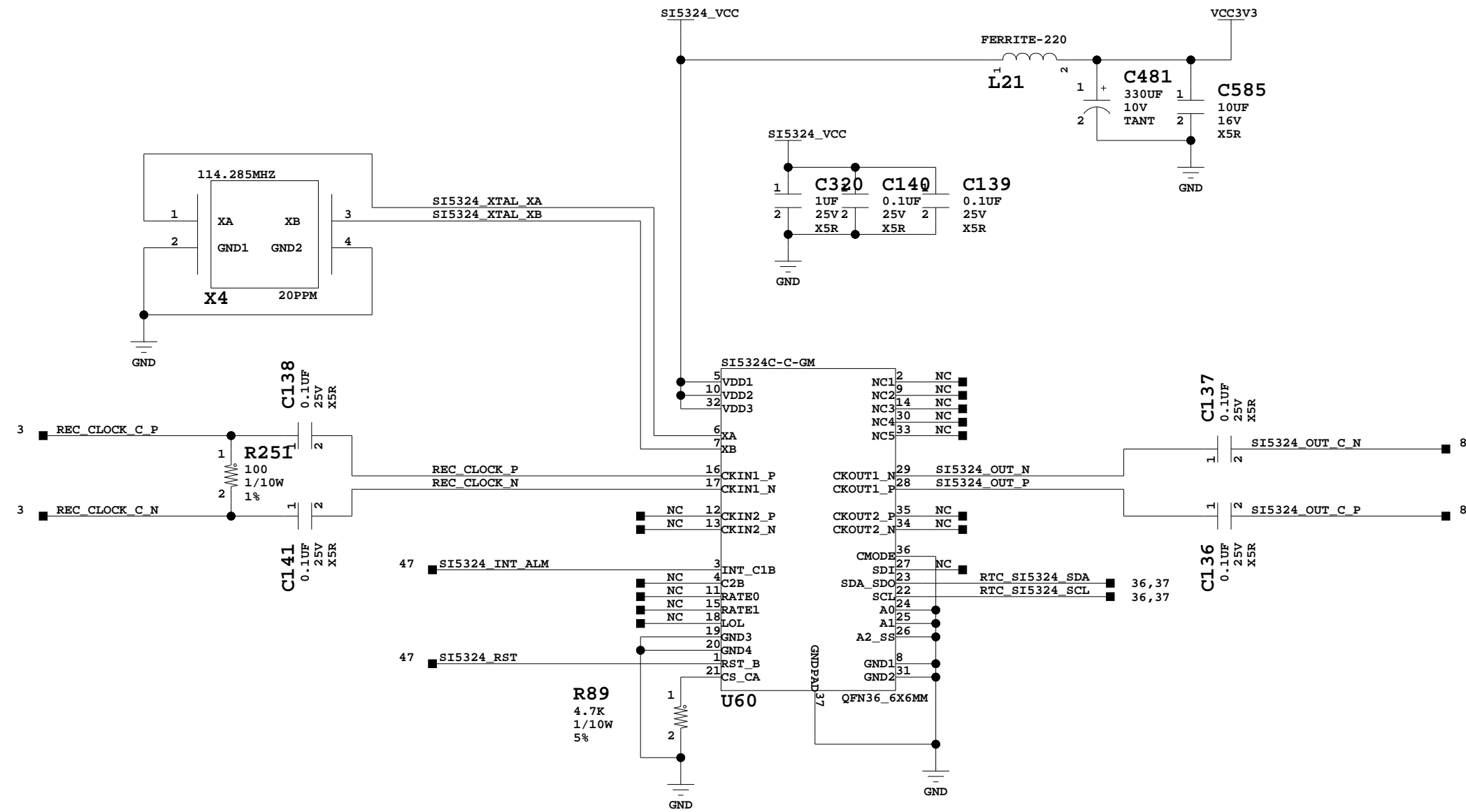
Title: SFP+ Connector and Cage SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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PCIe x4 Card edge



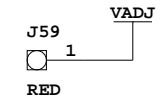
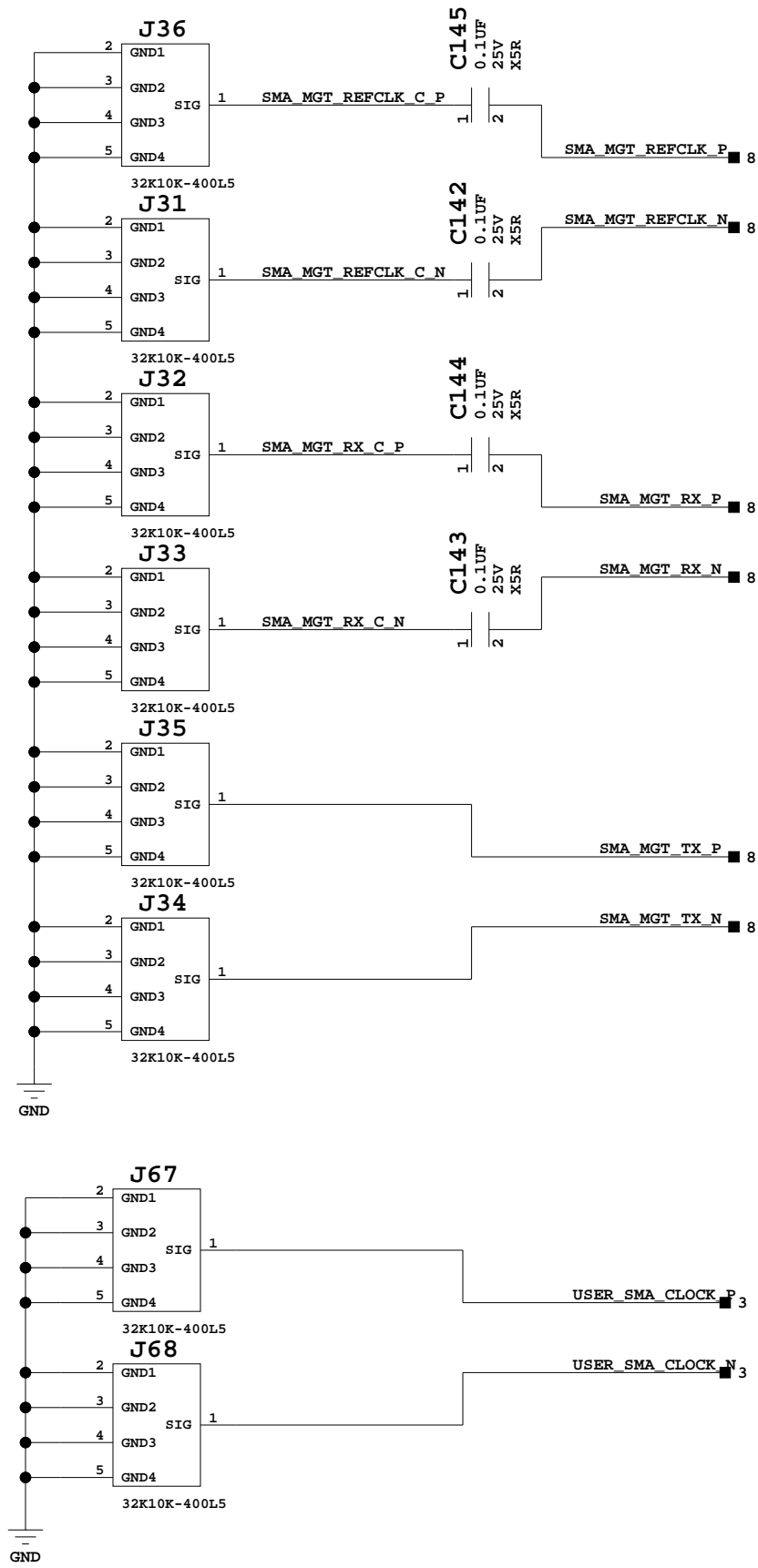
Title: PCIe x8 Card edge SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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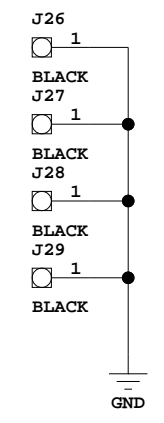
5324 Clock Recovery



Title: 5324 Clock Recovery SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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Place near FMC connectors



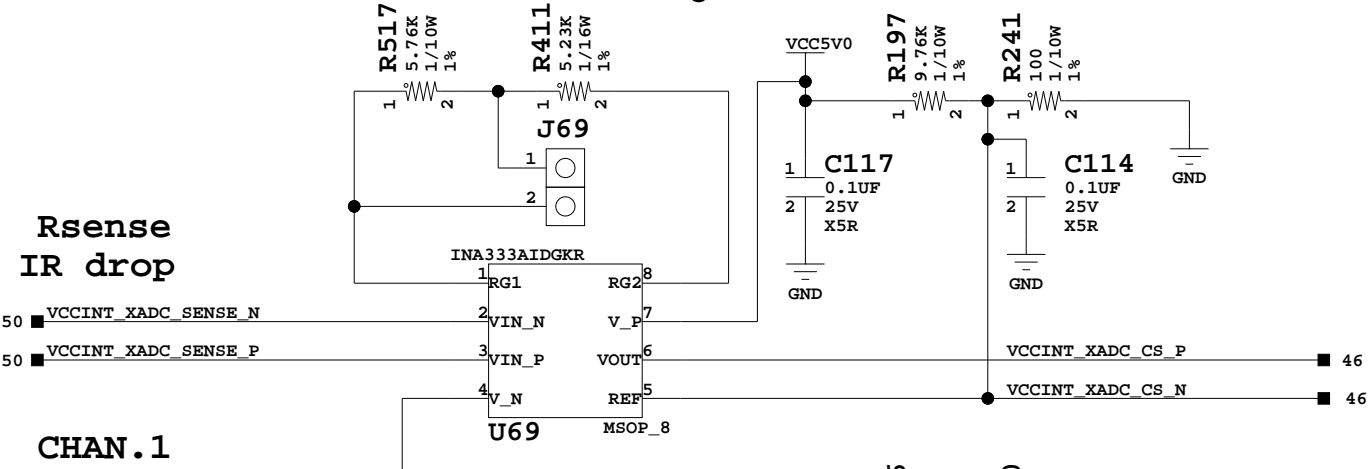
SMA and Testpoints



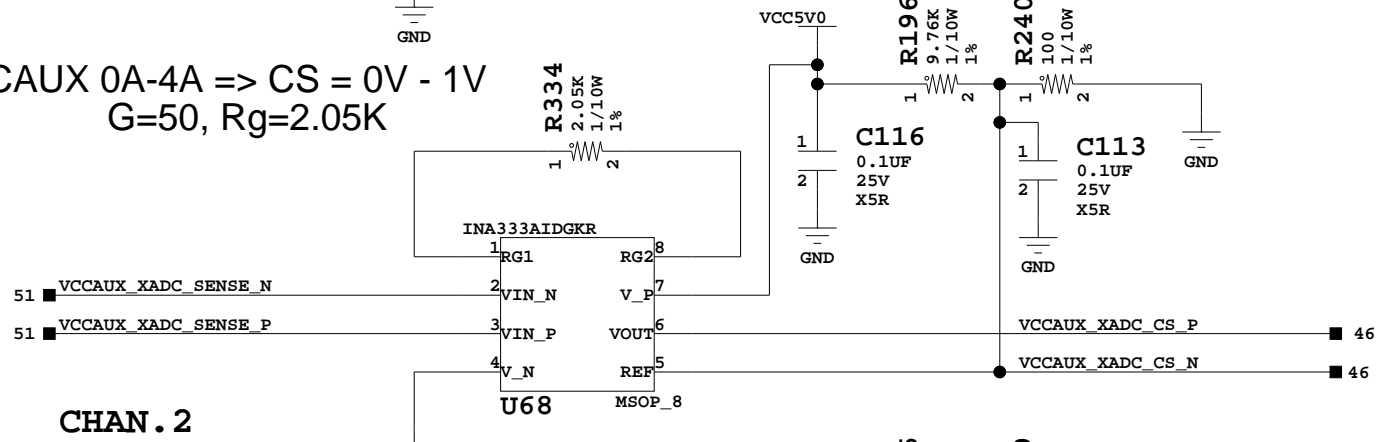
Title: SMA and Testpoints SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date:	10-31-2012_22:05	Ver: 1.1
Sheet Size:	B	Rev: 02
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XADC I/F MONITORING CIRCUIT PAGE 1

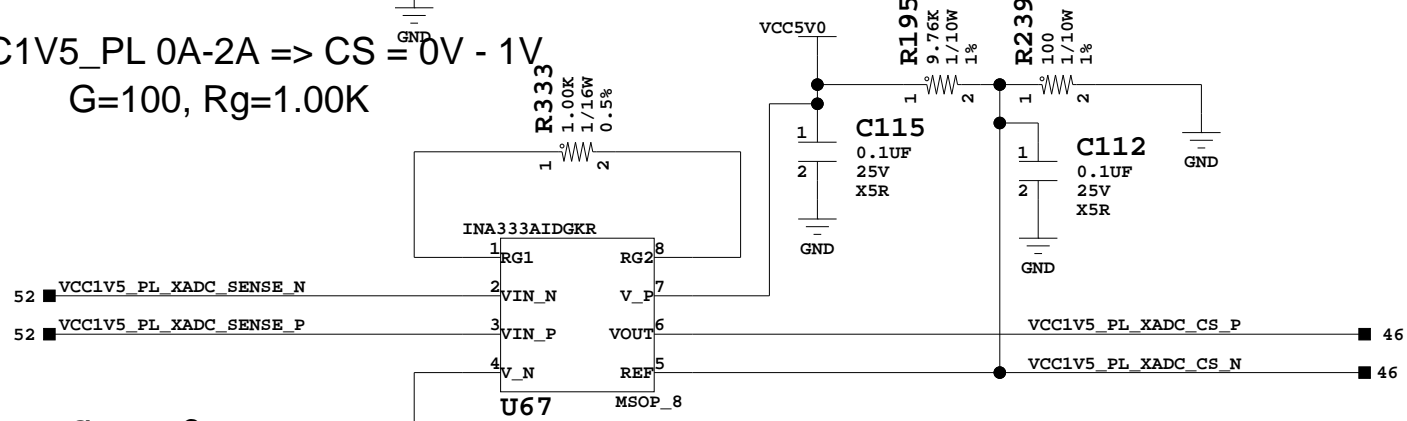
VCCINT 0A-16A => CS = 0V - 0.8V G=10, Rg=11K
 VCCINT 0A-8A => CS = 0V - 0.8V G=20, Rg=5.23K



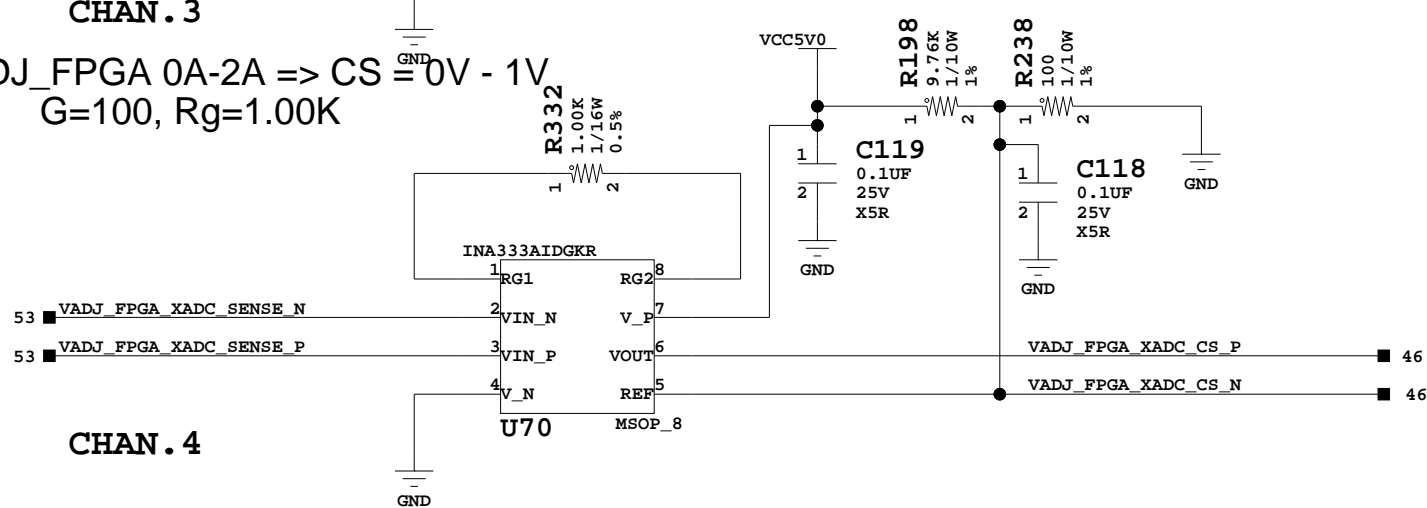
VCCAUX 0A-4A => CS = 0V - 1V
 G=50, Rg=2.05K



VCC1V5_PL 0A-2A => CS = 0V - 1V
 G=100, Rg=1.00K

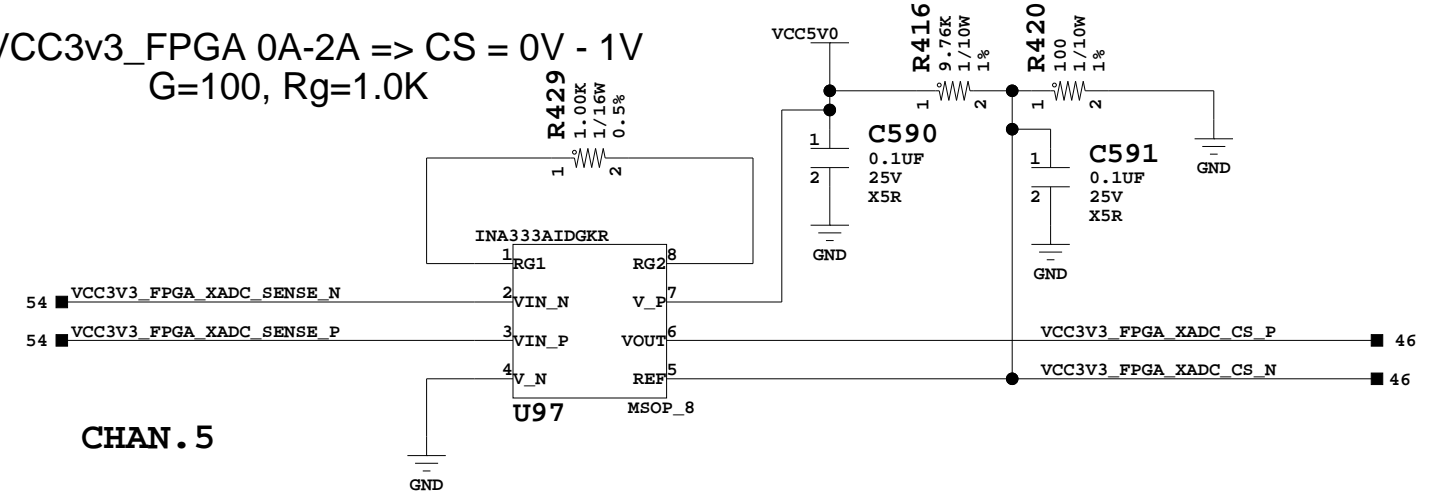


VADJ_FPGA 0A-2A => CS = 0V - 1V
 G=100, Rg=1.00K



CONTROLLER #1

VCC3v3_FPGA 0A-2A => CS = 0V - 1V
 G=100, Rg=1.0K



XADC I/F Monitoring Page 1

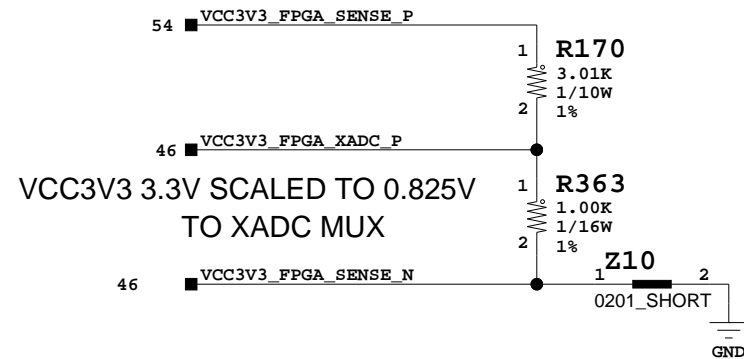
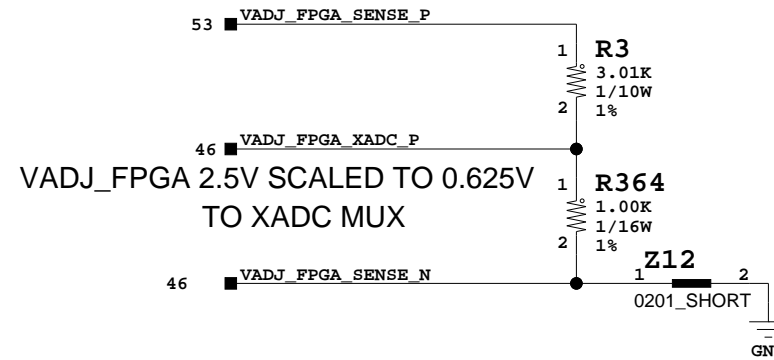
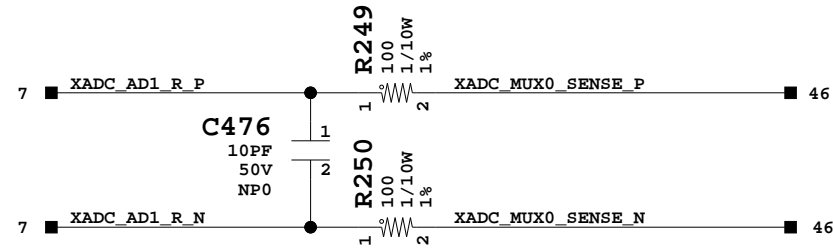
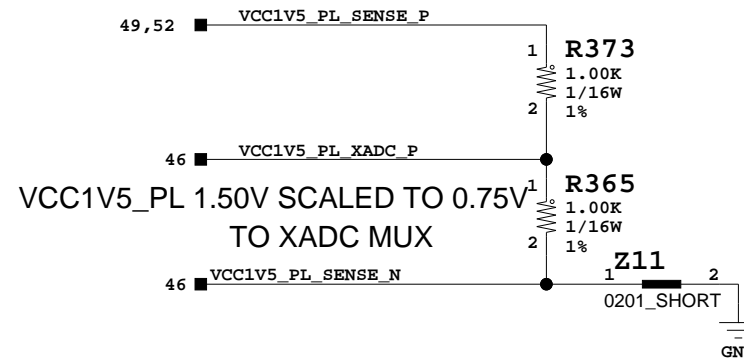
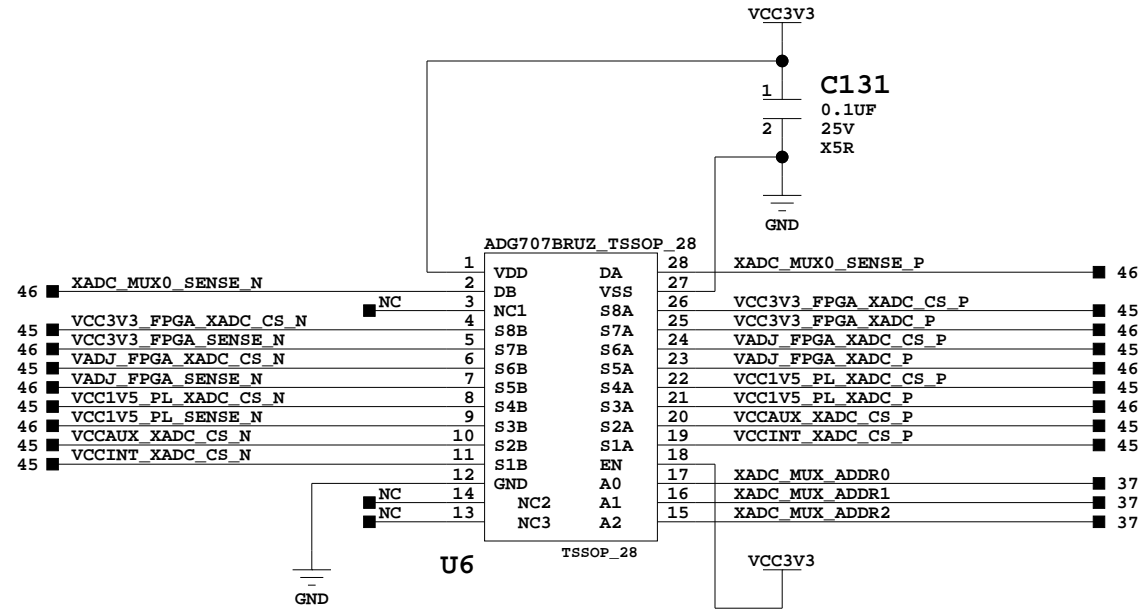


Title: XADC I/F Monitoring Page 1
 SCHEM, ROHS COMPLIANT
 ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
 PCB P/N: 1280681
 SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1
 Sheet Size: B Rev: 02
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XADC I/F MONITORING CIRCUIT PAGE 2



XADC I/F Monitoring Page 2



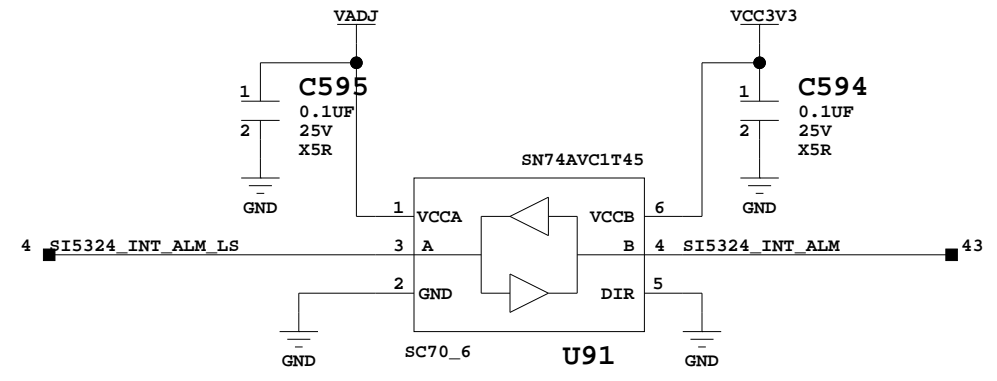
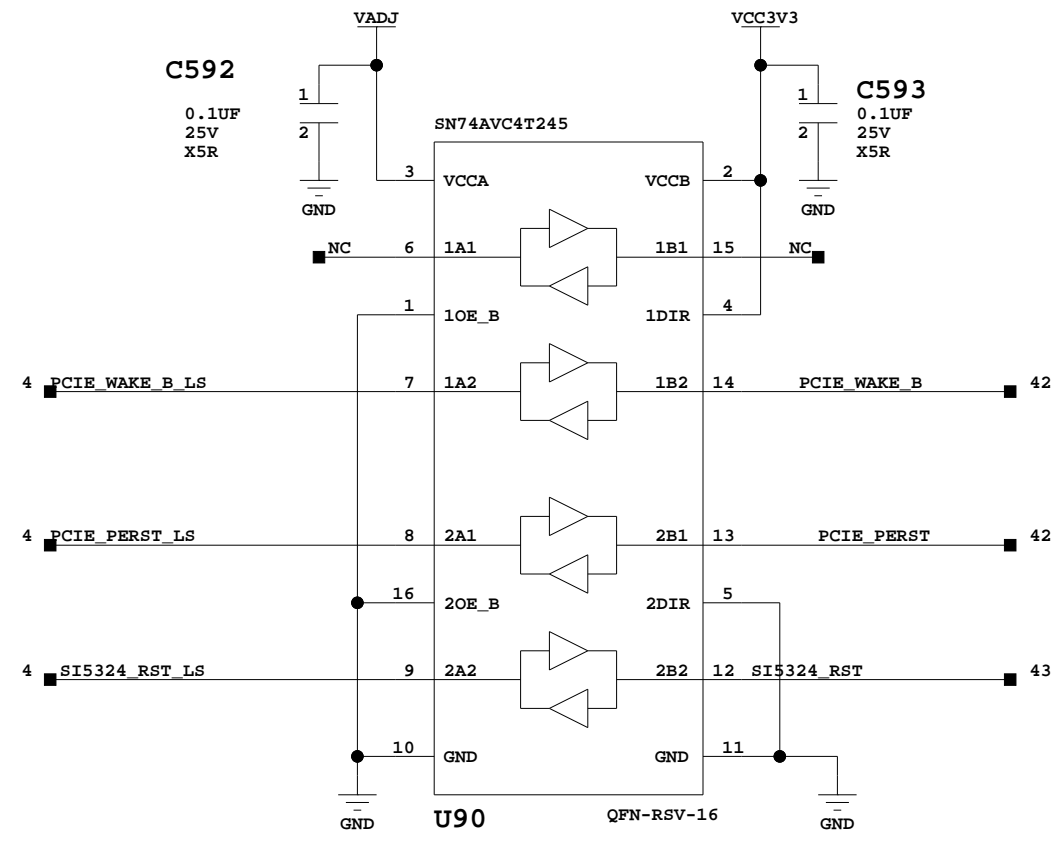
Title: XADC I/F Monitoring Page 3
 SCHEM, ROHS COMPLIANT
 ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
 PCB P/N: 1280681
 SCH P/N: 0381513

Date: 10-31-2012_22:05 Ver: 1.1

Sheet Size: B Rev: 02

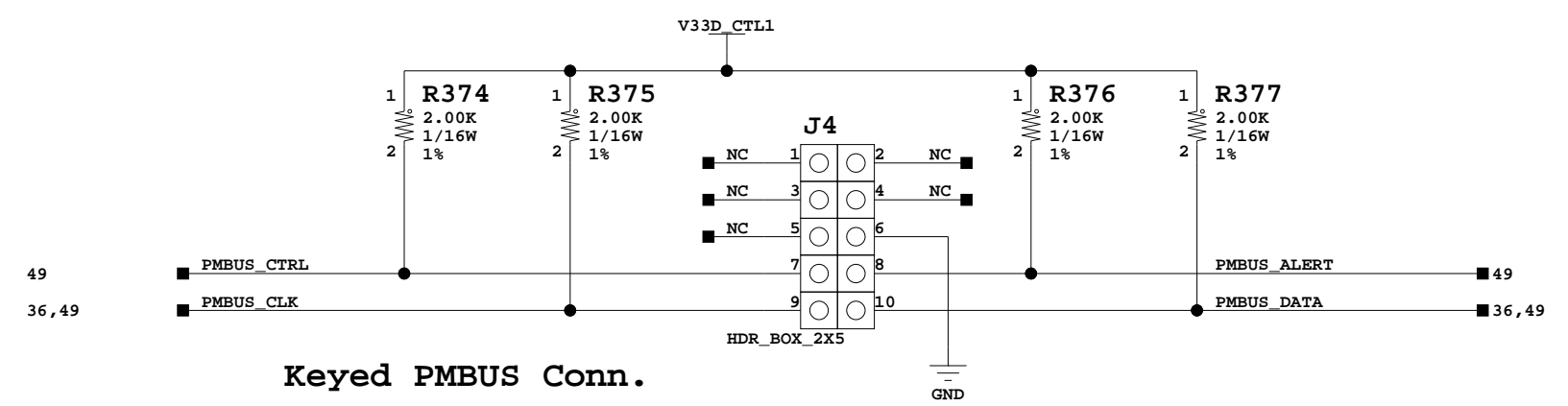
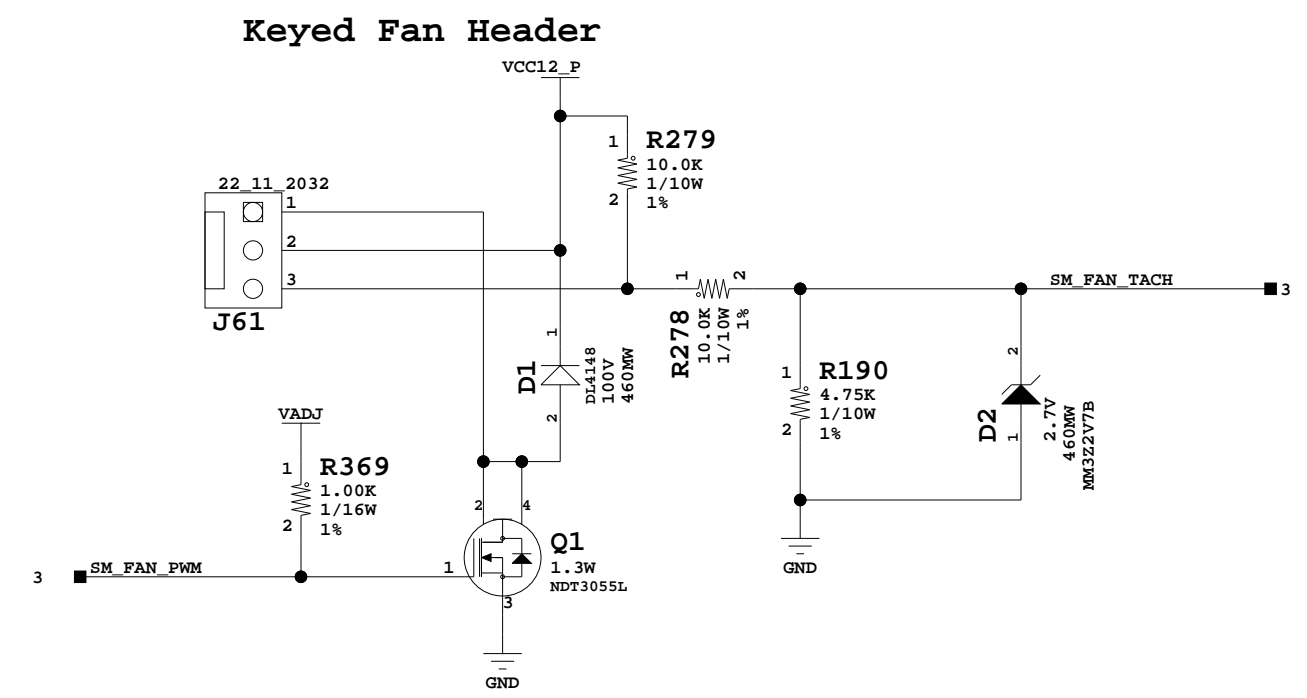
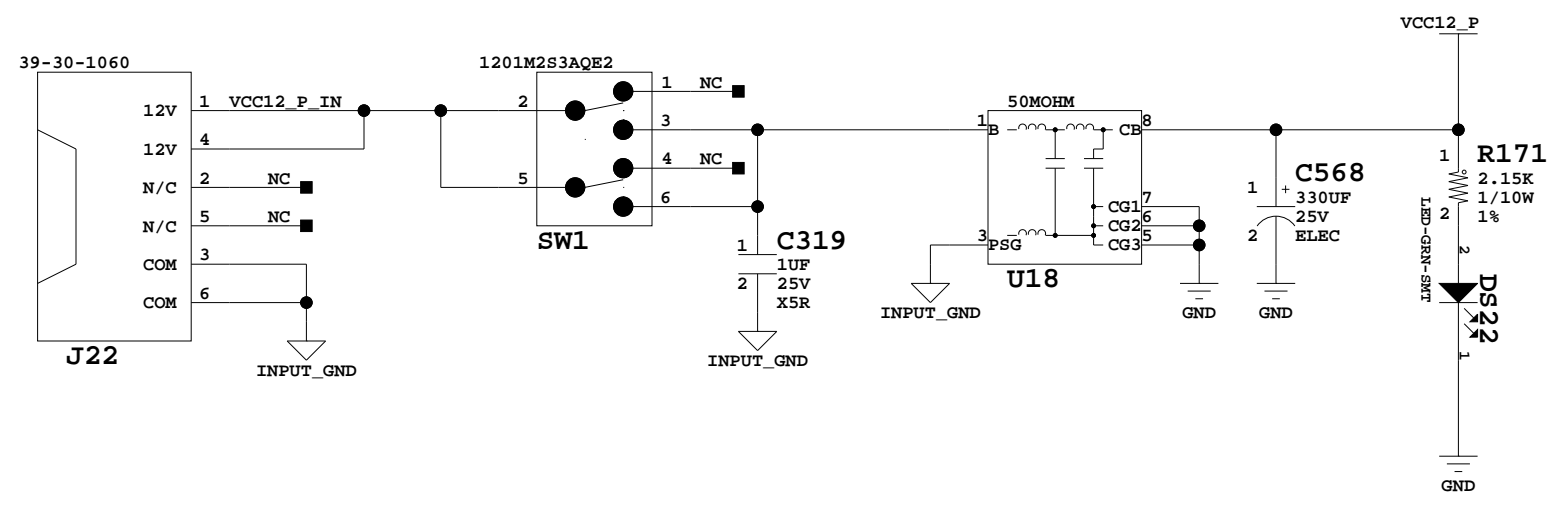
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Level Shifters

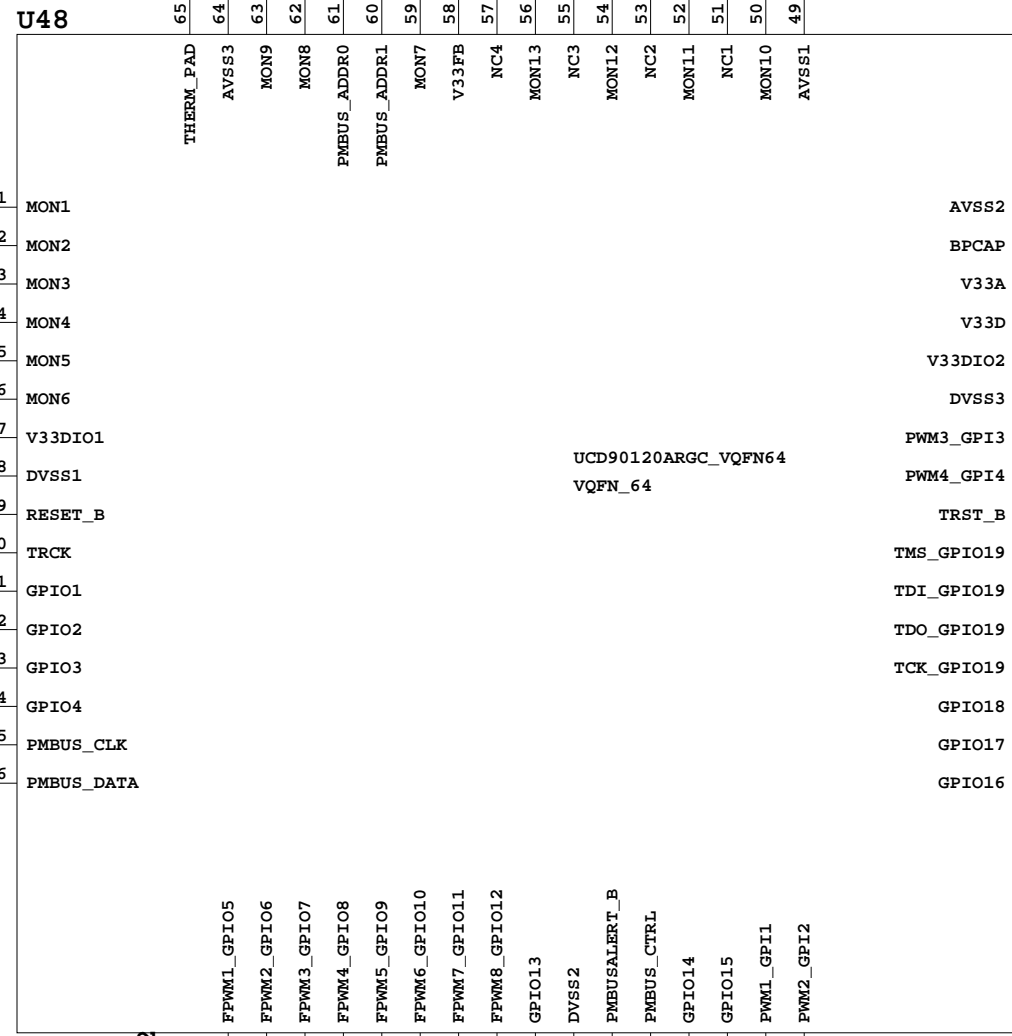
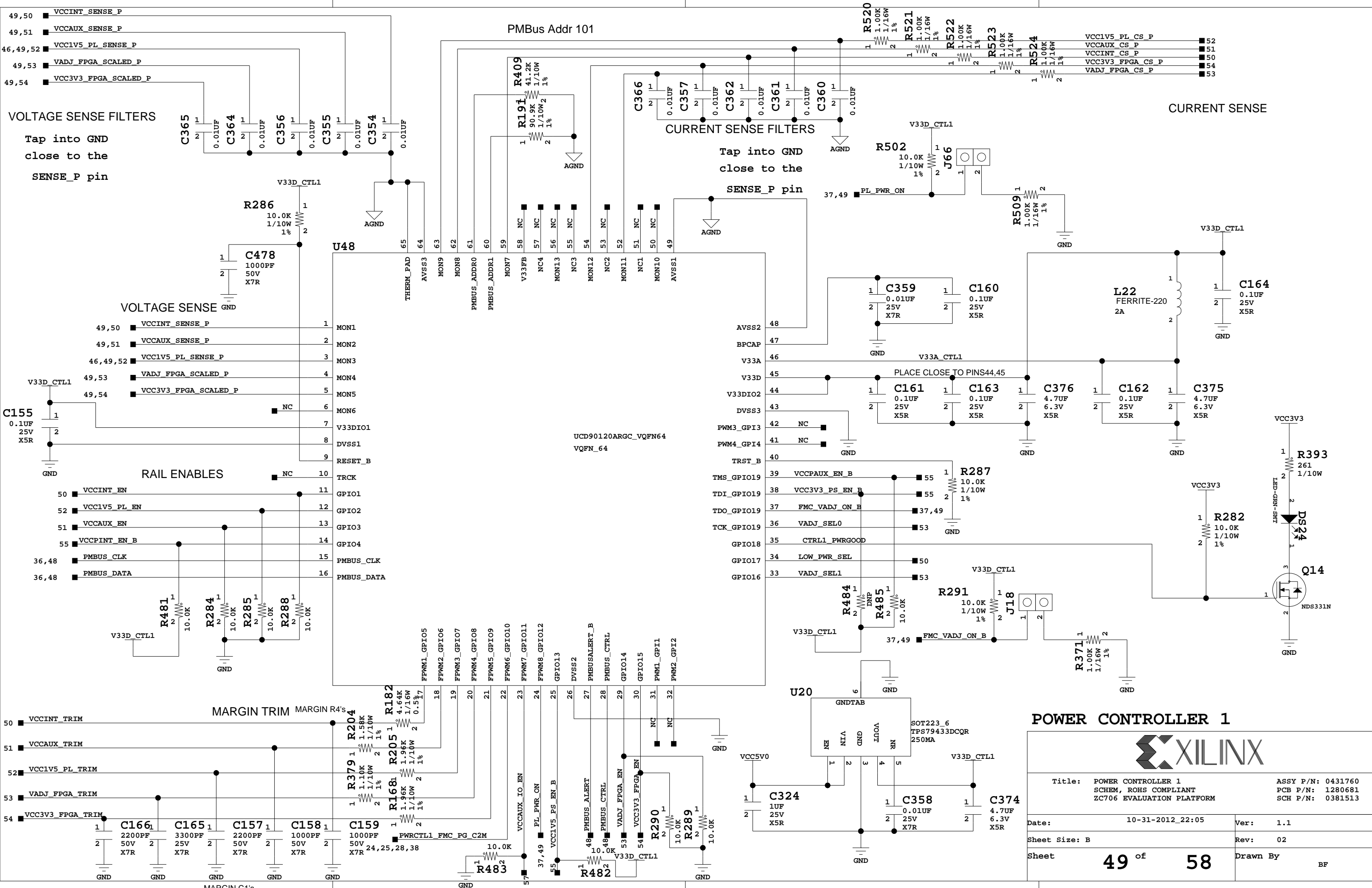


Title: Level Shifters SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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Power Connectors

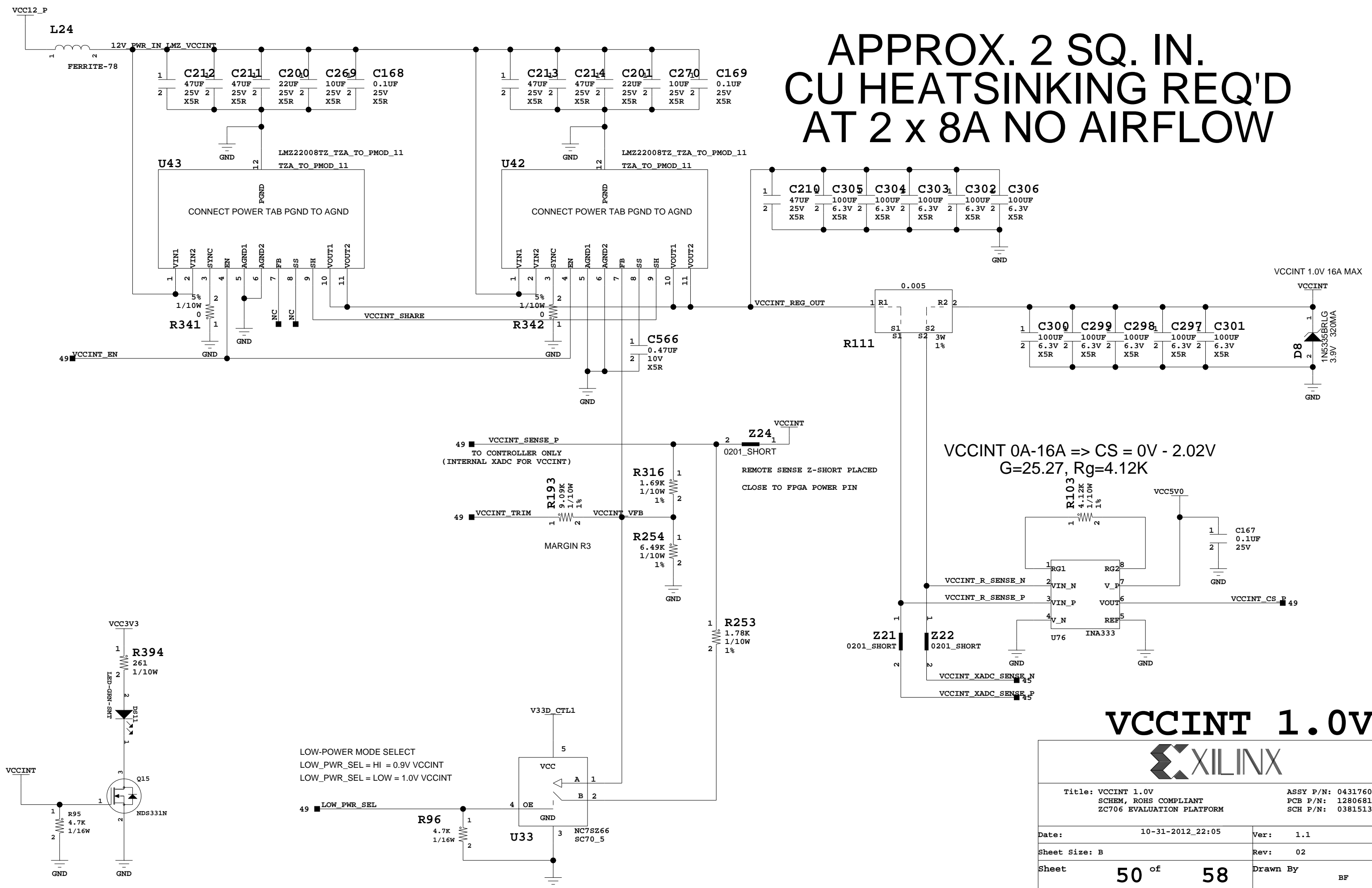
Title: Power Connectors SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM	
ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date: 10-31-2012_22:05	Ver: 1.1
Sheet Size: B	Rev: 02
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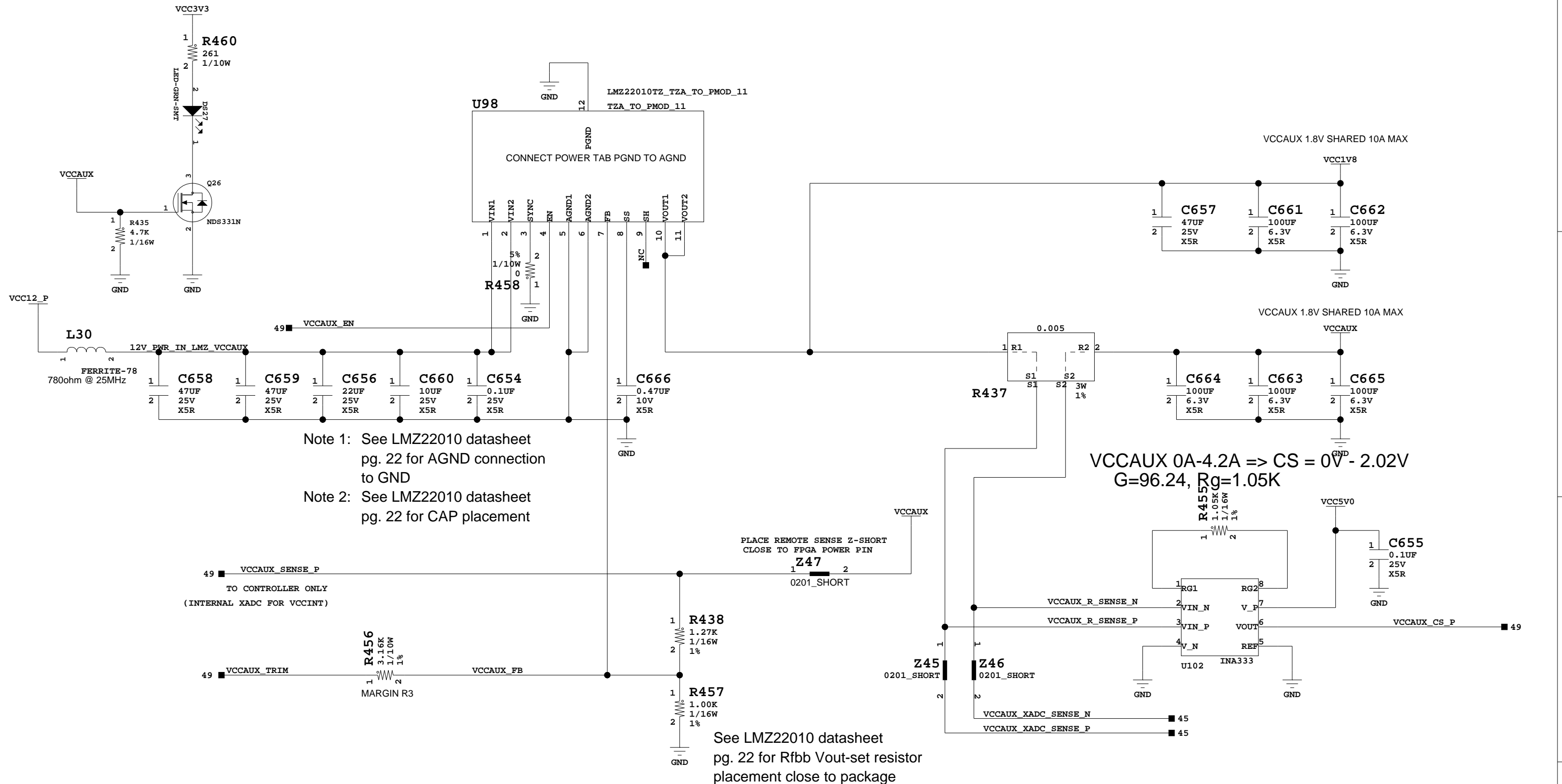


Title: POWER CONTROLLER 1	
SCHEM, ROHS COMPLIANT	
ZC706 EVALUATION PLATFORM	
Date: 10-31-2012_22:05	Ver: 1.1
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ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

APPROX. 2 SQ. IN. CU HEATSINKING REQ'D AT 2 x 8A NO AIRFLOW





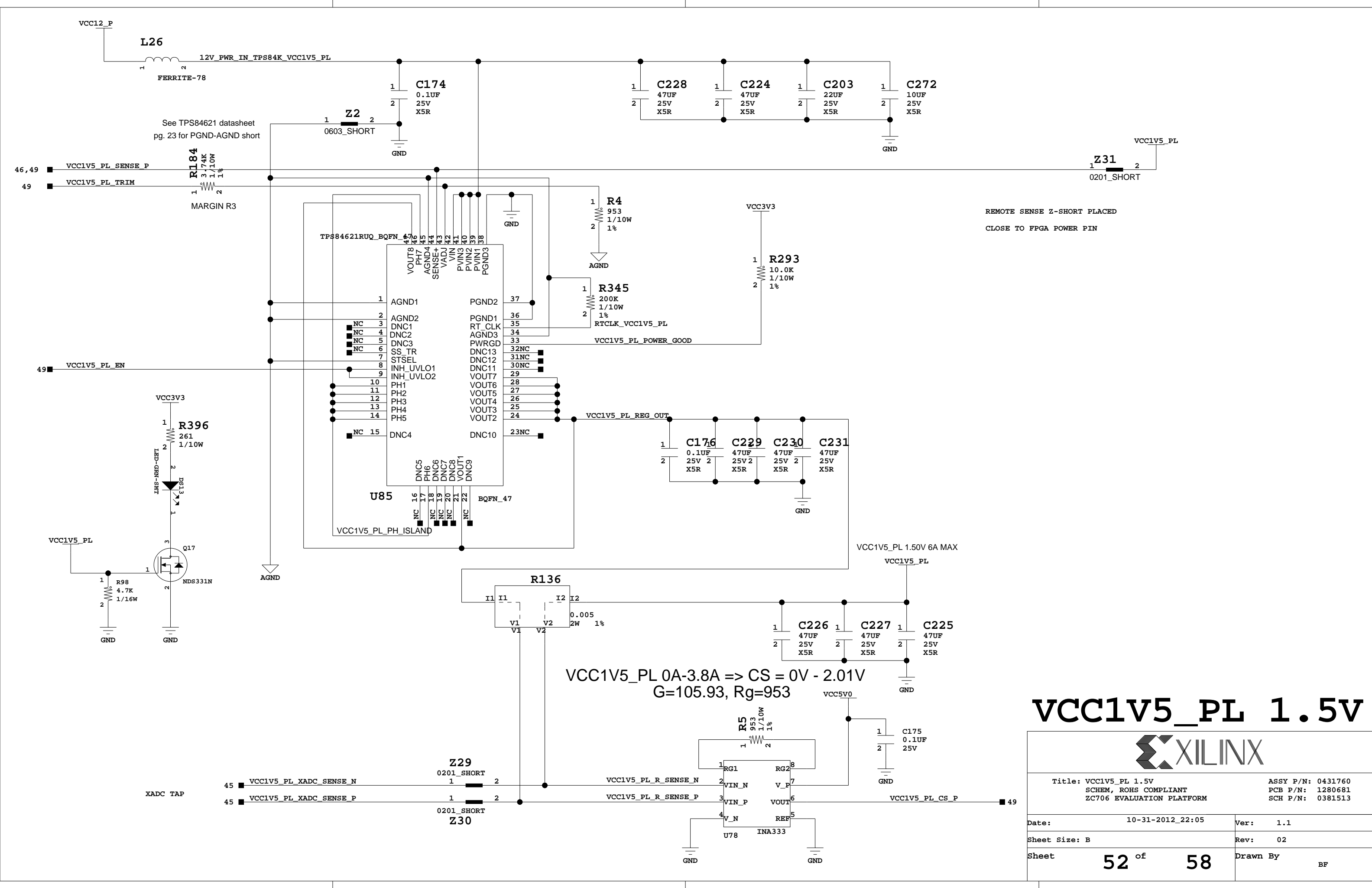
VCC1V8 / VCCAUX 1.8V



Title: VCC1V8/VCCAUX 1.8V SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM

ASSY P/N: 0431760
PCB P/N: 1280681
SCH P/N: 0381513

Date:	10-31-2012_22:05	Ver:	1.1
Sheet Size:	B	Rev:	02
Sheet	51 of 58	Drawn By	BF



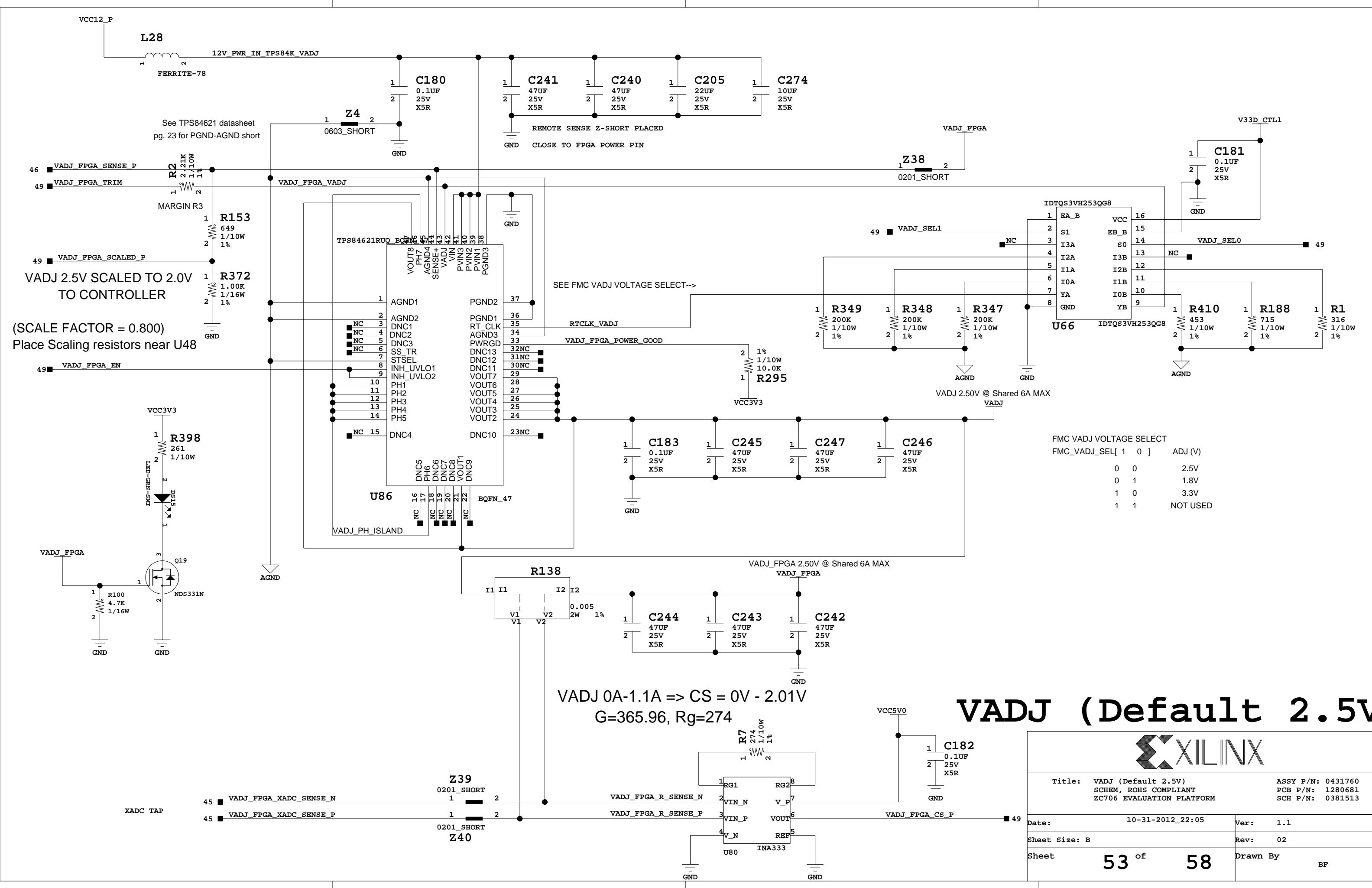
REMOTE SENSE Z-SHORT PLACED
CLOSE TO FPGA POWER PIN

VCC1V5_PL 0A-3.8A => CS = 0V - 2.01V
G=105.93, Rg=953

VCC1V5_PL 1.5V



Title: VCC1V5_PL 1.5V SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
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See TPS84621 datasheet pg. 23 for PGND-AGND short

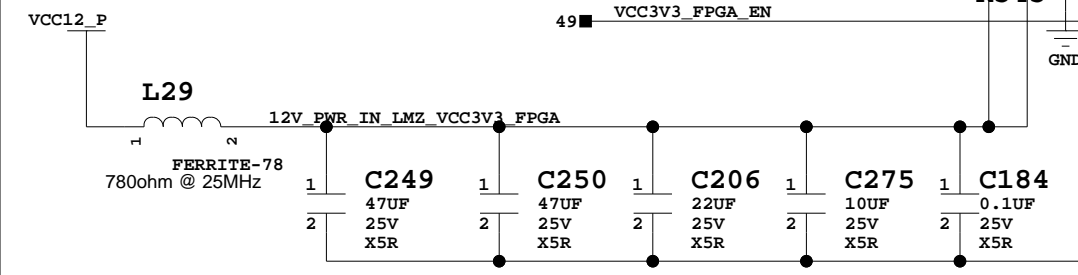
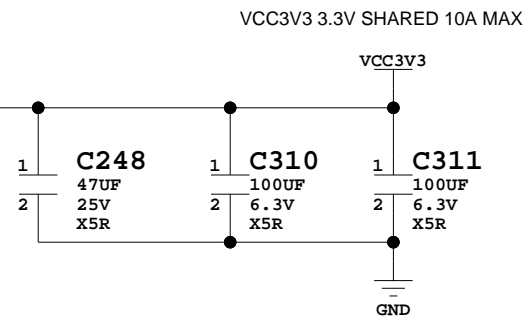
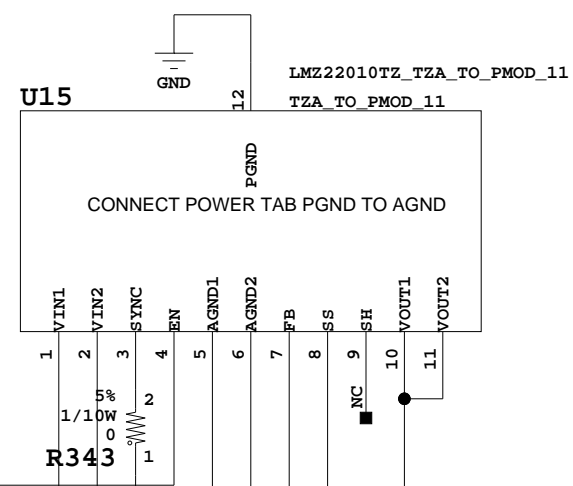
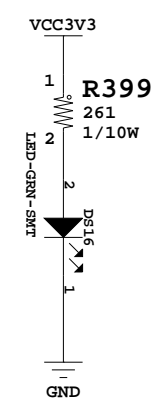
VADJ 2.5V SCALED TO 2.0V TO CONTROLLER
(SCALE FACTOR = 0.800)
Place Scaling resistors near U48

VADJ 0A-1.1A => CS = 0V - 2.01V
G=365.96, Rg=274

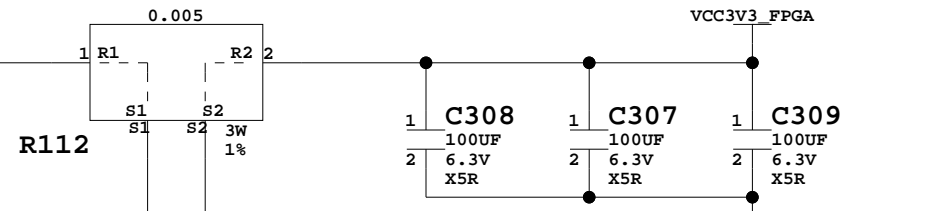
VADJ (Default 2.5V)



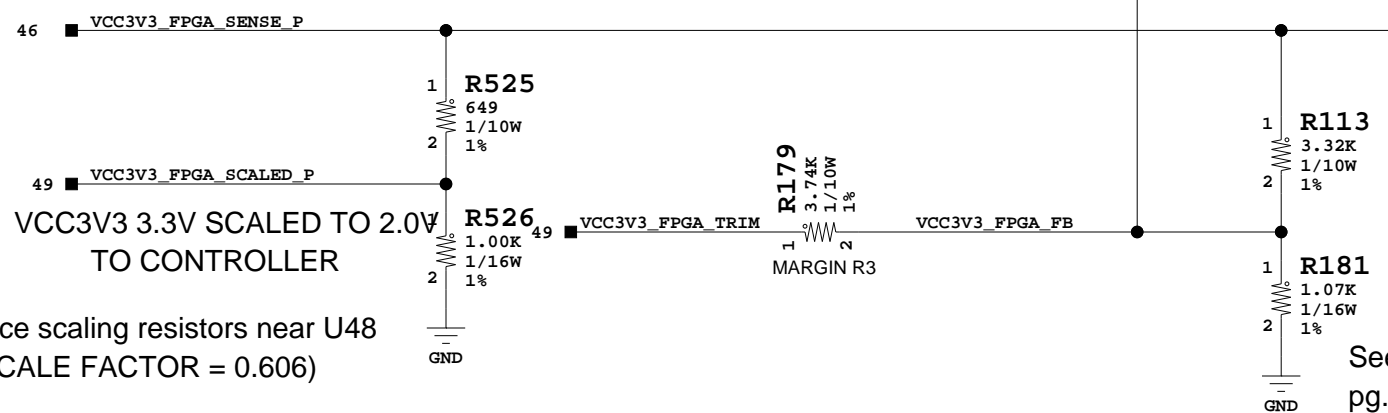
Title: VADJ (Default 2.5V) SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
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Note 1: See LMZ22010 datasheet pg. 22 for AGND connection to GND
 Note 2: See LMZ22010 datasheet pg. 22 for CAP placement



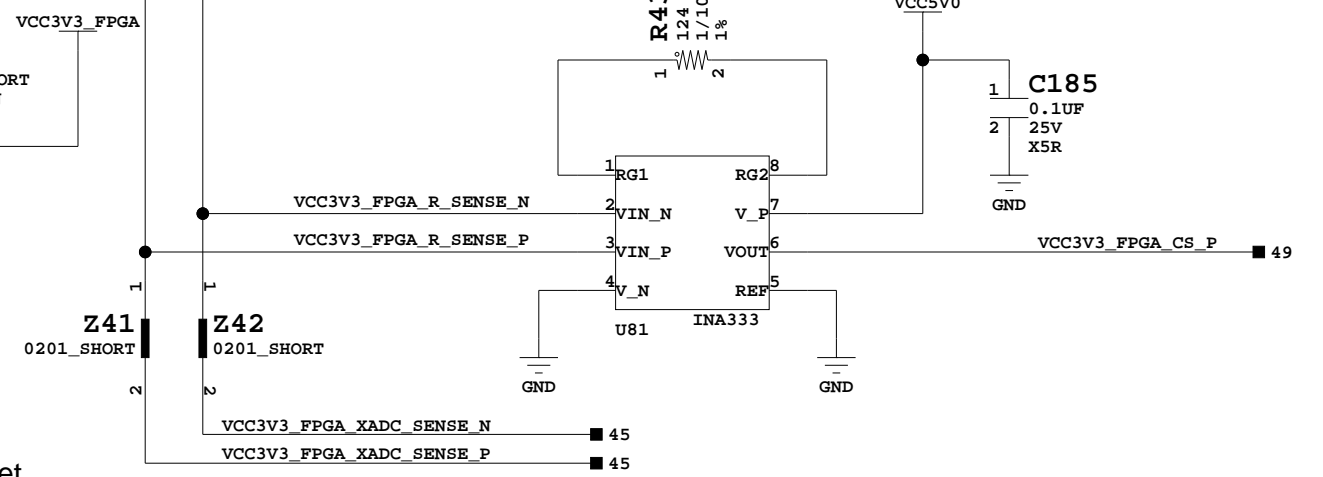
VCC3V3_FPGA 0A - 0.5A => CS = 0V - 2.02V
 $G=807.45, R_g=124$



Place scaling resistors near U48 (SCALE FACTOR = 0.606)

See LMZ22010 datasheet pg. 22 for Rfbb Vout-set resistor placement close to package

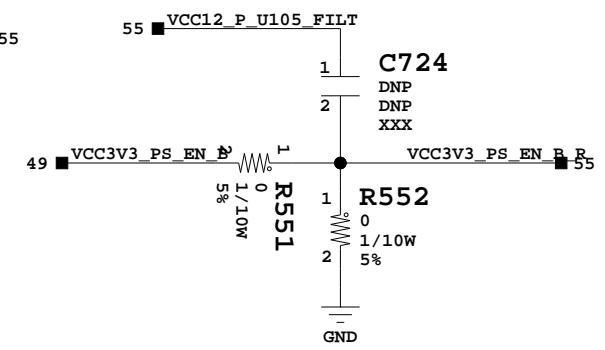
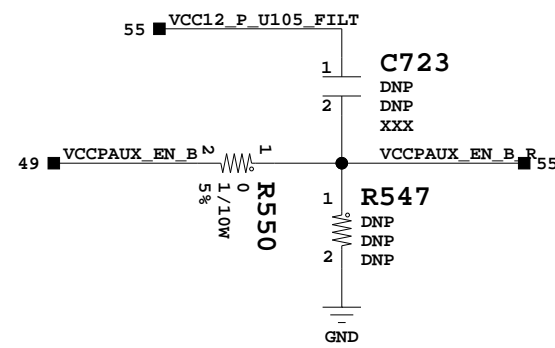
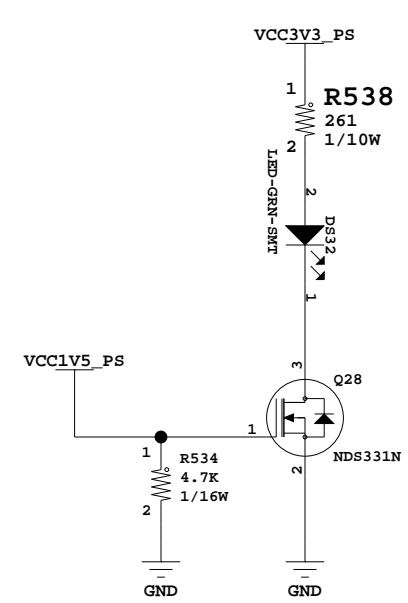
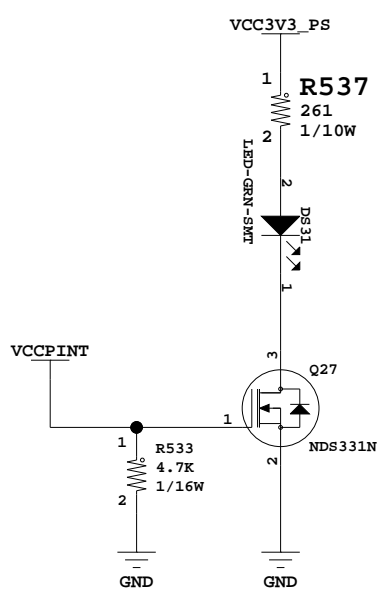
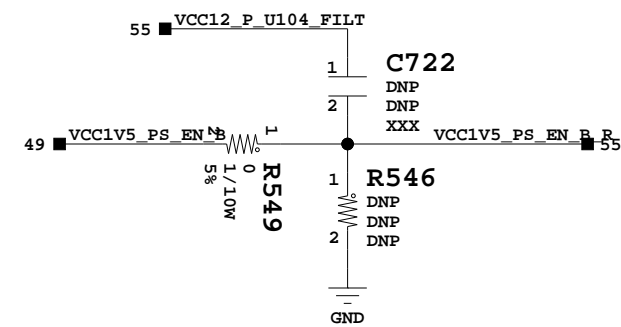
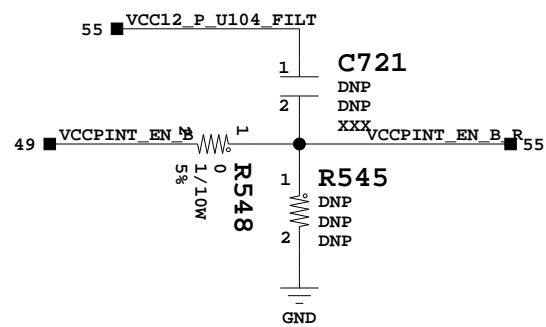
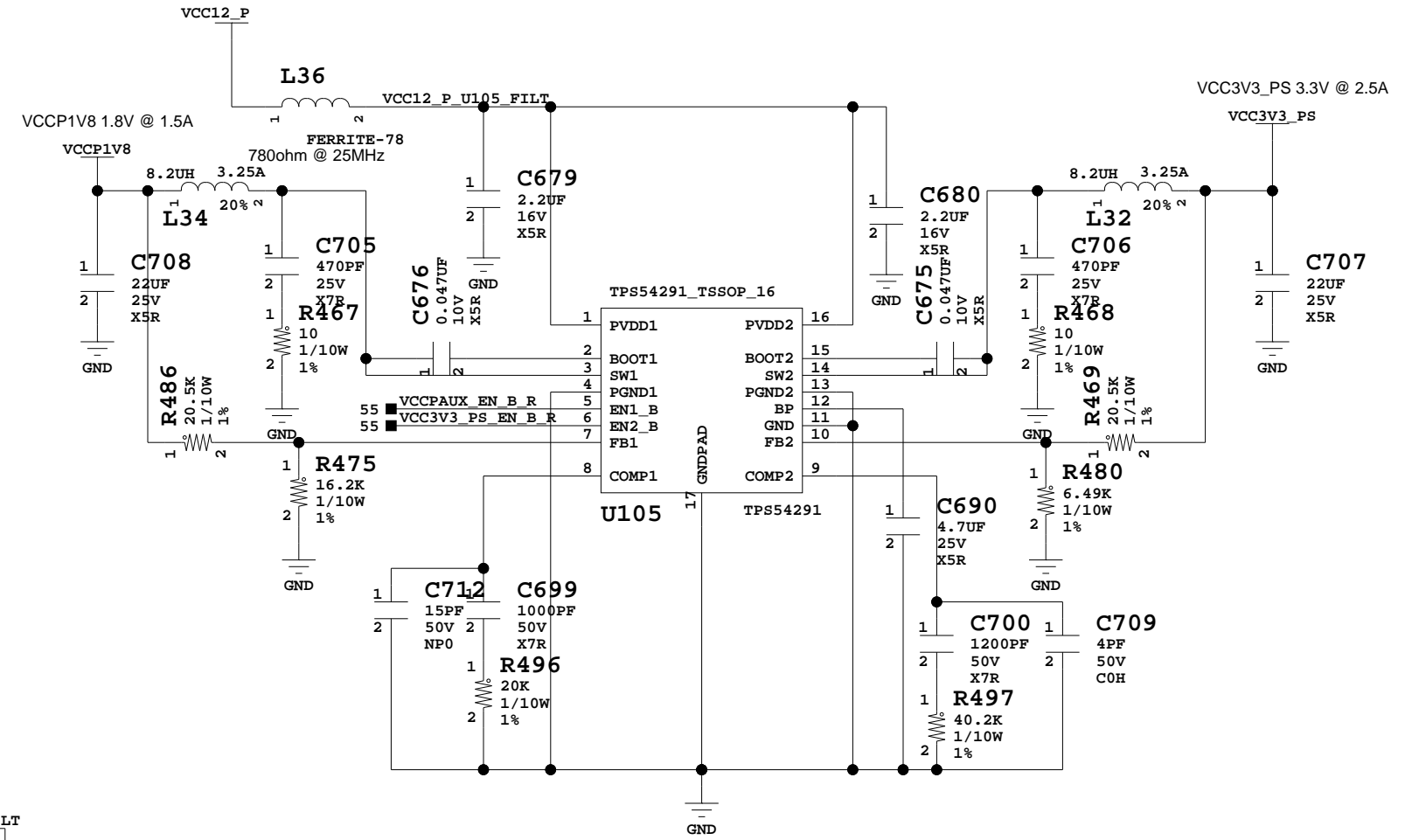
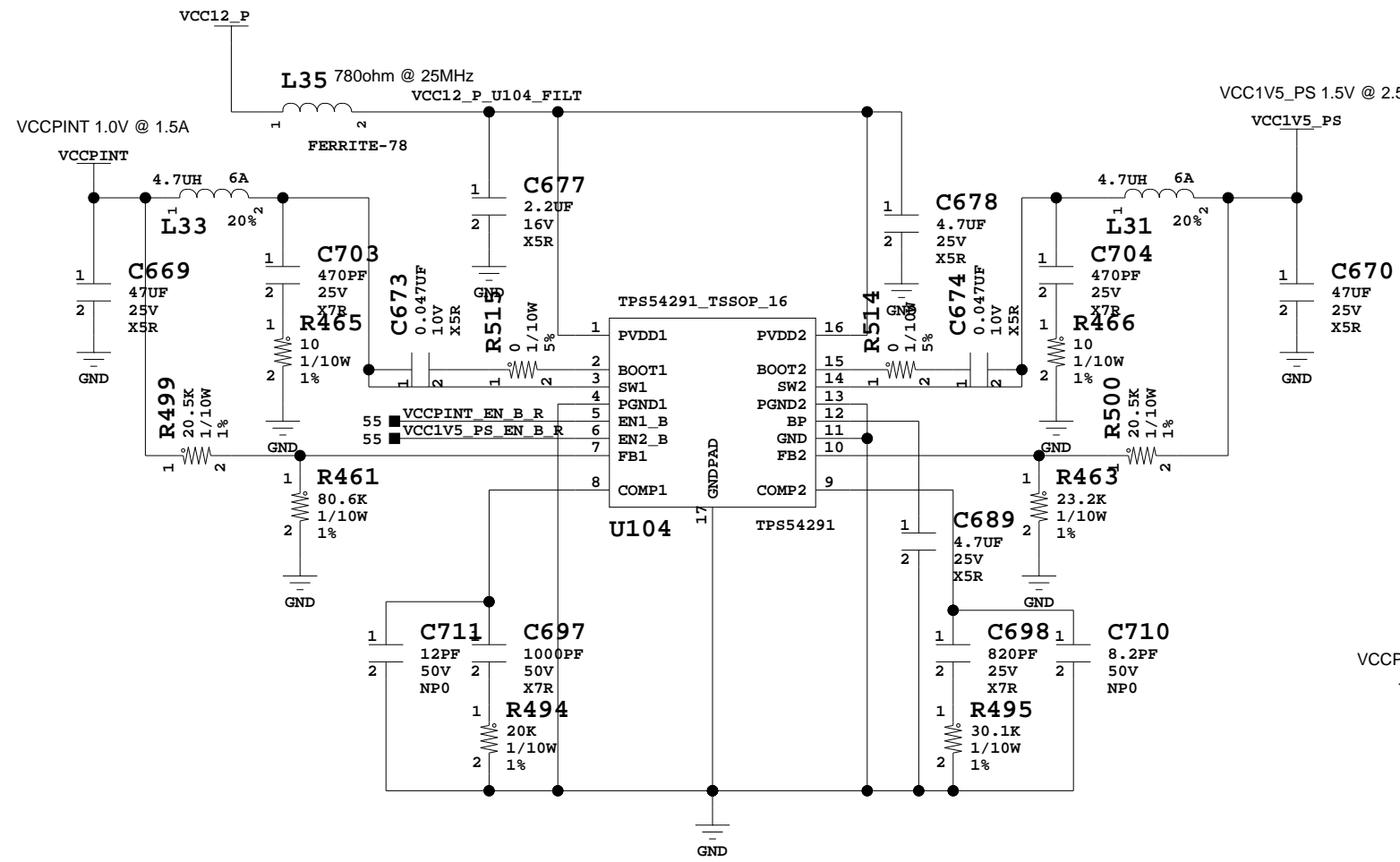
PLACE REMOTE SENSE Z-SHORT CLOSE TO FPGA POWER PIN
 Z44 0201_SHORT



VCC3V3/VCC3V3_FPGA 3.3V



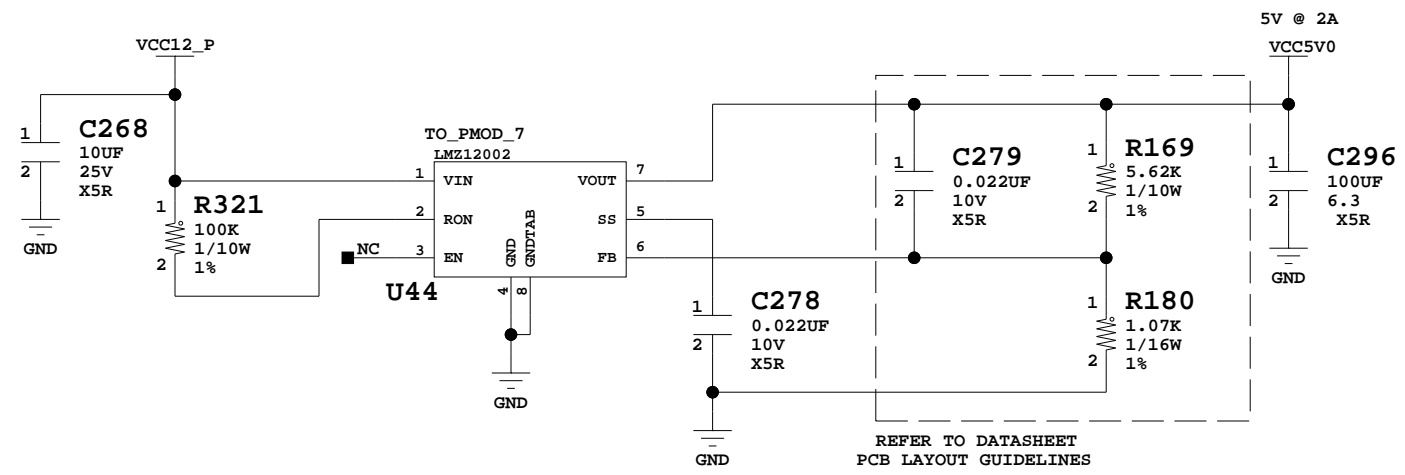
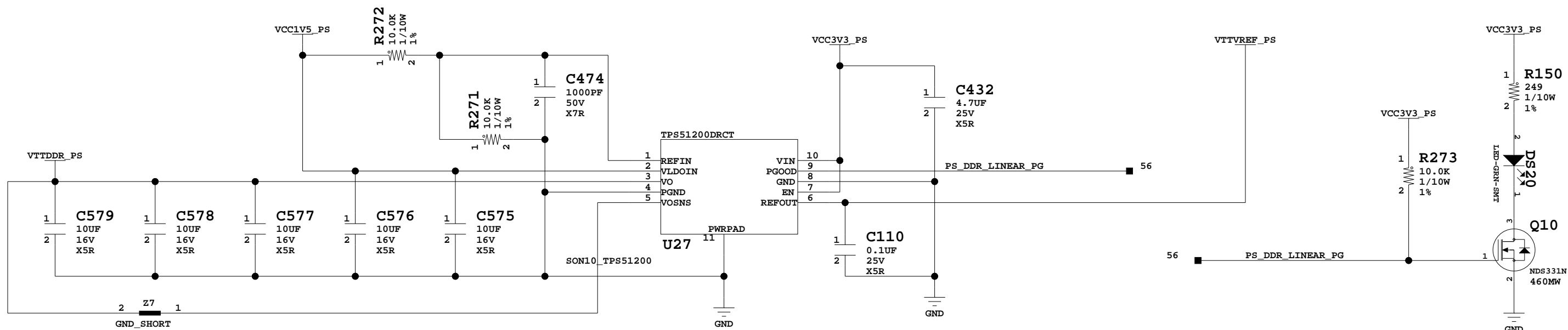
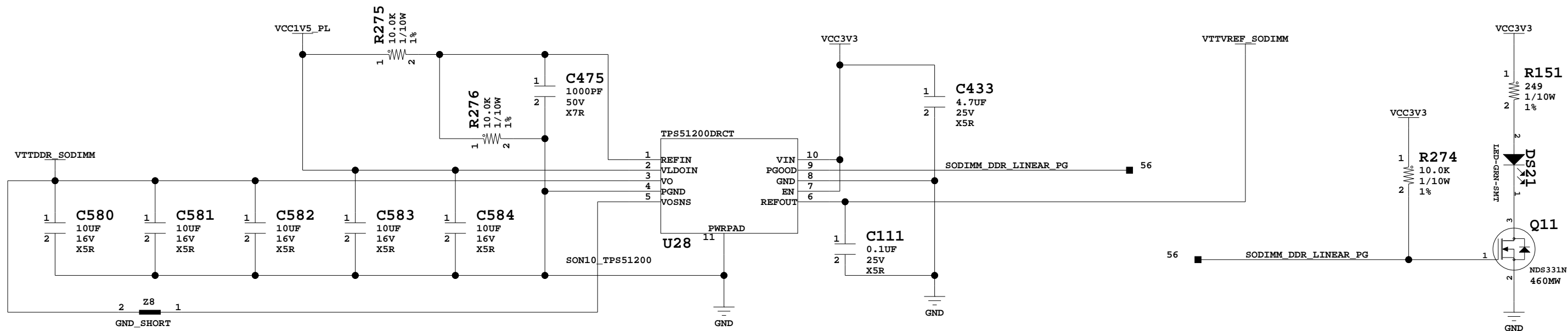
Title: VCC3V3/VCC3V3_FPGA 3.3V SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513	
Date:	10-31-2012_22:05	Ver:	1.1
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Dual switching supplies



Title: Dual switching supplies ZC706 EVALUATION PLATFORM SCHEM, ROHS COMPLIANT		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
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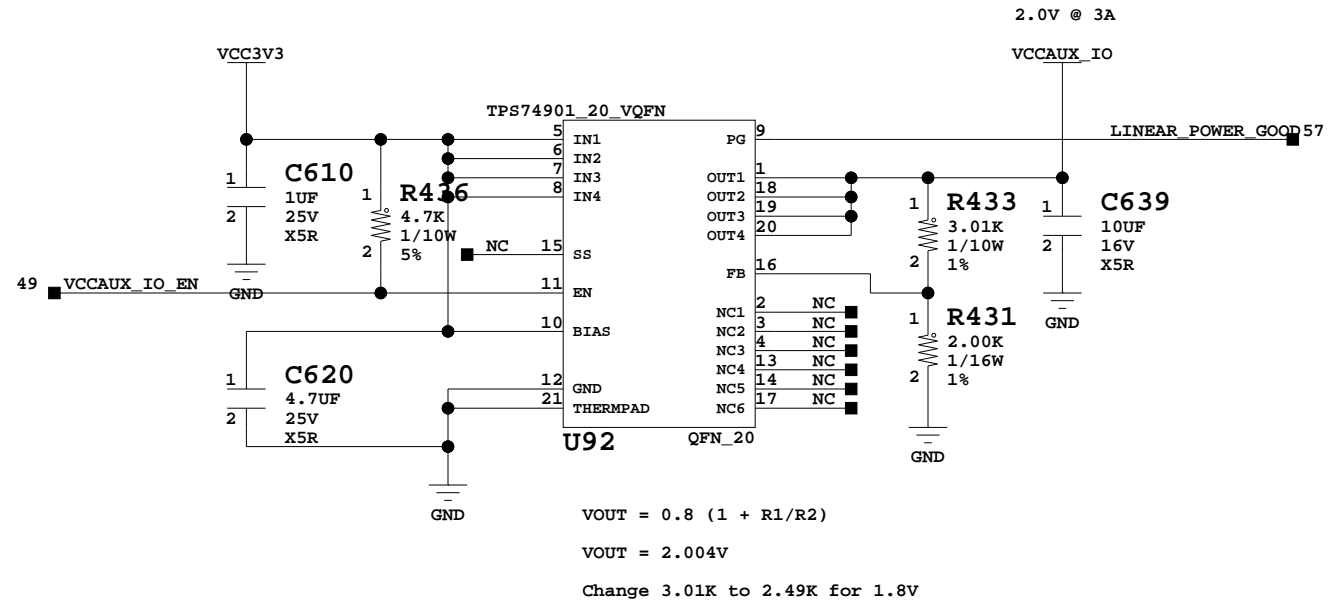
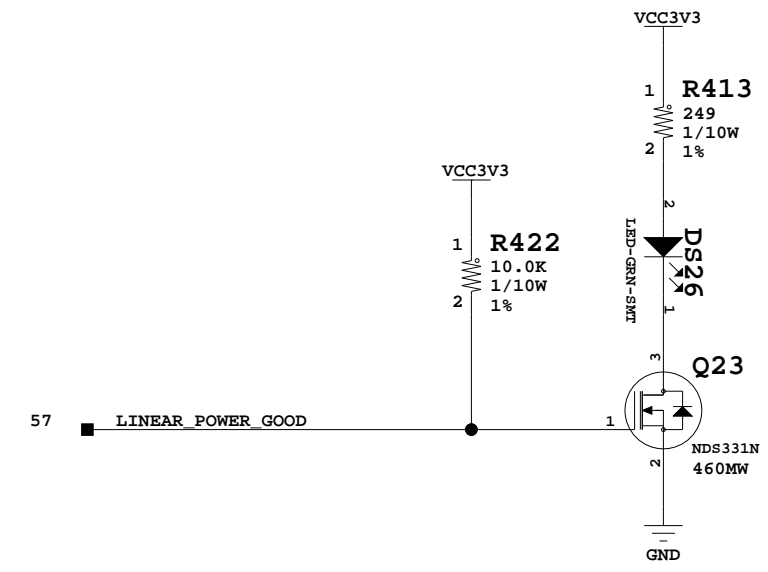
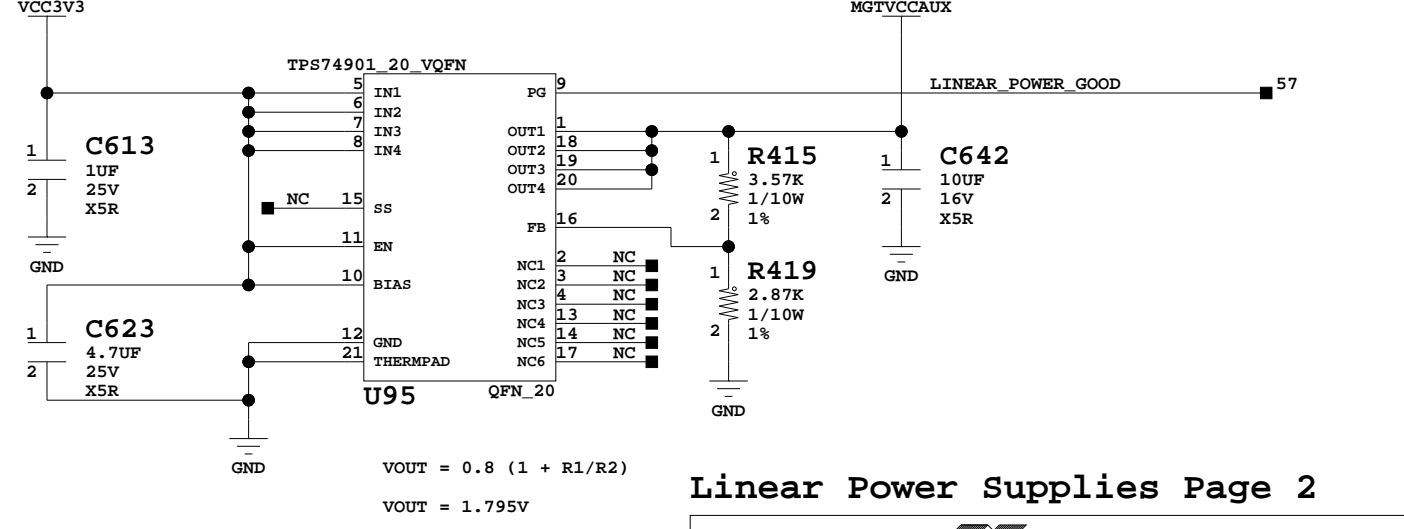
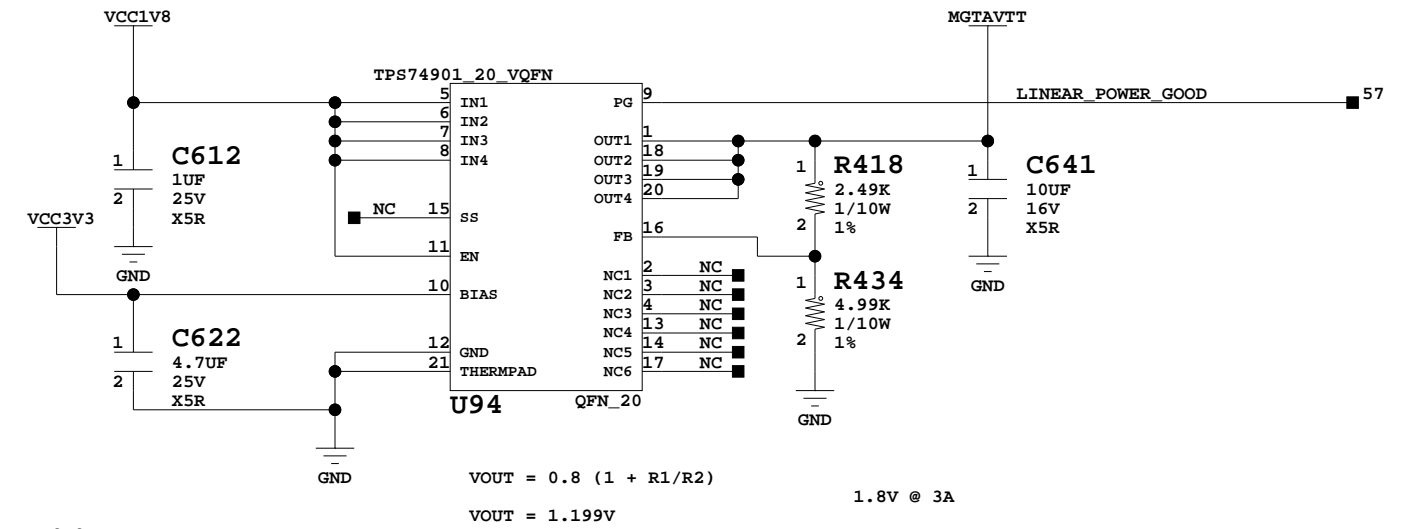
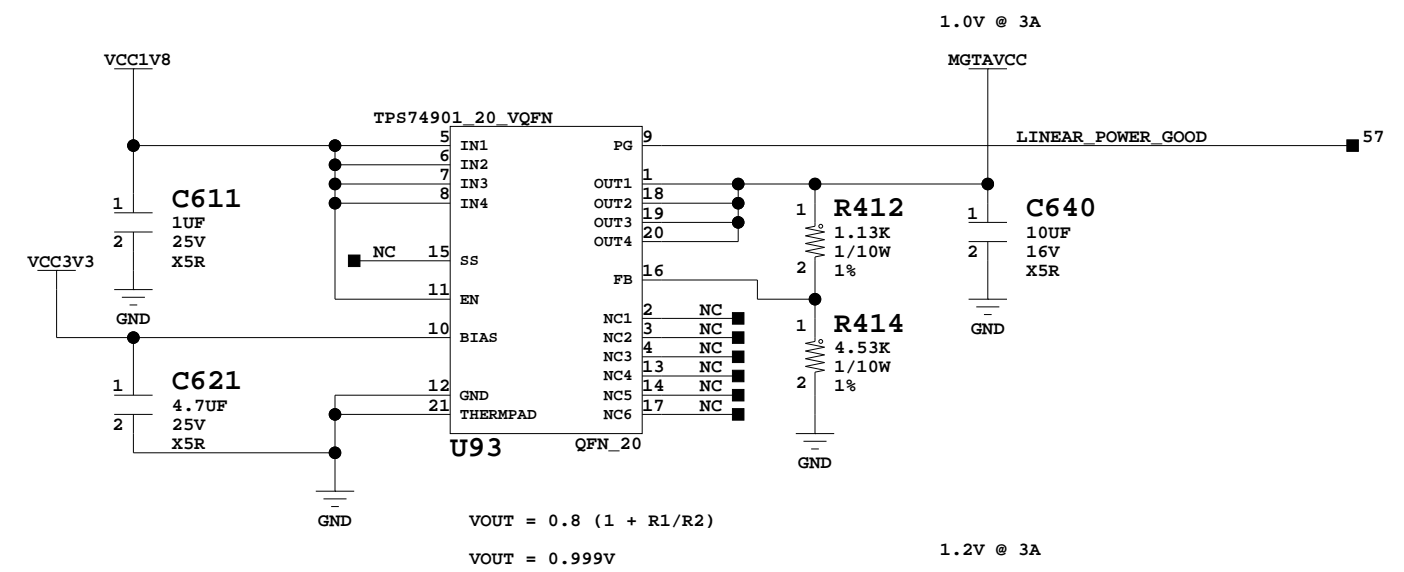
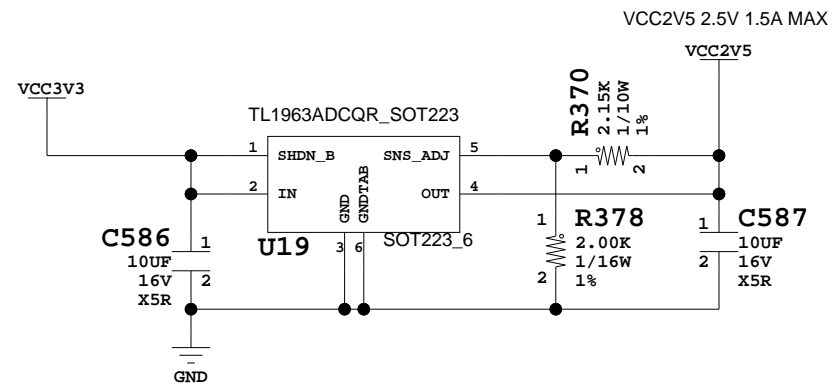


REFER TO DATASHEET
PCB LAYOUT GUIDELINES

Linear Power Supplies Page 1



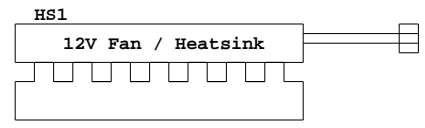
Title: Linear Power Supplies Page 1 SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 56 of 58	Drawn By BF	



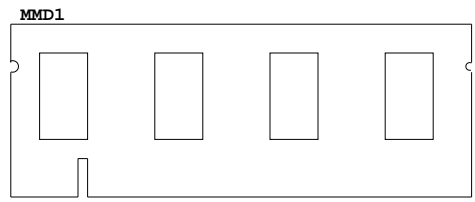
Linear Power Supplies Page 2



Title: Linear Power Supplies Page 2		ASSY P/N: 0431760
ZC706 EVALUATION PLATFORM		PCB P/N: 1280681
SCHEM, ROHS COMPLIANT		SCH P/N: 0381513
Date: 10-31-2012_22:05	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 57 of 58	Drawn By BF	



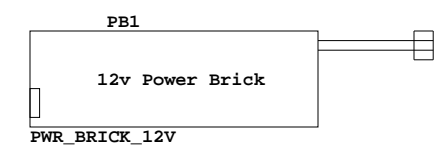
12VDC



DDR3_SODIMM



Power Cord

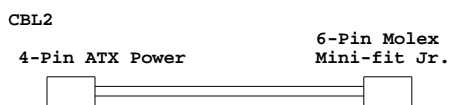


USB Mini-B Cable



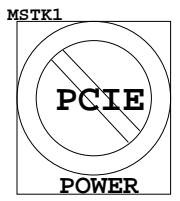
USB Micro-B Cable

USB_MICRO_CABLE

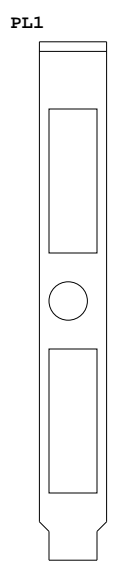


PCIe Adapter Cable

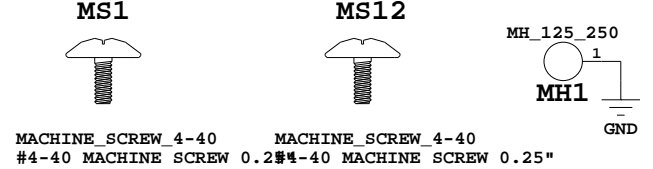
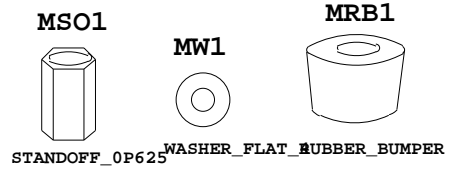
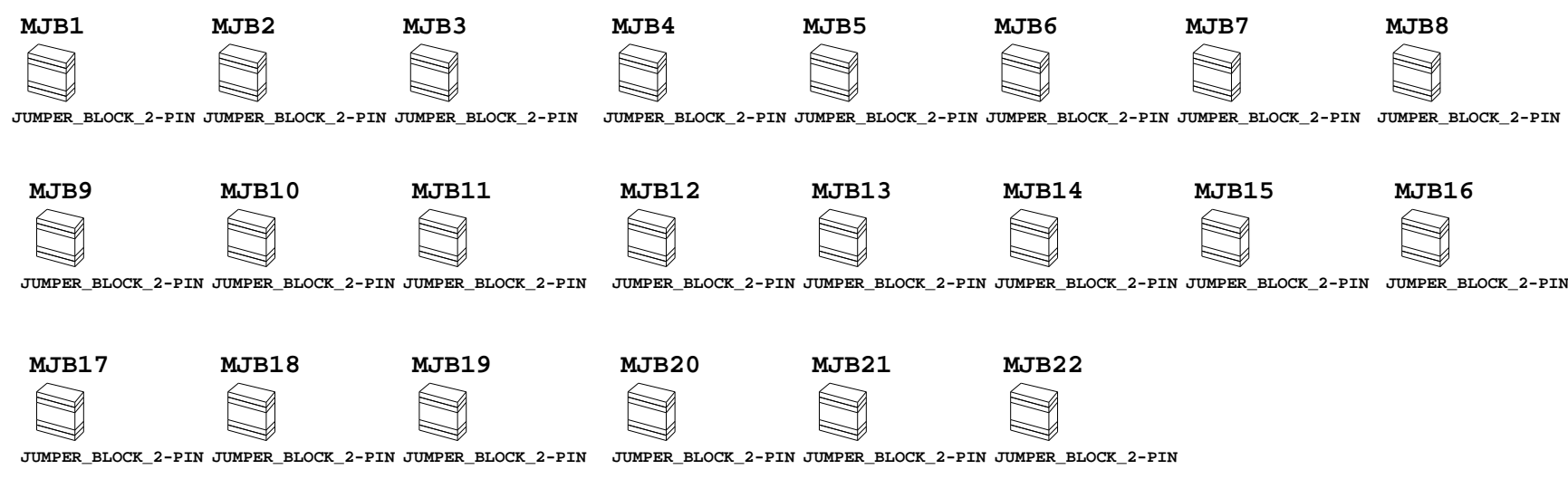
PCIe_ADAPTER_CABLE



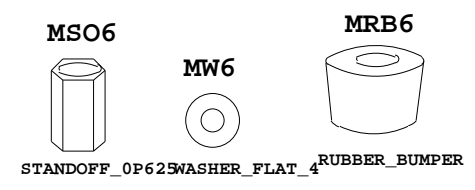
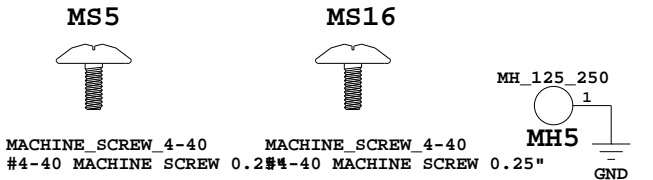
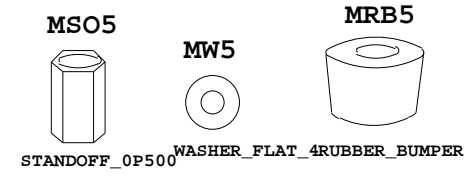
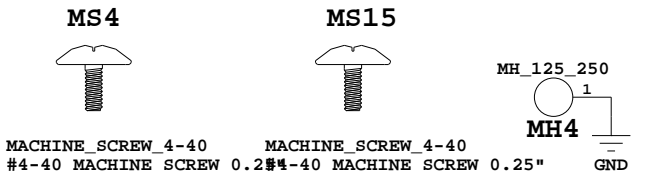
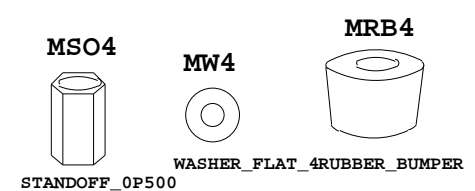
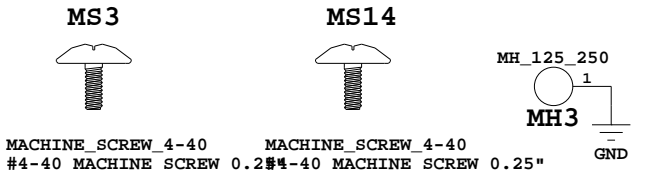
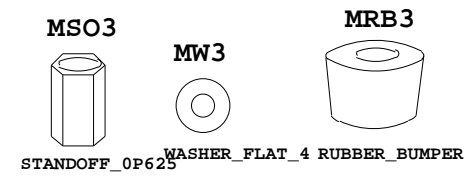
PCIE_POWER_STICKER



ZC706_PCIE_PLATE



NOTE: No standoff foot on MH2



NOTE: These two standoffs are shorter and must be connected to MH4 and MH5 to level the board properly

Mechanical Components



Title: Mechanical Components SCHEM, ROHS COMPLIANT ZC706 EVALUATION PLATFORM		ASSY P/N: 0431760 PCB P/N: 1280681 SCH P/N: 0381513
Date: 11-9-2012_11:18	Ver: 1.1	
Sheet Size: B	Rev: 02	
Sheet 58 of 58	Drawn By BF	